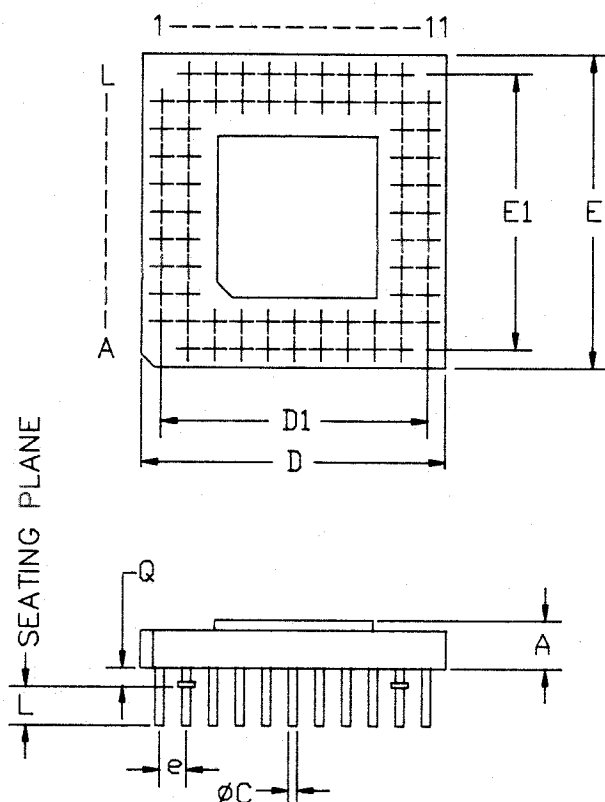
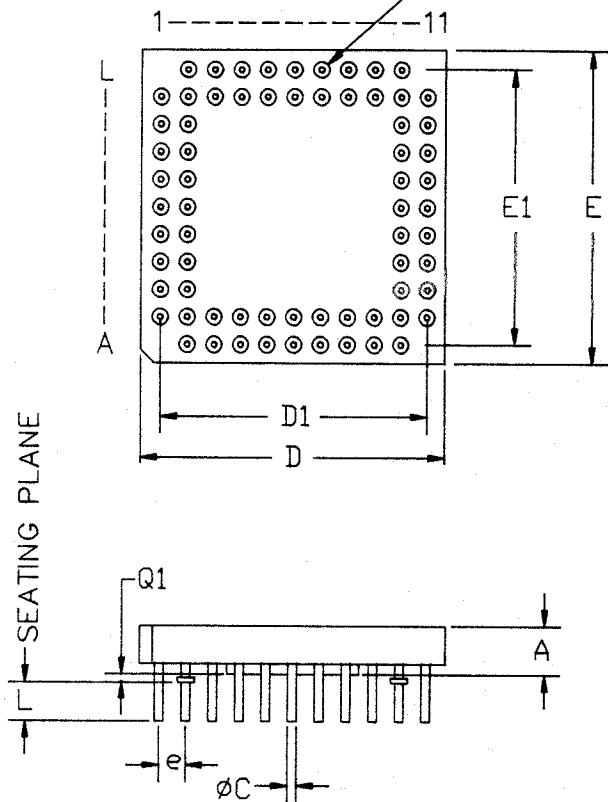


CAVITY DOWN .080 ϕ MAX

CAVITY UP



NOTES: UNLESS OTHERWISE SPECIFIED

1. SYMBOL "M" REPRESENTS THE PGA MATRIX SIZE.
2. SYMBOL "N" REPRESENTS THE NUMBER OF PINS.
3. DIM "A" INCLUDES BOTH THE PKG BODY & THE LID. IT DOES NOT INCLUDE HEATSINK OR OTHER ATTACHED FEATURES.
4. DIM "Q" APPLIES TO CAVITY UP CONFIGURATION AND "Q1" APPLIES TO CAVITY DOWN CONFIGURATION.
5. PIN DIAMETER "C" EXCLUDES SOLDER DIP OR OTHER LEAD FINISH.
6. PIN TIPS MAY HAVE RADIUS OF CHAMFER.

LIMITS SYMBOLS	INCHES		JEDEC	EXCEPTIONS
	MIN	MAX		
A	.115	.160	STD-MO-083-AC	NONE
C	.016	.020		
D	1.140	1.180	TOLERANCES UNLESS OTHERWISE SPECIFIED FRAC DEC ANGLES ± - ± - ± -	
D1	1.000 BSC			
E	1.140	1.180	APPROVALS DATE DRAWN <i>AA</i> 7/88 CHECKED <i>AF</i> 8/88	
E1	1.000 BSC			
e	.100	BSC	Integrated Device Technology, Inc. 3236 Scott Blvd., Santa Clara, CA 95051 (408) 727-6116 TWX: 910-338-2070	
L	.100	.160		
M	11		68 PPGA MKT DWG SCALE SIZE DRAWING NO. REV N/A A PSC-4019 01	
N	68			
Q	.040	.070	DO NOT SCALE DRAWING SHEET 2 OF 2	
Q1	.025	.070		