

# Serial RapidIO Signal Analyzer

## Serial RapidIO Signal Analyzer

- Serial RapidIO Signal Analyzer includes:
  - Hardware: LPC AMC board
  - Software: On-chip Scope (OCS) diagnostic software
- Sample the signal eye diagram at both ends of the link
- Characterize link BER as a function of phase and amplitude
- Evaluate link impact on:
  - Transmitter pre-emphasis
  - Receiver equalization
- No external probe points required
- Optional access to internal IDT Serial RapidIO registers

The Serial RapidlO Signal Analyzer enhances debug capability and accelerates the time-to-market for IDT RapidlO-based designs.

#### LPC Features

- AdvancedMC Form Factor
- Tsi574 Serial RapidIO Switch:
  - Serial RapidIO (Revision 1.3) compliant
  - 1x and 4x mode link width configuration
  - 1.25, 2.5, and 3.125 Gbps link rates
- Serial RapidIO Connectors
  - Two ports routed to AdvancedMC Ports
  - Serial/LVDS connector
  - SMA Coaxial connectors
- JTAG Interface
- USB Host interface
- IPMI Controller
- Stand-alone support from external power supply

#### OCS Software Features

- Windows XP (SP2) compatible
- Easy-to-use GUI
- Control Panel access to:
  - Scope Tool
  - Margining Tool
  - Temperature Sensor
- Link Control and Reporting
  - Pattern Generator
  - Pattern Matcher
  - Frequency
  - Transmit Pre-emphasis
  - Receiver Equalization
  - Link State
  - Bit Error Rate (BER)

The IDT family of RapidIO switches (Tsi572, Tsi574, Tsi576, Tsi577, Tsi578, and Tsi620) enable a system level diagnostic capability using features built into the SerDes. Any Serial RapidIO link connected between IDT switches, or between a IDT switch and a compatible endpoint, can be analyzed with this tool. The Serial RapidIO Signal Analyzer enables this on-die functionality through a hardware component, the Tsi574 Link Partner Card (LPC), and a software component, the On-chip Scope diagnostic software (OCS). These components of the Serial RapidIO Signal Analyzer work together to provide signal visibility and analyze link integrity in IDT RapidIO-based designs.

The Serial RapidlO Signal Analyzer provides visibility of the actual signal eye at the device receiver. This is made possible through the capabilities of the SerDes internal to the IDT switches. With this approach, the effects of package level parasitics are removed providing the user with a true representation of the received RapidlO signal. Full visibility is provided across all RapidlO ports with connections to the LPC or to other IDT switches without the need for external probe points. This reduces functional risk during hardware evaluation by providing an accurate view of signal quality.

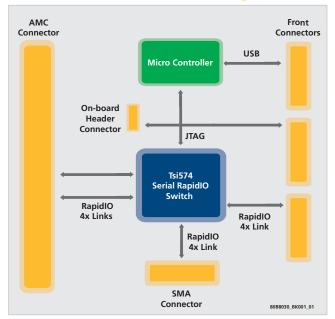
The Serial RapidlO Signal Analyzer contains all the building blocks of a time-sampling oscilloscope without the expense. It supports link testing of 1x and 4x mode, 1.25, 2.5 and 3.125 Gbps Serial RapidlO links.

With the Serial RapidlO Signal Analyzer, any design-under-test (DUT), such as a microTCA chassis, an AdvancedTCA carrier card, the IDT Serial RapidlO Development Platform (SRDP), or other stand-alone hardware, can be characterized.

#### LPC Hardware

The LPC hardware works with the OCS software and provides access to the on-chip functionality within the IDT switches as part of the overall Serial RapidlO Signal Analyzer. However, the LPC capabilities extend beyond being a part of the Serial RapidlO Signal Analyzer and can be used to bridge other serial RapidlO DUT hardware into a MicroTCA environment or connect multiple MicroTCA chassis together. The board supports AdvancedMC, Serial/LVDS, and SMA connectors. The host connection for the OCS software is through a USB connection.

## Link Partner Card Block Diagram



1 of 2

#### Serial RapidlO Switch Features

- High aggregate bandwidth
  - Tsi574 and Tsi576 have 40 Gbps bandwidth
  - Tsi578 has 80 Gbps bandwidth
- Low latency with cut-through capability
- Enhanced SerDes for low power solution
- RapidIO Interconnect Specification (Revision 1.3) compliant
- High performance hardware multicast
- Error management extensions
  - Proactive issue notification
- Port flexibility for multiple I/O bandwidth requirements:
  - Tsi574 has up to four 4x mode ports or eight 1x mode ports
  - Tsi576 has up to two 4x mode ports or twelve 1x mode ports
  - Tsi578 has up to eight 4x mode ports or sixteen 1x mode ports
  - Port frequency configuration to 1.25, 2.5, and 3.125 Gbps
  - Support for mixed speed and width configurations

# **Benefits**

- · Accelerates debug and time-to-market
  - Fast debug, validation, and characterization of high-speed signals
- Enables user to:
  - Verify board design
  - Measure actual eye at the device receiver
  - Evaluate impact of transmitter pre-emphasis and receiver equalization on signal integrity
- Reduces test expenses

# Design Support Tools

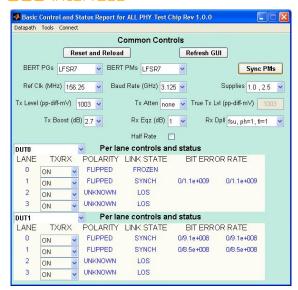
IDT is committed to helping customers minimize their time to market. That's why we provide one of the highest levels of design support in the industry, including:

- Application notes
- Evaluation boards
- IC models
- Hardware and software development tools

# OCS Software

The OCS software operates on a windows-based computer with a USB port. The easy-to-use graphical user interface (GUI) contains the parameter controls to optimize the receiver and transmitter link characteristics. The software also provides status and system reports.

#### OCS Interface



The LPC and OCS generate, collect, and display physical data about signal integrity in your RapidlO design.

Analyzer Eye Diagram

Stope Tool

Stope Tool

Stope Tool

Channel: 0, Baud=320ps, Res: (256 \* 2.0) x 47879

DUTO

Chan: 0

X Points per baud: 256

Start/Span display

0 2

Presets:

Release Rx At S...

Tight Yeax

X Scale:
ps

Man Stope: 7505 501 m/ys
Max Pic-R: 26.2500 ps

Signa: 41.7359 ps rms

100

100

200

300

40

Time (ps)

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