24 Lane 3-Port Non-Transparent PCI Express Switch

PES24N3
Product Brief

Device Overview

The PES24N3, 24 lane 3-port PCI Express switch, is a member of IDT's PCI Express based bridge and switch devices offering the next-generation I/O interconnect standard. The PES24N3 is a peripheral chip that performs PCI Express Base switching with a feature set optimized for high performance x8 applications such as graphics and storage. It provides fan-out and switching functions between a PCI Express upstream port and two downstream ports or peer-to-peer switching between downstream ports.

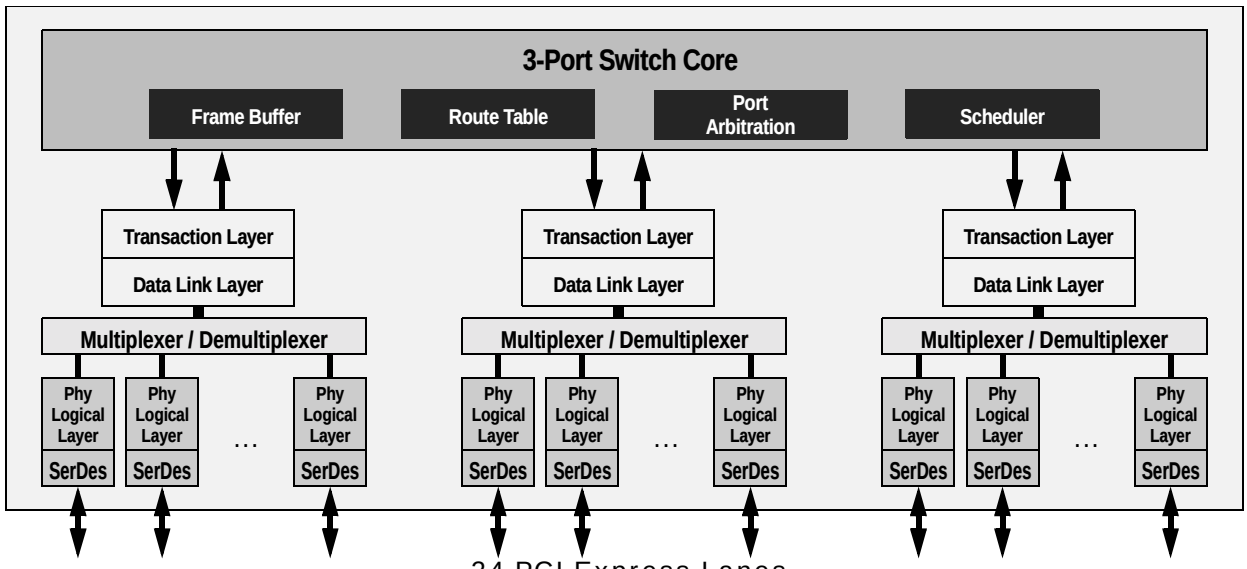
In addition to transparent switching, one port of the PES24N3 may be configured to operate in non-transparent mode. This allows the PES24N3 to be used in multi-host and intelligent I/O applications such as communications, storage, and blade servers.

Features

- **High Performance PCI Express Switch**
  - *Three x8 ports with 24 PCI Express lanes*
  - *Delivers 12 GBps (96 Gbps) aggregate switching capacity*
  - *Low latency cut-through switch architecture*
  - *Supports 128 and 256 byte maximum payload size*
  - *Supports one virtual channel*
  - *PCI Express Base specification Revision 1.0a compliant*
- **Flexible Architecture with Numerous Configuration Options**
  - *Port arbitration schemes utilizing round robin or weighted round robin algorithms*
  - *One port configurable as downstream or non-transparent port*
  - *Supports automatic per port link width negotiation (x8, x4, x2 or x1)*
  - *Supports static lane reversal on all ports*
  - *Supports polarity inversion*
  - *Supports locked transactions, allowing use with legacy software*
  - *Ability to load device configuration from serial EEPROM*
- **Non-Transparent Port**
  - *Supports four mapping windows*
    - *Each may be configured as a 32-bit memory or I/O window*
    - *May be paired to form a 64-bit memory window*
  - *Interprocessor communication*
    - *32 inbound and outbound doorbells*
    - *Four inbound and outbound message registers*
    - *Eight shared shadow registers*
  - *Allows up to 16 masters to communicate through the non-transparent switch*
  - *No limit on the number of supported outstanding transactions through the non-transparent bridge*
  - *Completely symmetric non-transparent bridge operation allows similar/same configuration software to be run on both sides*
  - *Supports direct non-transparent port to non-transparent port connection*
- **Highly Integrated Solution**
  - *Requires no external components*
  - *Incorporates on-chip internal memory for packet buffering and queueing*
  - *Integrates 24 2.5 Gbps embedded SerDes, 8B/10B encoder/decoder (no separate transceivers needed)*

Advance Information

Block Diagram



24 PCI Express Lanes

x8 Upstream Port and Two x8 Downstream Ports

- **Reliability, Availability, and Serviceability (RAS) Features**
  - *Internal end-to-end parity protection on all TLPs ensures data integrity even in systems that do not implement end-to-end CRC (ECRC)*
  - *Supports ECRC in transparent mode*
  - *Supports PCI Express Native Hot-Plug*
    - *Compatible with Hot-Plug I/O expanders used on PC motherboards*
  - *Supports Hot-Swap*
- **Power Management**
  - *Support PCI Express Power Management Interface specification, Revision 1.1 (PCI-PM)*
  - *Unused SerDes are disabled.*
  - *Supports Advanced Configuration and Power Interface Specification, Revision 2.0 (ACPI) supporting active link state*
- **Testability and Debug Features**
  - *Supports IEEE 1149.6 JTAG*
  - *Built in SerDes Pseudo-Random Bit Stream (PRBS) generator*
  - *Ability to read and write any internal register via the SMBus*
  - *Ability to bypass link training and force any link into any mode*
  - *Provides statistics and performance counters*
- **16 General Purpose Input/Output pins**
- **Packaged in a 27x27 BGA with 1mm ball spacing**

Product Description

Utilizing standard PCI Express interconnect the PES24N3 provides the most efficient fan-out device for applications requiring high throughput, low latency and simple board layout. It provides 12 GBps (96 Gbps) of aggregated, full-duplex switching capacity through 24 integrated serial lanes. Each lane provides 2.5 Gbps of bandwidth in both directions and is fully compliant with PCI Express Base specification 1.0a.

The PES24N3 is based on a flexible and efficient layered architecture. The PCI Express layer consists of SerDes, Physical, Data Link and Transaction layers in compliance with PCI Express Base specification Revision 1.0a. The PES24N3 can operate either as a store and forward or cut-through switch depending on the packet size and is designed to switch memory and I/O transactions. It supports eight Traffic Classes (TCs) and one Virtual Channel (VC) with sophisticated resource management. This includes system selectable algorithms such as round robin, weighted round-robin, and strict priority schemes guaranteeing bandwidth allocation and/or latency for critical traffic classes.

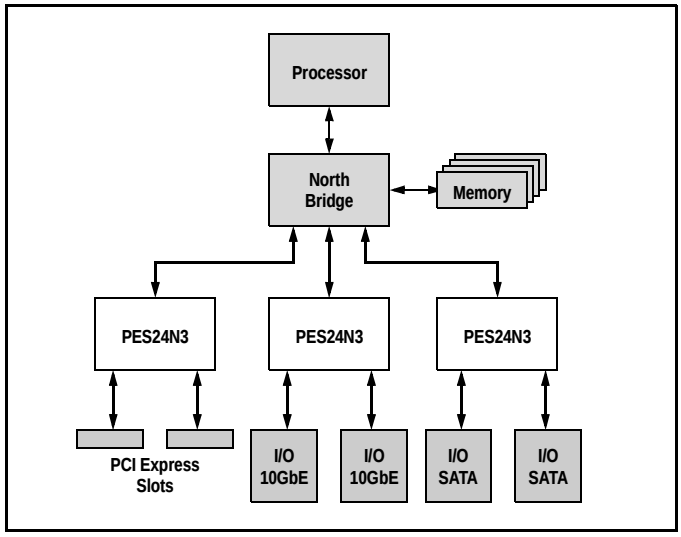


Figure 1 I/O Expansion Application

Advance Information

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