AS3812

16-Channel LED Driver for Local Dimming

The AS3812 is the next generation of fully integrated 16-channel LED backlight driver. LED current set resistors are integrated in order to save external components as well as reducing the pin-count of the IC while maintaining a very high absolute LED current accuracy of ±1%.

The speed of the current regulation has been increased to support minimum PWM on times down to 1µs.12-bit fully flexible PWM generators per channel and 10-bit LED current resolution can be used to adjust the brightness of the LED strings.

Dialog's patented digital enhanced DC/DC feedback function is regulating any external SMPS to the best suitable output voltage needs of the LED strings to minimize power dissipation.

Dialog's patented dimming method allows synchronizing the PWM generators with V/HSYNC of the video SOC/GPU.

The device can be programmed via SPI and daisy chain connection to cascade many devices easily.

Features

- 16 fully flexible, 12-bit PWM generators provide optimium power savings through local dimming
  - Period, high time, delay, reverse functions
- Global 10-bit IDAC gives ±1% LED current accuracy for highest brightness uniformity
- Integrated current sink FETs and current set resistors – Lower BOM cost
- VSYNC and HSYNC inputs and integrated digital PLL allow synchronization with TV frame
- Universally compatible DC/DC feedback architecture with digital enhancement – configurable via SPI
- Fully protected with integrated features
  - Short/Open LED detection
  - Over-temperature shutdown
  - Register lock/unlock
- Minimum PWM on-time of 1µs – enables high contrast ratios

Applications

- Ultra-HD/4K TVs
- LCD Monitors
- Notebooks/medium-small size displays

1. Overview

1.1 Typical Application

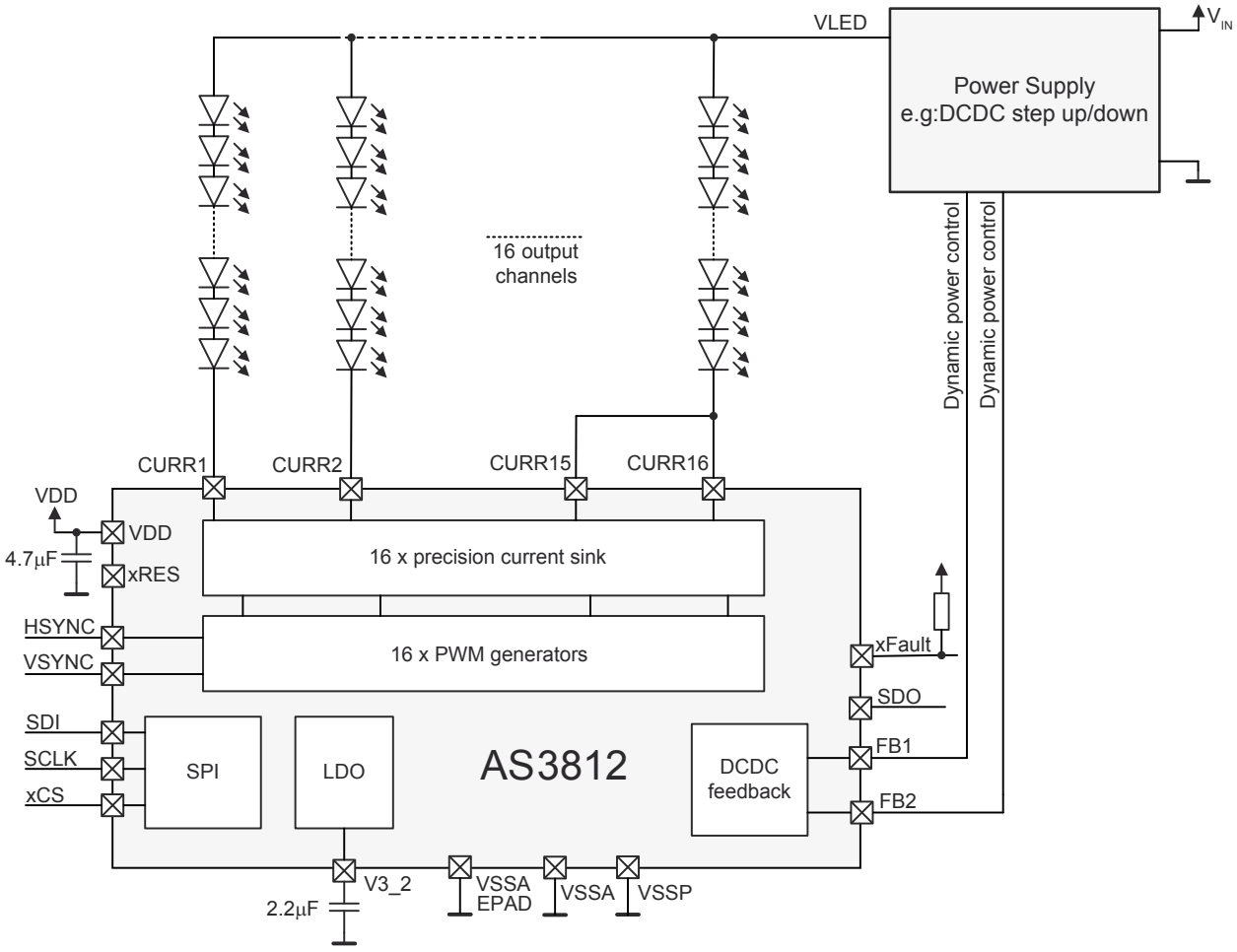


Figure 1. AS3812 Typical Application (With CURR15 and CURR16 connected together to show increased LED string current capability by paralleling outputs)

2. Pin Information

2.1 Pin Assignments

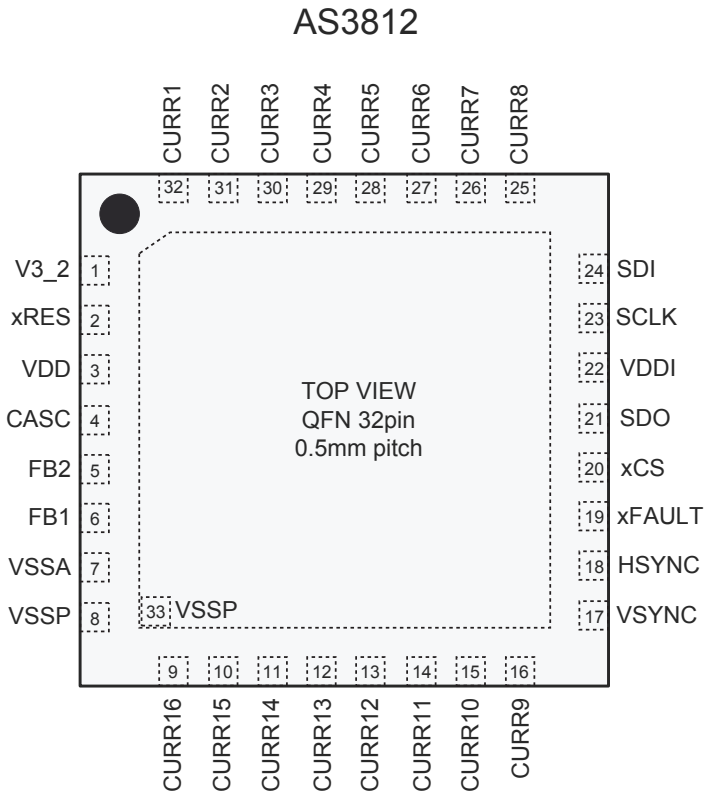


Figure 2. Top View

2.2 Pin Description

Pin Number	Pin Name	Type	Description	If Not Used
1	V3_2	P	Output of 3.2V LDO Connect 2.2mF capacitor to GND	
2	xRES	DI	Reset input active low Connect pull up resistor to VDDI	
3	VDD	P	Supply Voltage input Connect 4.7mF bypass capacitor to GND	
4	CASC	A_I/O	Connect to external cascade circuit	Leave open
5	FB2	A_I/O	Power supply feedback Connect to external SMPS	Leave open
6	FB1	A_I/O	Power supply feedback Connect to external SMPS	Leave open
7	VSSA	P	GND	
8	VSSP	P	GND	
9	CURR16	A_I/O	LED current output	Leave open
10	CURR15	A_I/O	LED current output	Leave open
11	CURR14	A_I/O	LED current output	Leave open
12	CURR13	A_I/O	LED current output	Leave open
13	CURR12	A_I/O	LED current output	Leave open

Pin Number	Pin Name	Type	Description	If Not Used
14	CURR11	A_I/O	LED current output	Leave open
15	CURR10	A_I/O	LED current output	Leave open
16	CURR9	A_I/O	LED current output	Leave open
17	VSYNC	DI-PD	Vertical sync frequency, PWM generator start/ reset, DPLL input	Leave open
18	HSYNC	DI-PD	External clock input	Leave open
19	xFAULT	DO-OD	Fault output (interrupt, active low) Connect pull up resistor to VDDI	Leave open
20	xCS	DI-PU	SPI interface chip select (active low)	Leave open
21	SDO	DO	SPI interface data output Daisy Chain: Connect to SDI of next device	Leave open
22	VDDI	P	Power Supply of digital input/output cells	Leave open
23	SCLK	DI-PD	SPI interface clock	Leave open
24	SDI	DI-PD	SPI interface data input	Leave open
25	CURR8	A_I/O	LED current output	Leave open
26	CURR7	A_I/O	LED current output	Leave open
27	CURR6	A_I/O	LED current output	Leave open
28	CURR5	A_I/O	LED current output	Leave open
29	CURR4	A_I/O	LED current output	Leave open
30	CURR3	A_I/O	LED current output	Leave open
31	CURR2	A_I/O	LED current output	Leave open
32	CURR1	A_I/O	LED current output	Leave open
33	EP	P	Exposed Pad: Connect to GND	

A_I/O: Analog pin
P: Power pin
DO: Digital Output
DO_OD: Digital Output Open Drain
DI: Digital Input
DI_PU: Digital Input with Pull Up resistor
DI_PD: Digital Input with Pull Down resistor

3. Specifications

3.1 Absolute Maximum Ratings

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.

Parameter	Symbol	Comments	Min	Max	Unit
Supply Voltage to Ground	V_{DDMAX} / V_{GND}	Applicable for pin VDD	-0.3	7	V
Maximum Voltage	V_{IN_5V}	Applicable for pins: FB1, FB2, VSYNC,HSYNC, V3_2, SDI, SDO, SCLK, xCS, xFAULT, xRES, VDDI	-0.3	VDD+ 0.3	V
Maximum voltage CURRx pins	V_{IN_30V}	Applicable for pins: CURR1-CURR16	-0.3	30	V

3.2 ESD Ratings

ESD Model/Test	Symbol	Rating	Unit
On all 5V pins Human Body Model (Tested per JS-001-2017)	ESD_{HBM_LV}	±2000	V
On all HV pins Charged Device Model (Tested per JS-001-2017)	ESD_{HBM_HV}	±8000	V
CDM (Tested per JESD78E)	ESD_{CDM}	±500	V
MM (Tested per JESD78E)	ESD_{MM}	±100	V
Latch-Up (Tested per JESD78E; Class 2, Level A)	I_{SCR}	±100	mA

3.3 Recommended Operating Conditions

Parameter	Symbol	Comments	Min	Max	Unit
Package Body Temperature	T_{BODY}	IPC/JEDEC J-STD-020 The reflow peak soldering temperature (body temperature) is specified according to IPC/JEDEC J-STD-020 “Moisture/Reflow Sensitivity Classification for Non-hermetic Solid State Surface Mount Devices.” The lead finish for Pb-free leaded packages is “Matte Tin” (100% Sn)		260	°C
Relative Humidity (non-condensing)	RH_{NC}		5	85	%
Moisture Sensitivity Level	MSL	Maximum floor life time of 168h	3		

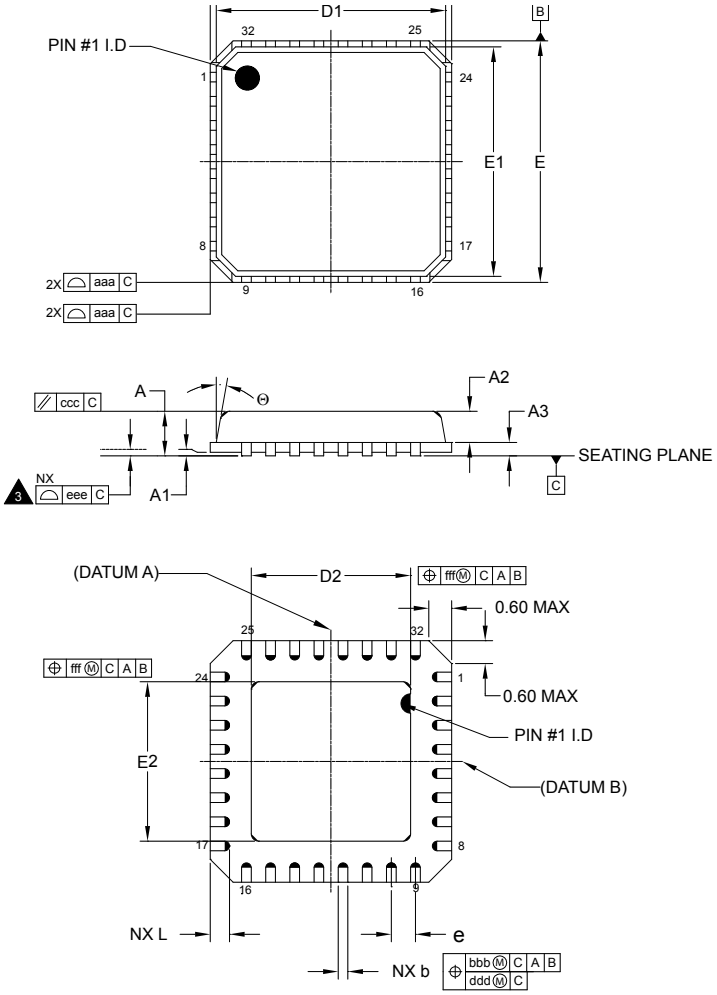
3.4 Thermal Specifications

Thermal Resistance (Typical)	θ_{JA} (°C/W)
QFN-32 package	35

Parameter	Symbol	Minimum	Maximum	Unit
Maximum Junction Temperature	T_J	-20	+115	°C
Maximum Storage Temperature Range	T_{STRG}	-55	+150	°C

4. Package Outline Drawings

The package outline drawings are located at the end of this document and are accessible from the Renesas website. The package information is the most current data available and is subject to change without revision of this document.



REF.	MIN	NOM	MAX
A	0.80	0.90	1.00
A1	0	0.02	0.05
A2	-	0.65	1.00
A3		0.20 REF	
L	0.35	0.40	0.45
Θ	0°	-	14°
b	0.18	0.25	0.30
D		5.00 BSC	
E		5.00 BSC	
e		0.50 BSC	
D2	3.40	3.50	3.60
E2	3.40	3.50	3.60
D1		4.75 BSC	
E1		4.75 BSC	
aaa	-	0.15	-
bbb	-	0.10	-
ccc	-	0.10	-
ddd	-	0.05	-
eee	-	0.08	-
fff	-	0.10	-
N		32	

NOTE:

1. DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES)
3. COPLANARITY APPLIES TO THE EXPOSED HEAT SLUG AS WELL AS THE TERMINAL.
4. RADIUS ON TERMINAL IS OPTIONAL.
5. N IS THE TOTAL NUMBER OF TERMINALS.

Figure 3. QFN-32 Package Outline Drawing

5. Ordering Information

Part Number	Ordering Code	Options	Package	Description
AS3812A	AS3812A-ZQFT	16-Channel Version	32-Pin QFN	Tape & Reel[1]

1. Tape & Reel packing quantity is 4,000/reel. Minimum packing quantity is 4,000.

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Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact Information

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