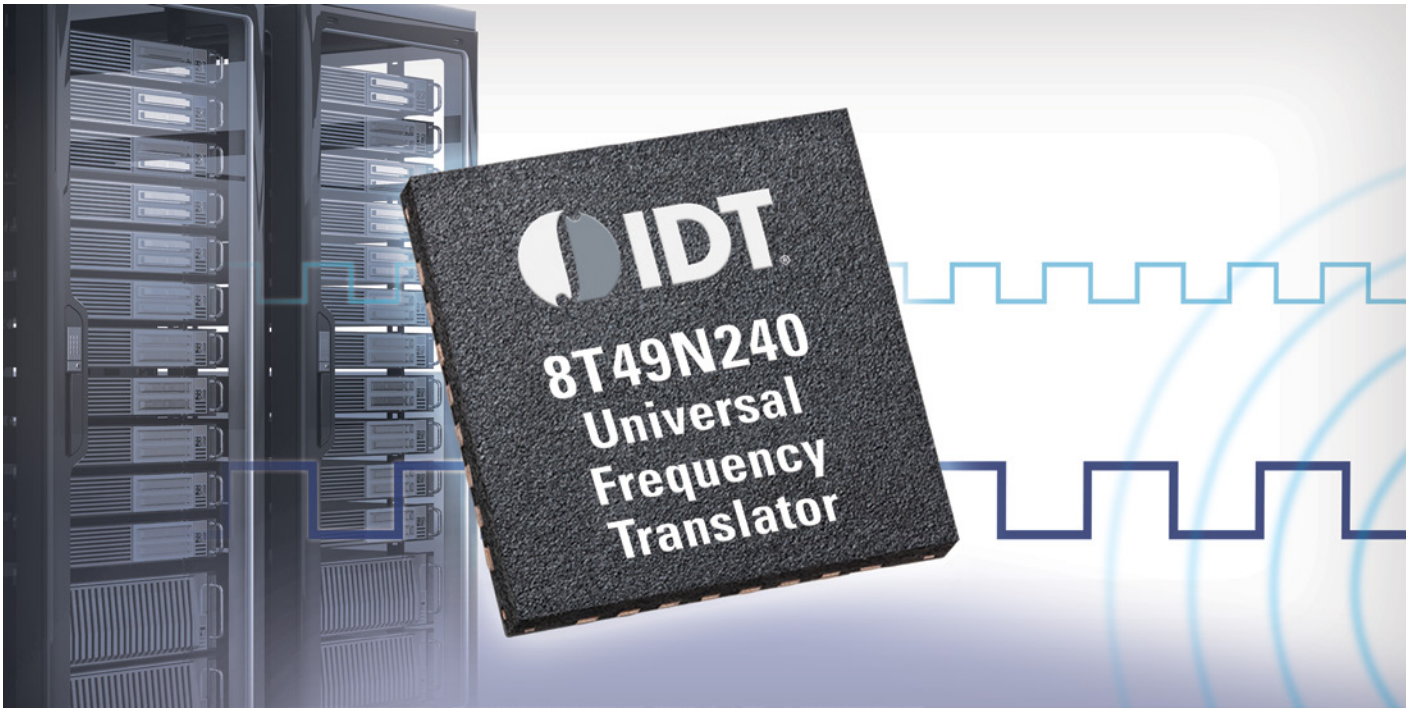
Integrated Device Technology

8T49N240 Sub-200fs Universal Frequency Translator



FEATURES

- Four differential outputs supporting HCSL, LVDS or LVPECL plus 2 x LVCMOS option
- Excellent jitter performance
  - < 200fs RMS (typical - including spurs): 12 kHz to 20 MHz for integer-divider outputs
- Operating Modes: Synthesizer, Jitter Attenuator
- Operates from a 10 to 54 MHz fundamental-mode crystal
- Accepts up to two LVPECL, LVDS, LVHSTL, or LVCMOS input clocks
- Flexible support for input redundancy
- Compact 6 x 6 mm 40-VQFN package

TARGET APPLICATIONS

- 40Gbps / 100Gbps datacenter switches
- Reference clocks for FPGAs
- Backhaul networks supporting 4G/4.5G & 5G mobile radio networks
- 10 Gbps / 40Gbps / 100Gbps datacom & telecom wide-area network switches & routers

The 8T49N240 high-performance clock generator and jitter attenuator features the ability to produce virtually any output frequency from virtually any input frequency. This highly-flexible device is a member of IDT's third-generation Universal Frequency Translator (UFT™) family and is ideal for 10Gbps or multi-lane 40Gpbs / 100Gbps timing applications where 300fs of phase noise is typically the maximum acceptable amount allowed at the physical ports. The 200fs phase noise specification of the 8T49N240 provides ample noise margin, enabling engineers to simplify their clock tree designs and utilize lower cost PCBs.

The 8T49N240 is a fractional-feedback single channel jitter attenuator with frequency translation. It is equipped with three integer and one fractional output dividers, allowing generation of up to four different output frequencies, ranging from 8 kHz to 867 MHz. These frequencies are completely independent of the input reference frequencies and the crystal reference frequency. The outputs may select among LVPECL, LVDS, HCSL, or LVCMOS output levels.

The device accepts up to two differential or single-ended input clocks and a fundamental-mode crystal input. The internal PLL can lock to either of the input reference clocks or just to the crystal to behave as a frequency synthesizer.

The 8T49N240 supports hitless reference switching between input clocks. The device monitors both input clocks for Loss of Signal (LOS), and generates an alarm when an input clock failure is detected. Automatic and manual hitless reference switching options are supported. LOS behavior can be set to support gapped or un-gapped clocks.

The 8T49N240 is programmable through an I^2C interface. It also supports I^2C master capability to allow the register configuration to be read from an external EEPROM. Factory pre-programmed devices are also available using the on-chip One Time Programmable (OTP) memory. The compact 6 x 6 mm footprint requires considerably less PCB area than most other solutions with this level of performance and flexibility.

To request samples, download documentation or learn more visit: **idt.com/8T49N240**