



SHORT FORM DATA SHEET

This Short Form Data Sheet is intended to provide an overview only. A full-version datasheet is available on the product page at www.IDT.com.

General Description

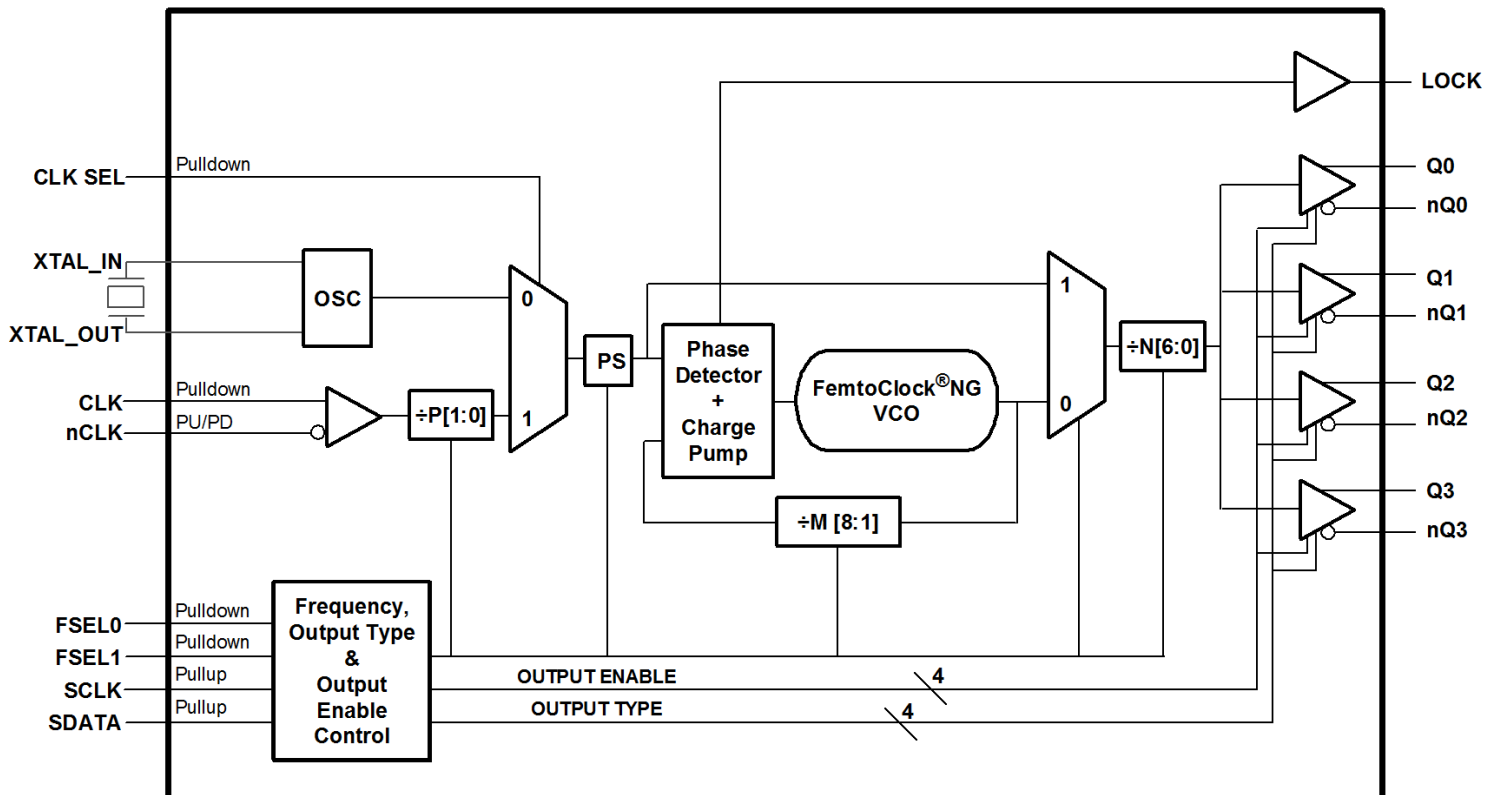
The IDT8T49N004I is a four output Clock Generator with selectable LVDS or LVPECL outputs. The IDT8T49N004I can generate any one of four frequencies from a single crystal or reference clock. The four frequencies are selected from the Frequency Selection Table (Table 1) and are programmed via I²C interface. The four predefined frequencies are selected in the user application by two frequency selection pins. Note the desired programmed frequencies must be used with the corresponding crystal or clock frequency as indicated in Table 1.

Excellent phase noise performance is maintained with IDT's Fourth Generation FemtoClock® NG PLL technology, which delivers sub-400fs RMS phase jitter.

Features

- Fourth Generation FemtoClock® NG PLL technology
- Four selectable LVPECL or LVDS outputs via I²C
- CLK, nCLK input pair can accept the following differential input levels: LVPECL, LVDS, HCSL
- FemtoClock NG VCO Range: 1.91GHz - 2.5GHz
- RMS phase jitter at 156.25MHz (12kHz - 20MHz): 228fs (typical)
- RMS phase jitter at 156.25MHz (10kHz - 1MHz): 175fs (typical)
- Full 2.5V or 3.3V power supply
- I²C programming interface
- PCI Express (2.5 Gb/s), Gen 2 (5 Gb/s), and Gen 3 (8 Gb/s) jitter compliant
- -40°C to 85°C ambient operating temperature
- Available in lead-free (RoHS 6) package

Block Diagram



Frequency Configuration

Table 1. Frequency Configuration Examples

Output Frequencies (MHz)	Input Frequency or Crystal Frequency (MHz)	Input Clock Divider P	Input Clock Prescaler PS	Feedback Divider M	Output Divider N	VCO Frequency (MHz)
30.72	30.72	1	x2	32	64	1966.08
61.44	30.72	1	x2	32	32	1966.08
62.5	25	1	x2	40	32	2000
76.8	30.72	1	x2	40	32	2457.6
78.125	25	1	x2	50	32	2500
100	25	1	x2	40	20	2000
106.25	26.5625	1	x2	40	20	2125
122.8	30.72	1	x2	32	16	1966.08
125	25	1	x2	40	16	2000
133.33	25	1	x2	48	18	2400
148.5	27	1	x2	44	16	2376
150	25	1	x2	42	14	2100
153.6	30.72	1	x2	40	16	2457.6
155.52	19.44	1	x2	64	16	2488.32
156.25	25	1	x2	50	16	2500
	100	2	x1	50	16	2500
	125	5	x2	50	16	2500
159.375	26.5625	1	x2	36	12	1912.5
160	20	1	x2	48	12	1920
166.66	25	1	x2	40	12	2000
184.32	30.72	1	x2	36	12	2211.84
	61.44	1	x1	36	12	2211.84
187.5	25	1	x1	90	12	2250
200	25	1	x2	40	10	2000
212.5	26.5625	1	x2	40	10	2125
250	25	1	x2	40	8	2000
300	25	1	x2	48	8	2400
311.04	19.44	1	x2	64	8	2488.32
	77.76	1	x1	32	8	2488.32
	155.52	2	x1	32	8	2488.32
312.5	25	1	x2	50	8	2500
	125	2	x1	40	8	2500
	156.25	5	x2	40	8	2500
318.75	26.5625	1	x2	36	6	1912.5
322.265625	25.78125	2	x1	150	6	1933.59375
375	25	1	x1	90	6	2250
400	25	1	x2	40	5	2000
425	26.5625	1	x2	40	5	2125
491.52	30.72	1	x2	32	4	1966.08

Table 1. Frequency Configuration Examples

Output Frequencies (MHz)	Input Frequency or Crystal Frequency (MHz)	Input Clock Divider P	Input Clock Prescaler PS	Feedback Divider M	Output Divider N	VCO Frequency (MHz)
614.4	30.72	1	x2	40	4	2457.6
	122.88	2	x1	40	4	2457.6
	153.6	5	x2	40	4	2457.6
622.08	19.44	1	x2	64	4	2488.32
625	25	1	x2	50	4	2500
1228.88	30.72	1	x2	40	2	2457.6

NOTE: Each device supports 4 output frequencies (with related input or crystal value) as selected from this table Register Settings.

NOTE: XTAL operation: $f_{OUT} = f_{REF} * PS * M / N$; CLK, nCLK input operation: $f_{OUT} = (f_{REF} / P) * PS * M / N$.

Power-up Default Configuration Description

The IDT8T49N004I supports a variety of options such as different output styles, number of programmed default frequencies, output enable and operating temperature range. The device options and default frequencies must be specified at the time of order and are programmed by IDT prior to shipment. The document, *Programmable FemtoClock[®] NG Product Ordering Guide* specifies the available order codes, including the device options and default frequency configurations.

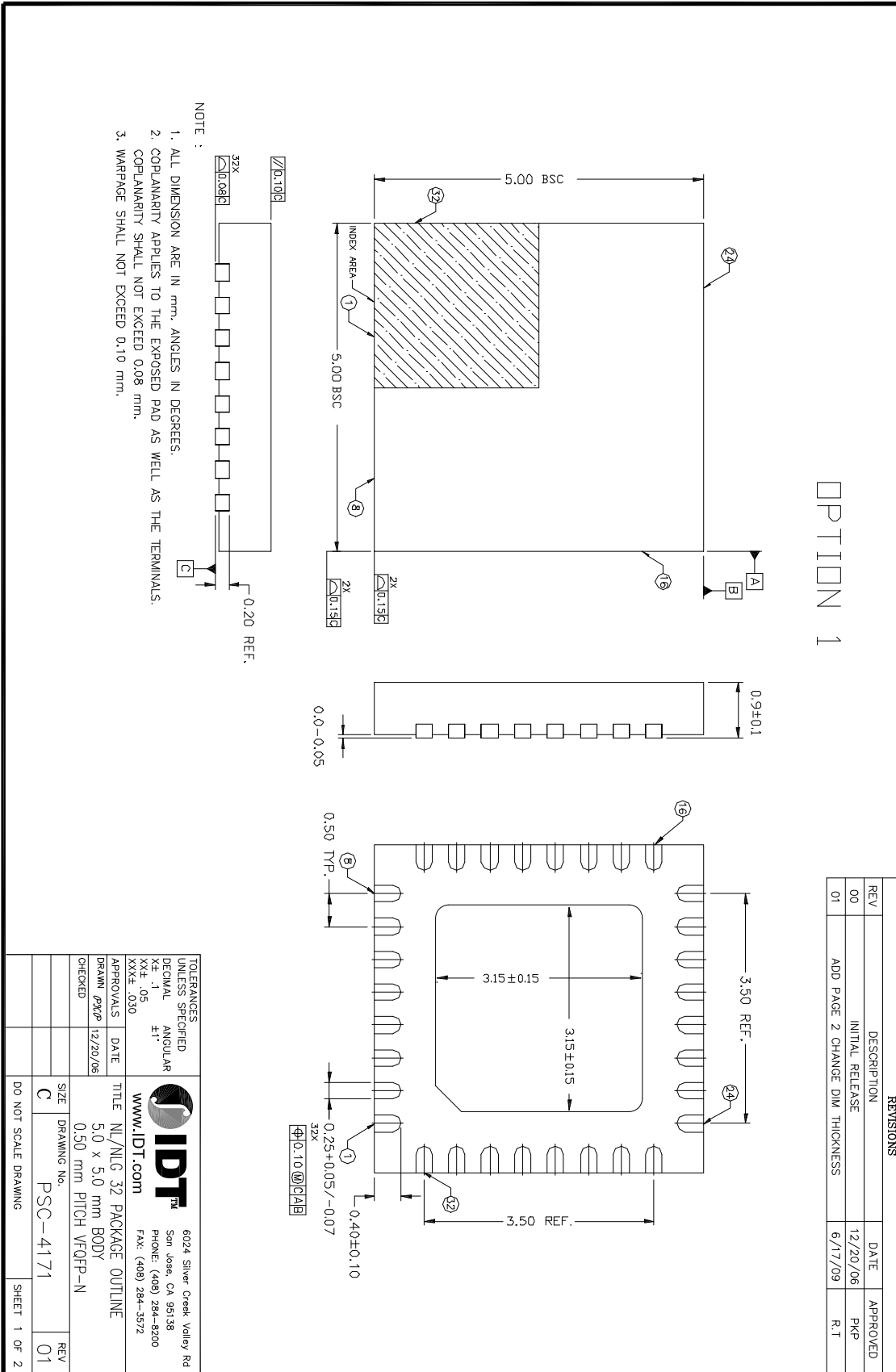
Other order codes with respective programmed frequencies are available from IDT upon request. After power-up changes to the output frequencies are controlled by FSEL[1:0] or the I²C interface. Changes to the style (LVDS or LVPECL) and state (active or high impedance) of each individual output can also be controlled with the I²C interface after power up.

Serial Interface Configuration Description

The IDT8T49N004I has an I²C-compatible configuration interface to access any of the internal registers for frequency and PLL parameter programming. The IDT8T49N004I acts as a slave device on the I²C bus and has the address 0b1101110. The interface accepts byte-oriented block write and block read operations.

For full electrical I²C compliance, it is recommended to use external pull-up resistors for SDATA and SCLK. The internal pull-up resistors have a size of 50k Ω typical.

32 Lead VFQFN Package Outline and Dimensions



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