



3-Lane 3-Port PCI Express® Switch

89HPES3T3 Product Brief

Device Overview

The 89HPES3T3 is a member of IDT's PRECISE™ family of PCI Express switching solutions. The PES3T3 is a 3-lane, 3-port peripheral chip that performs PCI Express Base switching. It provides connectivity and switching functions between a PCI Express upstream port and up to two downstream ports and supports switching between downstream ports.

Features

- ◆ **High Performance PCI Express Switch**
 - Three 2.5Gbps PCI Express lanes
 - Three switch ports
 - x1 Upstream port
 - Two x1 Downstream ports
 - Low latency cut-through switch architecture
 - Support for Max payload sizes up to 256 bytes
 - One virtual channel
 - Eight traffic classes
 - PCI Express Base Specification Revision 1.1 compliant
- ◆ **Flexible Architecture with Numerous Configuration Options**
 - Automatic lane reversal on all ports
 - Automatic polarity inversion on all lanes
 - Ability to load device configuration from serial EEPROM
- ◆ **Legacy Support**
 - PCI compatible INTx emulation
 - Bus locking

- ◆ **Highly Integrated Solution**
 - Requires no external components
 - Incorporates on-chip internal memory for packet buffering and queuing
 - Integrates three 2.5 Gbps embedded SerDes with 8B/10B encoder/decoder (no separate transceivers needed)
- ◆ **Reliability, Availability, and Serviceability (RAS) Features**
 - Internal end-to-end parity protection on all TLPs ensures data integrity even in systems that do not implement end-to-end CRC (ECRC)
 - Supports ECRC and Advanced Error Reporting
 - Supports PCI Express Native Hot-Plug, Hot-Swap capable I/O
 - Compatible with Hot-Plug I/O expanders used on PC motherboards
- ◆ **Power Management**
 - Utilizes advanced low-power design techniques to achieve low typical power consumption
 - Supports PCI Power Management Interface specification (PCI-PM 1.2)
 - Unused SerDes are disabled.
 - Supports Advanced Configuration and Power Interface Specification, Revision 2.0 (ACPI) supporting active link state
- ◆ **Testability and Debug Features**
 - Built in Pseudo-Random Bit Stream (PRBS) generator
 - Numerous SerDes test modes
 - Ability to bypass link training and force any link into any mode
 - Provides statistics and performance counters

Block Diagram

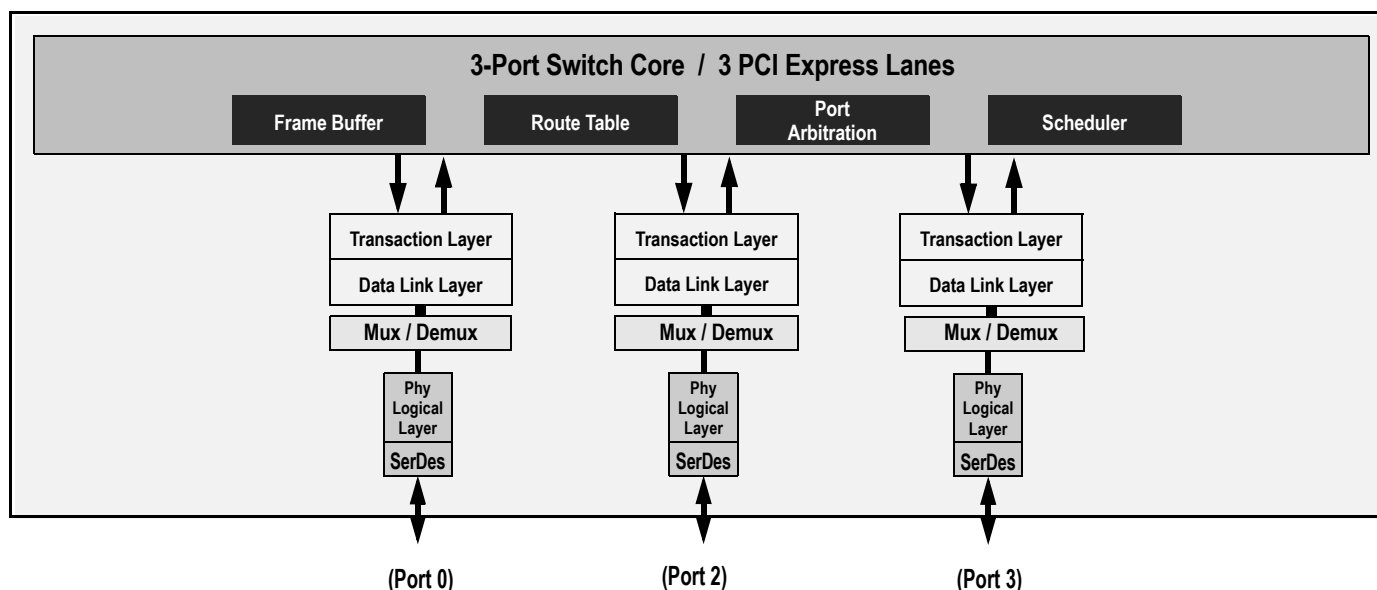


Figure 1 Internal Block Diagram

- ◆ **Five General Purpose Input/Output Pins**
 - Each pin may be individually configured as an input or output
 - Each pin may be individually configured as an interrupt input
 - Four pins have selectable alternate functions
- ◆ **Option A Package: 13mm x 13mm 144-ball BGA with 1mm ball spacing**
- ◆ **Option B Package: 10mm x 10mm 132-ball QFN with 1mm ball spacing**

Product Description

Utilizing standard PCI Express interconnect, the PES3T3 provides the most efficient fan-out solution for applications requiring x1 connectivity, low latency, and simple board layout with a minimum number of board layers. Each lane provides 2.5 Gbps of bandwidth in both directions and is fully compliant with PCI Express Base specification 1.1.

The PES3T3 is based on a flexible and efficient layered architecture. The PCI Express layer consists of SerDes, Physical, Data Link and Transaction layers in compliance with PCI Express Base specification Revision 1.1. The PES3T3 can operate either as a store and forward or cut-through switch and is designed to switch memory and I/O transactions. It supports eight Traffic Classes (TCs) and one Virtual Channel (VC) with sophisticated resource management to allow efficient switching for applications requiring additional narrow port connectivity and also some high-end connectivity.

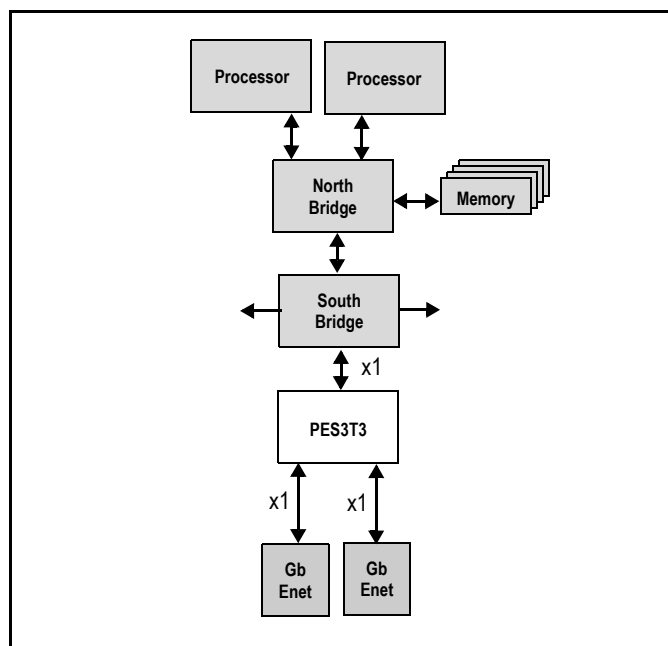


Figure 2 I/O Expansion Application

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