24-Lane 6-Port Gen 2 PCI Express® Switch

89HPES24T6G2
Product Brief

Device Overview

The 89HPES24T6G2 is a member of IDT's PRECISE™ family of PCI Express® switching solutions. The PES24T6G2 is a 24-lane, 6-port Gen2 peripheral chip that performs PCI Express base switching with a feature set optimized for high performance applications such as servers, storage, and communications systems. It provides connectivity and switching functions between a PCI Express upstream port and up to five downstream ports and supports switching between downstream ports.

Features

- High Performance PCI Express Switch
  - *Twenty-four 5 Gbps Gen2 PCI Express lanes supporting 5 Gbps and 2.5 Gbps operation*
  - *Up to six switch ports*
  - *Support for Max Payload Size up to 2048 bytes*
  - *Supports one virtual channel and eight traffic classes*
  - *Fully compliant with PCI Express base specification Revision 2.0*
- Flexible Architecture with Numerous Configuration Options
  - *Automatic per port link width negotiation to x8, x4, x2, or x1*
  - *Automatic lane reversal on all ports*
  - *Automatic polarity inversion*
  - *Supports in-band hot-plug presence detect capability*
  - *Supports external signal for hot plug event notification allowing SCI/SMI generation for legacy operating systems*
  - *Dynamic link width reconfiguration for power/performance optimization*
  - *Configurable downstream port PCI-to-PCI bridge device numbering*
  - *Crosslink support*
  - *Supports ARI forwarding defined in the Alternative Routing-ID Interpretation (ARI) ECN for virtualized and non-virtualized environments*
  - *Ability to load device configuration from serial EEPROM*
- Legacy Support
  - *PCI compatible INTx emulation*
  - *Supports bus locked transactions, allowing use of PCI Express with legacy software*
- Highly Integrated Solution
  - *Requires no external components*
  - *Incorporates on-chip internal memory for packet buffering and queueing*
  - *Integrates twenty-four 5 Gbps / 2.5 Gbps embedded SerDes, 8B/10B encoder/decoder (no separate transceivers needed)*
- Reliability, Availability, and Serviceability (RAS) Features
  - *Ability to disable peer-to-peer communications*
  - *Supports ECRC and Advanced Error Reporting*
  - *All internal data and control RAMs are SECDED ECC protected*
  - *Supports PCI Express hot-plug on all downstream ports*
  - *Supports upstream port hot-plug*

Block Diagram

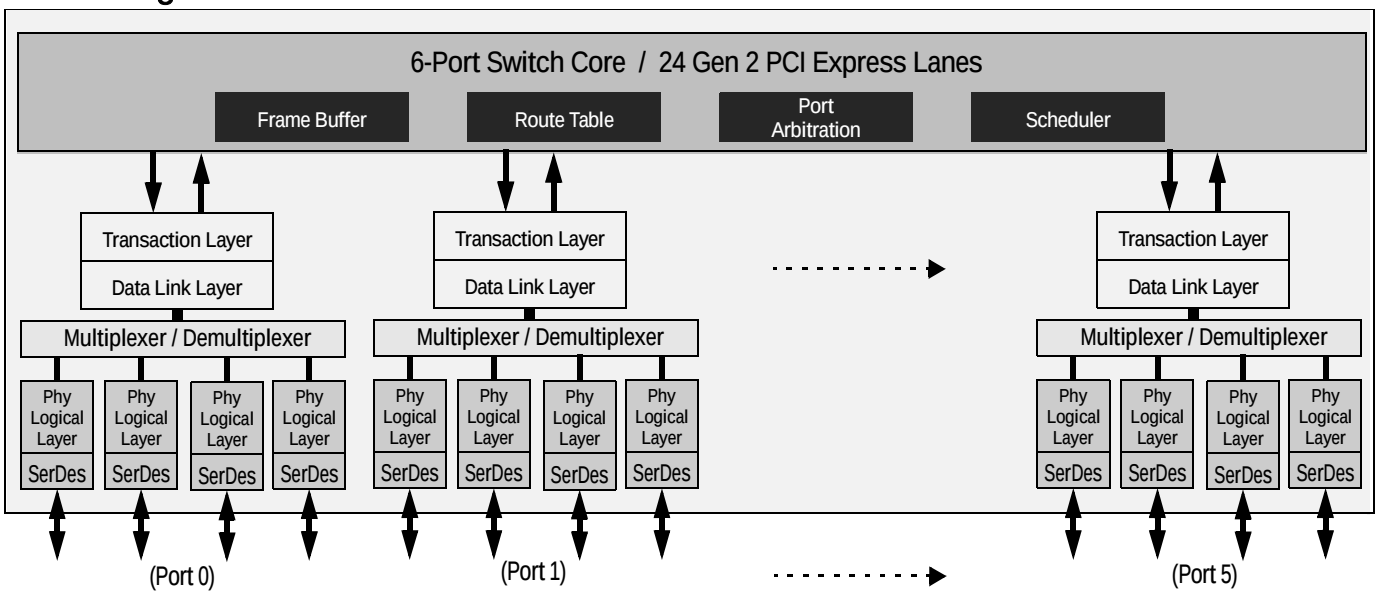

Figure 1 Internal Block Diagram

- *Hot-swap capable I/O*
- *External Serial EEPROM contents are checksum protected*
- *Supports PCI Express Device Serial Number Capability*
- *Capability to monitor link reliability and autonomously change link speed to prevent link instability*

◆ Power Management

- *Utilizes advanced low-power design techniques to achieve low typical power consumption*
- *Support PCI Power Management Interface specification (PCI-PM 1.1)*
  - *Supports device power management states: D0, $D3_{hot}$ and $D3_{cold}$*
- *Support for PCI Express Active State Power Management (ASPM) link state*
  - *Supports link power management states: L0, L0s, L1, L2/L3 Ready and L3*
- *Supports PCI Express Power Budgeting Capability*
- *Configurable SerDes power consumption*
  - *Supports optional PCI-Express SerDes Transmit Low-Swing Voltage Mode*
  - *Supports numerous SerDes Transmit Voltage Margin settings*
- *Unused SerDes are disabled*

◆ Testability and Debug Features

- *Per port link up and activity status outputs available on I/O expander outputs*
- *Built in SerDes 8-bit and 10-bit pseudo-random bit stream (PRBS) generators*
- *Numerous SerDes test modes, including a PRBS Master Loopback mode for in-system link testing*
- *Ability to read and write any internal register via SMBus and JTAG interfaces, including SerDes internal controls*
- *Per port statistics and performance counters, as well as proprietary link status registers*

◆ Eleven General Purpose Input/Output Pins

- *Each pin may be individually configured as an input or output*
- *Each pin may be individually configured as an interrupt input*
- *Some pins have selectable alternate functions*

◆ Option A Package: 19mm x 19mm 324-ball Flip Chip BGA with 1mm ball spacing

◆ Option B Package: 27mm x 27mm 676-ball Flip Chip BGA with 1mm ball spacing

Product Description

Utilizing standard PCI Express interconnect, the PES24T6G2 provides the most efficient I/O connectivity solution for applications requiring high throughput, low latency, and simple board layout with a minimum number of board layers. It provides connectivity for up to 6 ports across 24 integrated serial lanes. Each lane provides 5 Gbps of bandwidth in both directions and is fully compliant with PCI Express Base Specification, Revision 2.0, including operation in 5 Gbps, 2.5 Gbps, and mixed 5 Gbps / 2.5Gbps modes.

The PES24T6G2 is based on a flexible and efficient layered architecture. The PCI Express layer consists of SerDes, Physical, Data Link and Transaction layers in compliance with PCI Express Base specification Revision 2.0. The PES24T6G2 can operate either as a store and forward or cut-through switch and is designed to switch memory and I/O transactions. It supports eight Traffic Classes (TCs) and one Virtual Channel (VC) with sophisticated resource management to enable efficient switching and I/O connectivity for servers, storage, and embedded processors with limited connectivity.

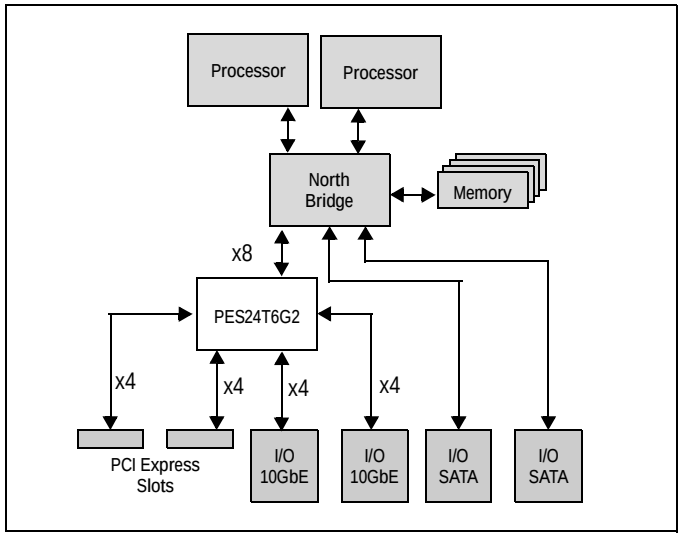

Figure 2 I/O Expansion Application

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