12-Lane 3-Port Non-Transparent PCI Express® Switch

89HPES12NT3
Product Brief

Device Overview

The 89HPES12NT3 is a member of the IDT PRECISE™ family of PCI Express® switching solutions offering the next-generation I/O interconnect standard. The PES12NT3 is a 12-lane, 3-port peripheral chip that performs PCI Express Base switching with a feature set optimized for high performance applications such as servers, storage, and communications/networking. It provides high-performance I/O connectivity and switching functions between a PCIe® upstream port, a transparent downstream port, and a non-transparent downstream port.

With non-transparent bridging (NTB) functionality, the PES12NT3 can be used standalone or as a chipset with IDT PCIe System Interconnect Switches in multi-host and intelligent I/O applications such as communications, storage, and blade servers where inter-domain communication is required.

Features

- High Performance PCI Express Switch
  - Twelve PCI Express lanes (2.5Gbps), three switch ports
  - Delivers 48 Gbps (6 GBps) of aggregate switching capacity
  - Low latency cut-through switch architecture
  - Support for Max Payload size up to 2048 bytes
  - Supports one virtual channel and eight traffic classes
  - PCI Express Base specification Revision 1.0a compliant
- Flexible Architecture with Numerous Configuration Options
  - Port arbitration schemes utilizing round robin
  - Supports automatic per port link width negotiation (x4, x2, or x1)
  - Static lane reversal on all ports
  - Automatic polarity inversion on all lanes
  - Supports locked transactions, allowing use with legacy software
  - Ability to load device configuration from serial EEPROM
  - Ability to control device via SMBus
- Non-Transparent Port
  - Crosslink support on NTB port
  - Four mapping windows supported
    - Each may be configured as a 32-bit memory or I/O window
    - May be paired to form a 64-bit memory window
  - Interprocessor communication
    - Thirty-two inbound and outbound doorbells
    - Four inbound and outbound message registers
    - Two shared scratchpad registers
  - Allows up to sixteen masters to communicate through the non-transparent port
  - No limit on the number of supported outstanding transactions through the non-transparent bridge
  - Completely symmetric non-transparent bridge operation allows similar/same configuration software to be run
  - Supports direct connection to a transparent or non-transparent port of another switch

Block Diagram

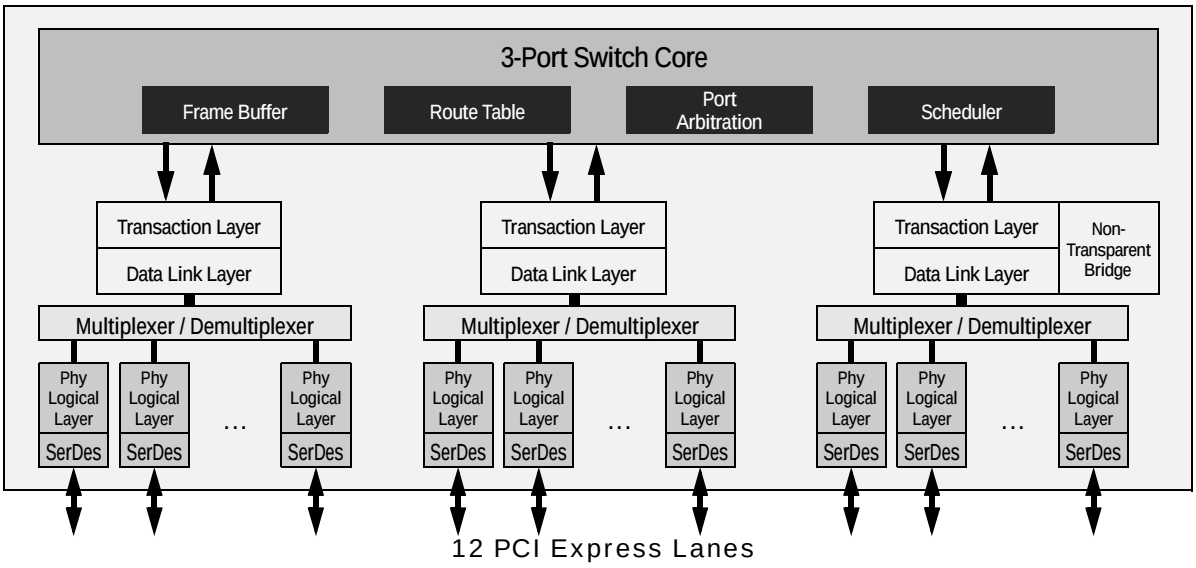

Figure 1 Internal Block Diagram

- Highly Integrated Solution
  - Requires no external components
  - Incorporates on-chip internal memory for packet buffering and queueing
  - Integrates twelve 2.5 Gbps embedded full duplex SerDes, 8B/10B encoder/decoder (no separate transceivers needed)
- Reliability, Availability, and Serviceability (RAS) Features
  - Upstream port can be dynamically swapped with non-transparent downstream port to support failover applications
  - Internal end-to-end parity protection on all TLPs ensures data integrity even in systems that do not implement end-to-end CRC (ECRC)
  - Supports ECRC pass-through in transparent and non-transparent ports
  - Supports Hot-Swap
- Power Management
  - Supports PCI Power Management Interface specification, Revision 1.1 (PCI-PM)
  - Unused SerDes are disabled
- Testability and Debug Features
  - Built in SerDes Pseudo-Random Bit Stream (PRBS) generator
  - Ability to read and write any internal register via the SMBus
  - Ability to bypass link training and force any link into any mode
  - Provides statistics and performance counters
- Two SMBus Interfaces
  - Slave interface provides full access to all software-visible registers by an external SMBus master
  - Master interface provides connection for an optional serial EEPROM used for initialization
  - Master interface is also used by an external Hot-Plug I/O expander
  - Master and slave interfaces may be tied together so the switch can act as both master and slave
- Eight General Purpose Input/Output pins
- Packaged in 19x19mm 324-ball BGA with 1mm ball spacing

Product Description

Utilizing standard PCI Express interconnect, the PES12NT3 provides the most efficient high-performance I/O connectivity solution for applications requiring high throughput, low latency, and simple board layout with a minimum number of board layers. With support for non-transparent bridging, the PES12NT3, as a standalone switch or as a chipset with IDT PCIe System Interconnect Switches, enables multi-host and intelligent I/O applications requiring inter-domain communication. The PES12NT3 provides 48 Gbps (6 GBps) of aggregated, full-duplex switching capacity through 12 integrated serial lanes, using proven and robust IDT technology. Each lane provides 2.5 Gbps of bandwidth in both directions and is fully compliant with PCI Express Base specification 1.0a.

The PES12NT3 is based on a flexible and efficient layered architecture. The PCI Express layer consists of SerDes, Physical, Data Link and Transaction layers in compliance with PCI Express Base specification Revision 1.0a. The PES12NT3 can operate either as a store and forward or cut-through switch depending on the packet size and is designed to switch memory and I/O transactions. It supports eight Traffic Classes (TCs) and one Virtual Channel (VC) with sophisticated resource management. This includes round robin port arbitration, guaranteeing bandwidth allocation and/or latency for critical traffic classes in applications such as high throughput 10 GbE I/Os, SATA controllers, and Fibre Channel HBAs.

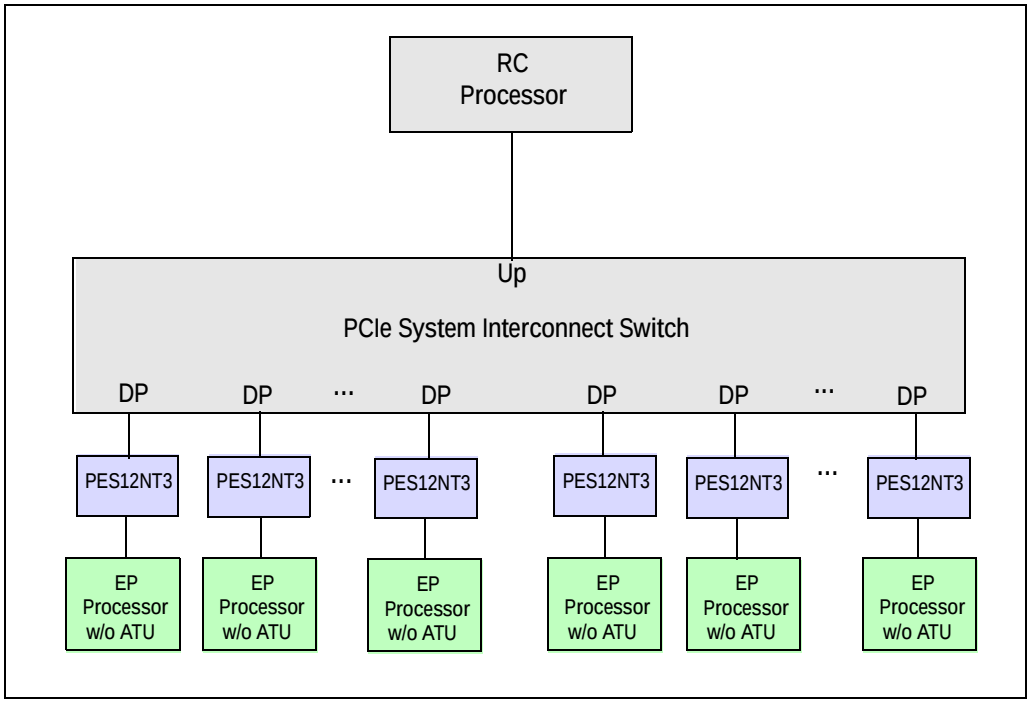

Figure 2 Embedded Compute Application - Processors With and Without Address Translation Unit (ATU) Functionality

CORPORATE HEADQUARTERS
6024 Silver Creek Valley Road
San Jose, CA 95138

for SALES:
800-345-7015 or 408-284-8200
fax: 408-284-2775
www.idt.com

for Tech Support:
email: ssdhelp@idt.com
phone: 408-284-8208