32 Channel PCIe® Signal Retimer for 8.0Gbps, 5.0Gbps, and 2.5Gbps

89HT0832P
Product Brief

Device Overview

The 89HT0832P (T0832P) is a Signal Retimer/Conditioner used to improve signal integrity for enhancing system performance and reliability across long PCB traces or cables. It removes both random and deterministic jitter from the input signal eliminating inter-symbol interference, and resets the output jitter budget. It provides 32 differential, 8GT/s PCIe Express® 3.0 channels, supporting up to 16 full lanes. The Retimer also fully supports PCIe Express 5GT/s and 2.5GT/s features. The T0832P is targeted to meet the high-performance needs of PCIe® Gen 3/2/1 applications.

Applications

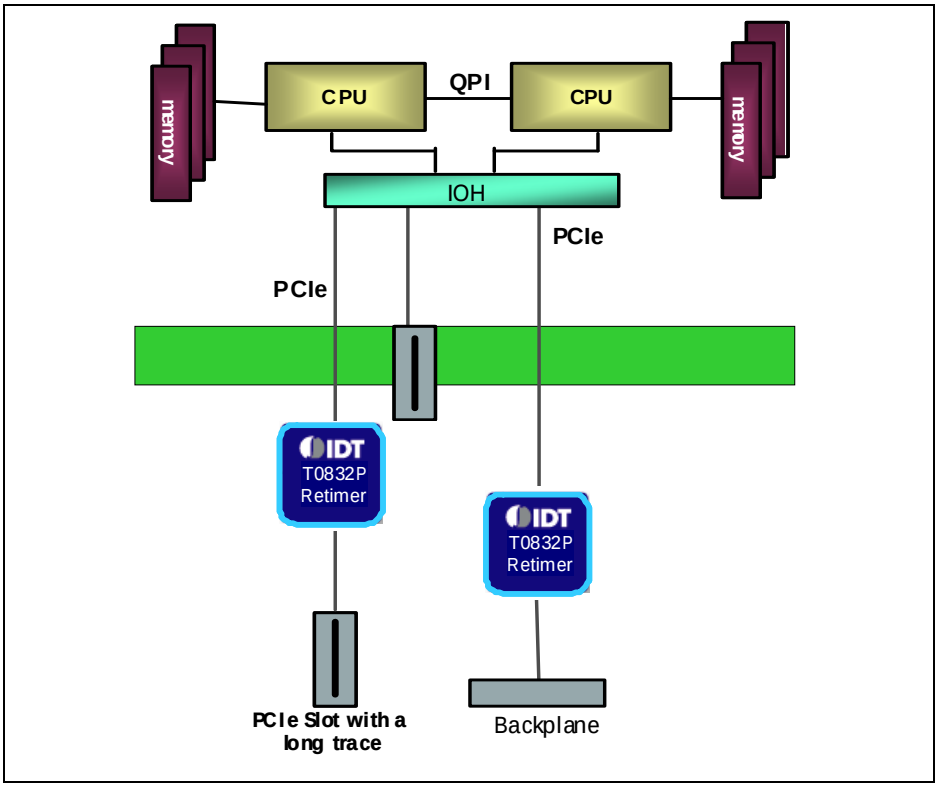
- Computing and Storage
- Communications

Features

- **High Performance 8GT/s Retimer**
  - Fully complies with new PCIe 3.0 Link Equalization Procedure (including Phase 2 and 3)
  - Eliminates input Random Jitter (Rj), Deterministic Jitter (Dj) and ISI
  - Receiver equalizer: CTLE plus 5-tap DFE
  - Compensates for non-linear PCB trace and cable loss to 40 inches of FR4
  - 4-tap TX FIR filter implements boost, preshoot, and deemphasis fully compliant with PCIe specification
  - Wide swing transmit driver offers up to 8dB of transmit deemphasis to meet the needs of the most challenging of backplanes
  - Fast acquisition PLL for L0s exit
- **PCIe Standards and Compatibility**
  - PCI Express Base Specification 3.0 compliant
  - PCI Express Base Specification 2.1 compliant
- **Power Management**
  - Low power
  - Supports the following optional PCI Express features
    - L0s ASPM
    - L1 ASPM
- **Hot Plug Support**
- **SerDes Power Savings**
  - Supports low swing (half-swing as low as 0.4V) SerDes operation
  - SerDes associated with unused lanes are placed in a low power state automatically
- **Link Configurability**
  - Links can be configured as 1x16, 2x8, or 4x4 (1, 2 or 4 independent links)
  - Automatic per port link width negotiation (e.g., a x16 port can link train to x16, x8, x4, or x1 active lanes)
  - Per-channel SerDes configuration
- **Clocking**
  - Uses standard 100 MHz PCIe reference clock
  - SSCLK (Spread Spectrum Clocking) supported with common clock configuration
    - Non-SSCLK supported with common and non-common clock configuration
- **I^2C Interface**
  - Dedicated master interface
    - External EEPROM configuration loading
  - Dedicated slave interface
    - Configuration loading
    - Writing new or initial image into external EEPROM
    - Expose internal global CSR space to system controller
- **Reliability, Availability and Serviceability (RAS)**
  - Physical layer error checking and accounting
  - End-to-end data path parity protection
  - Checksum Serial EEPROM content protected
- **Extensive Test and Debug Features**
  - SERDES Rx eye generation (on-chip)
  - Pattern generator/checker
- **Packaged in a 20x13mm, 345-ball CABGA, 0.8mm spacing**

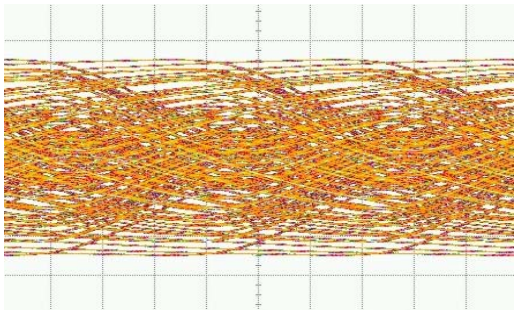
Applications

IDT's Retimer products fit into server, storage, and blade products.

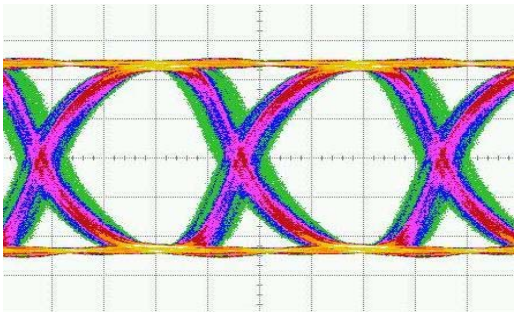


Improving Signal Integrity with IDT Retimers

No Retimer



With IDT Retimer



Example Eye diagram FR4 and PRBS patterns

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