89HT0816AP PCIe 3.0 Signal Retimer

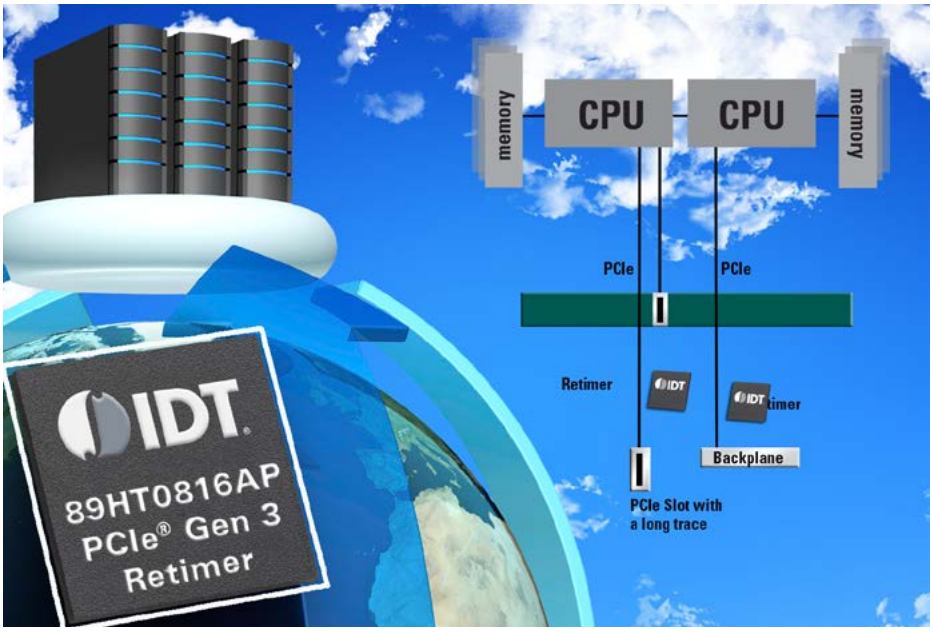
16 Channel Signal Retimers for 8.0 Gbps, 5.0 Gbps and 2.5 Gbps PCIe®

Integrated Device Technology

CLOCKS AND TIMING | **INTERFACE AND CONNECTIVITY** | MEMORY AND LOGIC | POWER MANAGEMENT | RF PRODUCTS

FEATURES

- **High Performance Retimer**
  - Fully complies with PCIe 3.0 link equalization procedure
  - Eliminates random input jitter (R_J)
  - Eliminates deterministic ISI jitter (D_J)
  - Compensates for PCB trace and cable attenuations
  - Adjustable operation for each data rate
  - Wide swing, transmit driver with 4-tap TX FIR filter implements boose, preshoot and deemphasis fully compliant with PCIe 3.0 standard
  - Multi-stage equalizer: CTLE and 5 tap DFE
- **PCIe Standards and Compatibility**
  - PCI Express Base Specification 3.0 compliant
  - PCI Express Base Specification 2.1 compliant
- **Power Management**
  - Low power modes
  - Supports the following optional PCI Express features
    - L0s ASPM and L1 ASPM
- **Hot Plug Support**
- **SerDes Power Savings**
  - Supports low swing (half-swing) SerDes operation
  - SerDes associated with unused lanes are placed in a low power state automatically
- **Link Configurability**
  - Links can be configured with 1x8 or 2x4
  - Automatic per port link width negotiation (e.g., a x8 port can link train to x8, x4, or x1)
  - Per-lane SerDes configuration
- **Clocking**
  - Uses standard 100 MHz PCIe reference clock
  - SSCLK (Spread Spectrum Clocking) supported with common clock configuration
  - Non-SSCLK supported with common and non-common clock configuration
- **I²C and JTAG Interface**
  - Dedicated master interface
    - External EEPROM configuration loading
  - Dedicated slave interface
    - Configuration loading
    - Writing new or initial image into external EEPROM
    - Expose internal CSR space to system controller
- **Reliability, Availability and Serviceability (RAS)**
  - Physical layer error checking and accounting
  - End-to-end data path parity protection
  - Checksum Serial EEPROM content protected
- **Test and Debug**
  - All registers accessible from I²C or JTAG port
  - Per link/lane error diagnostic registers
  - Supports IEEE 1149.6 AC JTAG and IEEE 1149.1 JTAG
  - Several loopback modes
  - SERDES Rx eye generation on-chip pattern generator/checker
- Packaged in a 15x15 mm, 196-pin FCBGA with EMI seal 1 mm ball spacing



General Description

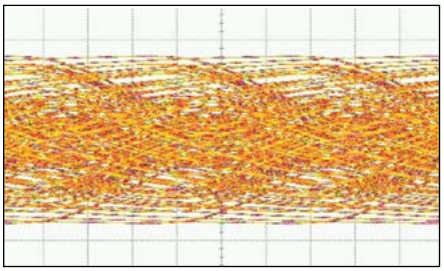
The 89H0816AP is a Signal Retimer/Conditioners used to improve signal integrity for enhancing system performance and reliability across long PCB traces or cables. It removes both random and deterministic jitter from the input signal eliminating inter-symbol interference, and resets the output jitter budget. It provides sixteen differential, 8Gbps PCIe Express® 3.0 channels, supporting up to 8 full lanes. It also fully support PCIe Express 5Gbps and 2.5Gbps features. The 89HT0816AP is targeted to meet the high-performance needs of PCIe® Gen 3/2/1 applications.

Applications

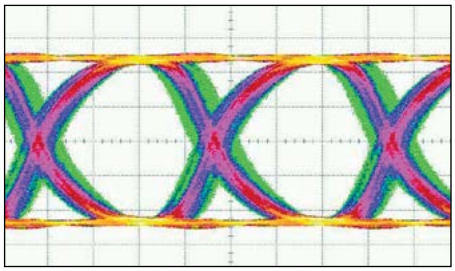
IDT's PCIe 3.0 Retimer products fit into server, storage, and blade products, as well as consumer electronics and communications applications.

Improving Signal Integrity with IDT Retimers

No Retimer



With IDT Retimer



Example Eye diagram FR4 and PRBS patterns

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