

Integrated Device Technology, Inc. 6024 Silver Creek Valley Road, San Jose, CA - 95138

PCN #: W1911-01	DATE:	19-Dec-2019	MEANS OF DIS	TINGUISHING CHANGED DEVICES:		
Product Affected: F1431NBGK	x, F1431NBGK8		□ Product Mark □ Back Mark ■ Date Code □ Other	Datecode 2018 and above		
Date Effective: 19-Mar-2020						
Contact: PCN DESK			Attachment:	Yes No		
E-mail: <u>idt-pcn@lm.ren</u>	esas.com		Samples: N/A			
DESCRIPTION AND PURPOSE	OF CHANGE:					
 □ Die Technology ■ Wafer Fabrication Process □ Assembly Process □ Equipment □ Material □ Testing 		This notification is to advise our customers that the MIM capacitor architecture has been re-designed by the foundry WaveTek to improve device robustness. This change is to address the CGR (Capacitive Guard Ring) MIMCAP design that is susceptible to peeling of nitride layer between metal layers.				
☐ Manufacturing Site			Current	New		
☐ Data Sheet☐ Other	MIMCAP Architecture		CGR	TPM		
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Product Qualification Report (Re-Spin)

Date: 11/19/2019

Product: F1431ZJNBGK

Fab Base: GRF2014B C2018 Process Technology: ED25_5V GaAs E/D-HEMT

Package Type:NBG24Fab Location:WaveTek

Assembly Location: Carsem Qual Plan#: Q19-11-005

Test Description	Conditions	Sample Size	Results (rej/SS)	Comments
Early Life Failure Rate	JESD22-A108, Ta 97°C, 5.0V, 48 hrs	320	0/320	Pass
ESD: Human Body Model	JESD22-A114 (JS-001) Classification ±2000V	3	0/3	Pass
ESD: Charged Device Model	JESD22-C101 Classification ±500V	3	0/3	Pass
Latch-Up	JESD78, T _A at 85°C	6	0/6	Pass
Electrical Characterization	Datasheet	3	Results reported in Datasheet	Complete

Package Qual							
Temperature Cycling ¹	JESD22-A104, -55°C to +125°C, 700 cycles	25	0/25, x3 lots	Pass			
Highly Accelerated Temperature and Humidity stress (Biased) ¹	JESD22-A110, +130°C, 85% RH, Vcc _{max} , 96 hrs	25	0/25, x3 lots	Pass			
High Temperature Storage Life ¹	JESD22-A103, +150°C, 1000 hrs	25	0/25, x3 lots	Pass			
Bond Pull Strength	M2011	5	0/5, x3 lots	Pass			
Bond Shear	JESD22-B116	5	0/5, x3 lots	Pass			
Physical Dimension	JESD22-B100 (Per applicable IDT Package Outline Drawing)	30	0/30, x3 lots	Pass			
Solderability Test	MIL-STD-883 (Method 2003), J-STD-002D	5	0/5, x3 lots	Pass			

Note:

1. Preconditioning per JESD22-A113, MSL 1 (260°C)