Integrated Device Technology, Inc.
2975 Stender Way, Santa Clara, CA - 95054

PRODUCT/PROCESS CHANGE NOTICE (PCN)

PCN #: SR0003-02 DATE: 5/3/00
Product Affected: 71V016S, 71V124S, 71V016SA, 71V124SA

Manufacturing Location Affected: N/A
Date Effective: 8/3/00

MEANS OF DISTINGUISHING CHANGED DEVICES:
- ☒ Product Mark "H" character on top mark
- ☐ Back Mark
- ☐ Date Code
- ☐ Other

Contact: Mary Vesey
Title: Director of Quality
Phone #: (831)-754-4565
Fax #: (831)-754-4672
E-mail: Mary.vesey@idt.com

Attachment:: ☒ Yes ☐ No

Samples: Available on request

DESCRIPTION AND PURPOSE OF CHANGE:
- ☒ Die Technology
- ☐ Wafer Fabrication Process
- ☐ Assembly Process
- ☐ Equipment
- ☐ Material
- ☐ Testing
- ☐ Manufacturing Site
- ☐ Data Sheet
- ☐ Other

Die Shrink : From "K" Die revision to "H".

RELIABILITY/QUALIFICATION SUMMARY:
Qualification is expected to be completed 6/15/00 and will be available upon request.

CUSTOMER ACKNOWLEDGMENT OF RECEIPT:
IDT records indicate that you require written notification of this change. Please use the acknowledgement below or E-Mail to grant approval or request additional information. If IDT does not receive acknowledgement within 30 days of this notice it will be assumed that this change is acceptable.
IDT reserves the right to ship either version manufactured after the process change effective date until the inventory on the earlier version has been depleted.

Customer: ______________________

☐ ***Approval for shipments prior to effective date.***

Name/Date: ______________________

E-Mail Address: ______________________

Title: ______________________

Phone# /Fax# : ______________________

CUSTOMER COMMENTS: ______________________

IDT ACKNOWLEDGMENT OF RECEIPT:

RECD. BY: ______________________ DATE: ______________________

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PCN Summary

PCN Type:	Mask/Design Change for Die Shrink
Commodity	Memory
Forecast or Execute	Execute
Planned or Unplanned	Planned
Data Sheet Change	No

Detail of Change

Die Revision	K Step	H Step
Wafer Fab Facility	Hillsboro, OR	Hillsboro, OR
Wafer Fab Technology	Cmos 11.5	Cmos 11.5
Wafer Size	8 inch	8 inch
Cell Type	6T	6T
# Poly Layers	1	1
# Metal Layers	3	3
Die Dimension (sq mils)	28.3k	15.3k

Conversion schedule (Estimated)

	Sample Availability	**Production Shipments**
71V016S	6/1/00	7/24/00
71V124S	6/1/00	7/24/00
71V016SA	6/15/00	7/24/00
71V124SA	6/15/00	7/24/00

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Qualification Plan **QS 9811-12**

Test Vehicle: **71V016S** **Expected Completion Date:**

		6/15/00	7/15/00
	Lot SS / Acc #	Lot # 1	Lot # 2
Dynamic Life Test: 750 hours @ +135°C, 4Vcc	116 / 0		
High Temp Storage Test: 1000 hours @ +150°C	77 / 0		
Temperature Cycle: -65°C to +150°C, 1000	45 / 0		
HAST: 100 hours @ +130°C/85% R.H. 100	45 / 0		
Autoclave: Unbiased 2 ATM Saturated Steam @	45 / 0		
ESD: Human Body Model	12 / 0		
ESD: Charged Device Model	12 / 0		
Latch-Up Immunity	6 / 0		
Bake & Ballshear Test: +200°C - 48 hour	20 / 0		

Characterization Data: Characterization will be completed as part of product qualification and data available upon request.