Integrated Device Technology, Inc.
2975 Stender Way, Santa Clara, CA - 95054

PRODUCT/PROCESS CHANGE NOTICE (PCN)

PCN #: SM 0008-04 DATE: 8/21/00
Product Affected: 256K & 512K Dual Port Family
(refer to attached list for product details)
Manufacturing Location Affected: N/A
Date Effective: 11/20/00

MEANS OF DISTINGUISHING CHANGED DEVICES:
■ Product Mark Die Revision "X" on Top Mark
☐ Back Mark
☐ Date Code
☐ Other

Contact: Lakshmi Srinivasan
Title: Quality Engineering Supervisor
Phone #: (831) 775-4022
Fax #: (831) 754-4672
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Attachment:: ■ Yes ☐ No

Samples: Available on request. Please contact you local Sales Representative for schedule

DESCRIPTION AND PURPOSE OF CHANGE:

■ Die Technology
■ Wafer Fabrication Process
☐ Assembly Process
☐ Equipment
☐ Material
☐ Testing
☐ Manufacturing Site
☐ Data Sheet
☐ Other

This change is to upgrade to a new technology (CMOS 9) and shrink die. This change is to improve manufacturabilty and allow for expanded product offerings.

RELIABILITY/QUALIFICATION SUMMARY:

Qualification testing will verify that there is no change to product reliability. Qualification details are available upon request.

CUSTOMER ACKNOWLEDGMENT OF RECEIPT:

IDT records indicate that you require written notification of this change. Please use the acknowledgement below or E-Mail to grant approval or request additional information. If IDT does not receive acknowledgement within 30 days of this notice it will be assumed that this change is acceptable.
IDT reserves the right to ship either version manufactured after the process change effective date until the inventory on the earlier version has been depleted.

Customer: _____ ☐ ***Approval for shipments prior to effective date.***

Name/Date: _____ E-Mail Address: _____

Title: _____ Phone# /Fax# : _____

CUSTOMER COMMENTS: _____

IDT ACKNOWLEDGMENT OF RECEIPT:

RECD. BY: _____ DATE: _____

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PCN Summary
PCN Type: Mask/Design Change for Die Shrink

Commodity Memory

Forecast or Execute Execute

Planned or Unplanned Planned

Data Sheet Change N/A

Detail of Change: The base device for each part is detailed on the attached product detail sheet. The new base device for future products listed on this PCN will be 7027 "X". This product redesign will allow for IDT to expand product offerings and upgrade technology. This change will also provide the flexibility of manufacturing the product in either Wafer Facility.
Both Wafer Fab facilities have been previously qualified for CMOS 9 processing.

	Current Die Revision			Planned Change	
Base Device / Die Revision	7026 Z	7027 Z	7027 Y	7027 X	
Wafer Fab Facility	Salinas, CA	Salinas, CA	Hillsboro, OR	Hillsboro, OR	Salinas, CA
Wafer Fab Technology	CMOS 7	CMOS 8	CMOS 9	CMOS 9	CMOS 9
Wafer Size	6 Inch	6 Inch	8 Inch	8 Inch	6 Inch
# Poly Layers	2	2	3	3	3
# Metal layers	2	2	2	2	2
Minimum Feature Size / µm	0.64	.60 /. 40	0.35	0.35	0.35
Die Dimensions/(K sq mils)	86.2	113.8	132.6	81.3	81.3

Conversion schedule: Contact the local IDT Sales Representative for schedule.

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Qualification Plan

Test Vehicles		Expected Completion Date 11/15/00	12/15/00	11/15/00	12/15/00
70V37X (3.3V) & 7037X (5V)	Required Sample / # Fails	LOT #1 3.3V	LOT #2 3.3V	LOT #1 5V	LOT #2 5V
Operating Life Test: Dynamic @+135°C, Vcc=6V for 500 hours or Vcc=4V for 750 hours	116 / 0				
High Temp. Storage Life Test (Unbiased, 1000 hours @+150°C)	77 / 0				
Bake & Ballshear Test @ 200°C / 4 ball bonds per device	5 / 0				
Thermal Shock: (-65°C to +150°C, 100 cycles)	45 / 0				
Temperature Cycling: (-65°C to +150°C, 1000 cycles)	45 / 0				
HAST: (Biased, 100 Hrs. @+130°C, +85%RH, 3 Atm.)	45 / 0				
Autoclave:(Unbiased, 2 Atm Saturated Steam, +121°C, 168 Hrs)	45 / 0				
ESD Human Body Model	6 / 0				
ESD Charged Device Model	6 / 0				
Latch up: (Tested to 2X Vcc)	10 / 0				

Tests are completed for unshaded areas. Product released is based on qualification of initial lot.

Characterization Data: Characterization is completed as part of qualification and will verfiy that there is no change to the datasheet parameters.

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IDT7026 Family of Parts							
Part Number	Old Rev.	New Rev.	Interface	Vcc	Bus	Depth	Density
IDT7026S/L	'Z'	'X'	Async	5.0	x16	16K	256K
IDT70261S/L	'Z'	'X'	Async	5.0	x16	16K	256K
IDT7007S/L	'Z'	'X'	Async	5.0	x8	32K	256K
IDT70V26S/L	'Z'	'X'	Async	3.3	x16	16K	256K
IDT70V261S/L	'Z'	'X'	Async	3.3	x16	16K	256K
IDT70V07S/L	'Z'	'X'	Async	3.3	x8	32K	256K
IDT709269S/L	'Z'	'X'	Sync	5.0	x16	16K	256K
IDT709079S/L	'Z'	'X'	Sync	5.0	x8	32K	256K
IDT70V9269S/L	'Z'	'X'	Sync	3.3	x16	16K	256K
IDT70V9079S/L	'Z'	'X'	Sync	3.3	x8	32K	256K

IDT7027 Family of Parts							
Part Number	Old Rev.	New Rev.	Interface	Vcc	Bus	Depth	Density
IDT7027S/L	'Z'	'X'	Async	5.0	x16	32K	512K
IDT7008S/L	'Z'	'X'	Async	5.0	x8	64K	512K
IDT70V27S/L	'Z'	'X'	Async	3.3	x16	32K	512K
IDT70V08S/L	'Z'	'X'	Async	3.3	x8	64K	512K
IDT709279S/L	'Z'	'X'	Sync	5.0	x16	32K	512K
IDT709089S/L	'Z'	'X'	Sync	5.0	x8	64K	512K
IDT70V9089S/L	'Z'	'X'	Sync	3.3	x16	32K	512K
IDT70V9279S/L	'Z'	'X'	Sync	3.3	x8	64K	512K
IDT7037L	'Y'	'X'	Async	5.0	x18	32K	576K
IDT7018L	'Y'	'X'	Async	5.0	x9	64K	576K
IDT70V18L	'Y'	'X'	Async	3.3	x9	64K	576K
IDT709379L	'Y'	'X'	Sync	5.0	x18	32K	576K
IDT709189L	'Y'	'X'	Sync	5.0	x9	64K	576K
IDT70V9379L	'Y'	'X'	Sync	3.3	x18	32K	576K
IDT70V9189L	'Y'	'X'	Sync	3.3	x9	64K	576K

New Parts							
Part Number	Old Rev.	New Rev.	Interface	Vcc	Bus	Depth	Density
IDT7036S/L	–	'X'	Async	5.0	x18	16K	288K
IDT7017S/L	–	'X'	Async	5.0	x9	32K	288K
IDT70V36S/L	–	'X'	Async	3.3	x18	16K	288K
IDT70V17S/L	–	'X'	Async	3.3	x9	32K	288K
IDT709369S/L	–	'X'	Sync	5.0	x18	16K	288K
IDT709179S/L	–	'X'	Sync	5.0	x9	32K	288K
IDT70V9369S/L	–	'X'	Sync	3.3	x18	16K	288K
IDT70V9179S/L	–	'X'	Sync	3.3	x9	32K	288K