Integrated Device Technology, Inc.
6024 Silver Creek Valley Road, San Jose, CA 95138

PRODUCT/PROCESS CHANGE NOTICE (PCN)

PCN #: **N1408-01** DATE: **September 9, 2014**

Product Affected: 874208BKILF
874208BKILFT

Date Effective: **September 9, 2014**

MEANS OF DISTINGUISHING CHANGED DEVICES:

- ☐ Product Mark
- ☐ Back Mark
- ☐ Date Code
- ■ Other — Shipment after PCN effective date.

Contact: TSD Clock Team

E-mail: clocks@idt.com

Attachment: ■ Yes ☐ No

Samples: Contact your local sales representative for sample and datasheet requests.

DESCRIPTION AND PURPOSE OF CHANGE:

- ☐ Die Technology
- ☐ Wafer Fabrication Process
- ☐ Assembly Process
- ☐ Equipment
- ☐ Material
- ☐ Testing
- ☐ Manufacturing Site
- ■ Data Sheet
- ☐ Other - Die revision

The Data Sheet parameter for "Input Resistance" and "Differential Input Resistance" are updated, which allow input specification to be TIA/EIA-644-A compliant.

This is an update of the datasheet only, no change of the silicon design, die revision, circuitry, process or device performance.

RELIABILITY/QUALIFICATION SUMMARY:

There is no expected change to the product quality or reliability performance.

CUSTOMER ACKNOWLEDGMENT OF RECEIPT:

IDT records indicate that you require written notification of this change. Please use the acknowledgement below or E-Mail to grant approval or request additional information. If IDT does not receive acknowledgement within 30 days of this notice it will be assumed that this change is acceptable.
IDT reserves the right to ship either version manufactured after the process change effective date until the inventory on the earlier version has been depleted.

Customer: _____ ☐ ***Approval for shipments prior to effective date.***

Name/Date: _____ E-Mail Address: _____

Title: _____ Phone # /Fax #: _____

CUSTOMER COMMENTS: _____

IDT ACKNOWLEDGMENT OF RECEIPT:

RECD. BY: _____ DATE: _____

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ATTACHMENT I - PCN #: N1408-01

PCN Type: Data Sheet Change

Data Sheet Change: Yes

Detail of Change:

From:

Table 4B. LVCMOS/LVTTL Input DC Characteristics, $V_{DD} = V_{DDO} = 2.5V$, $T_A = -40°C$ to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage			1.7		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage			-0.3		0.7	V
I_{IH}	Input High Current	FSEL1, FSEL0, ADR[1:0]	$V_{DD} = V_{IN} = 2.625V$			150	µA
		SCK, SDA	$V_{DD} = V_{IN} = 2.625V$			5	µA
I_{IL}	Input Low Current	FSEL1, FSEL0, ADR[1:0]	$V_{DD} = 2.625V$, $V_{IN} = 0V$	-5			µA
		SCK, SDA	$V_{DD} = 2.625V$, $V_{IN} = 0V$	-150			µA
V_{IN}	Input Voltage Swing	IN, nIN		0.15		1.2	V
V_{CMR}	Common Mode Input Voltage; NOTE 1			1.2		V_{DD}	V
V_{DIFF}	Differential Input Voltage Swing	IN, nIN		0.3		2.4	V
R_{IN}	Input Resistance	IN, nIN to V_T		40	50	60	Ω
$R_{IN, DIFF}$	Differential Input Resistance	IN to nIN, V_T = open		80	100	120	Ω

NOTE 1: Common mode input voltage is defined as V_{IH}.

To:

Table 4B. LVCMOS/LVTTL Input DC Characteristics, $V_{DD} = V_{DDO} = 2.5V$, $T_A = -40°C$ to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage			1.7		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage			-0.3		0.7	V
I_{IH}	Input High Current	FSEL1, FSEL0, ADR[1:0]	$V_{DD} = V_{IN} = 2.625V$			150	µA
		SCK, SDA	$V_{DD} = V_{IN} = 2.625V$			5	µA
I_{IL}	Input Low Current	FSEL1, FSEL0, ADR[1:0]	$V_{DD} = 2.625V$, $V_{IN} = 0V$	-5			µA
		SCK, SDA	$V_{DD} = 2.625V$, $V_{IN} = 0V$	-150			µA
V_{IN}	Input Voltage Swing	IN, nIN		0.15		1.2	V
V_{CMR}	Common Mode Input Voltage; NOTE 1			1.2		V_{DD}	V
V_{DIFF}	Differential Input Voltage Swing	IN, nIN		0.3		2.4	V
R_{IN}	Input Resistance	IN, nIN to V_T		45	50	66	Ω
$R_{IN, DIFF}$	Differential Input Resistance	IN to nIN, V_T = open		90	100	132	Ω

NOTE 1: Common mode input voltage is defined as V_{IH}.