



Integrated Device Technology, Inc.
2975 Stender Way, Santa Clara, CA - 95054

PRODUCT/PROCESS CHANGE NOTICE (PCN)

ATTACHMENT - PCN #: L0108-01R1 (Addendum)

PCN Type: Die revision

Data Sheet Change No

Detail of Change The die has been revised from "YQ" , "ZQ" and "QC" stepping to "Z" stepping

Die Revision Details

	<u>Current Die Rev</u> YQ	<u>Current Die Rev</u> ZQ	<u>Current Die Rev</u> QC	<u>New Die Rev</u> Z
Wafer Fab Technology	0.8µm	0.8µm	0.8µm	0.8µm
Poly Gate	0.8µm	0.8µm	0.8µm	0.8µm
Minimum Gate Oxide Thickness	150Å	150Å	150Å	150Å
Wafer Size	6"	6"	6"	6"
Fab Facility	Fab 5 (PSA, Australia)	Fab 5 (PSA, Australia)	Fab 2 (Salinas, CA)	Fab 2 (Salinas, CA)
Date Code Prefix	YQ	ZQ	QC	Z
Affected Parts	IDTQS3VH125 IDTQS3VH126	IDTQS3VH257 IDTQS3VH2245 IDTQS32XH2245 IDTQS34XVH2245	IDTQS3VH125 IDTQS3VH126 IDTQS3VH257 IDTQS3VH2245 IDTQS32XVH2245 IDTQS34XVH2245	IDTQS3VH125 IDTQS3VH126 IDTQS3VH257 IDTQS3VH2245 IDTQS32XVH2245 IDTQS34XVH2245



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Qualification Plan QLG-01-01

Test Vehicle: IDTQS3VH862

Qualification Test Plan and Results:

Test Description	SS/Acc #	Test Results
Dynamic High Temp Operating Life Test Mil-Std-883, Method-1005	116/0	116/0
ESD - HBM Mil-Std-883, Method-3015	3/0	3500 Volts
ESD-CDM JESD22-C101	3/0	1000 Volts
ESD-MM EIAJ-IC-121	3/0	400 Volts
Latch-up EIA/JESD78	10/0	10/0

Characterization Data:

Characterization data is available upon request.