

KMB001CEVAL Schematics

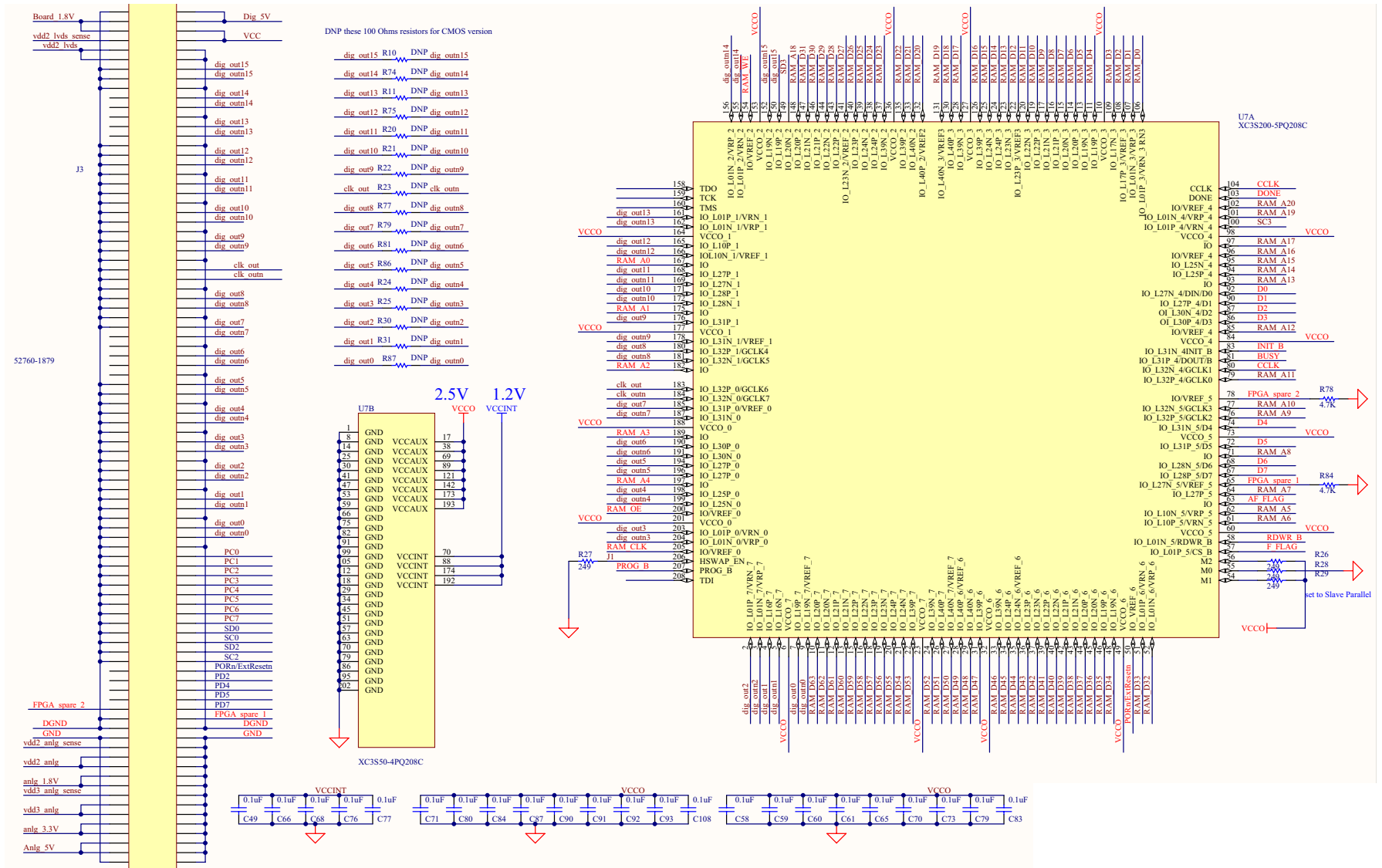


FIGURE 1. FPGA, INPUT/OUTPUT MEZZANINE CONNECTOR

KMB001CEVAL Schematics (Continued)

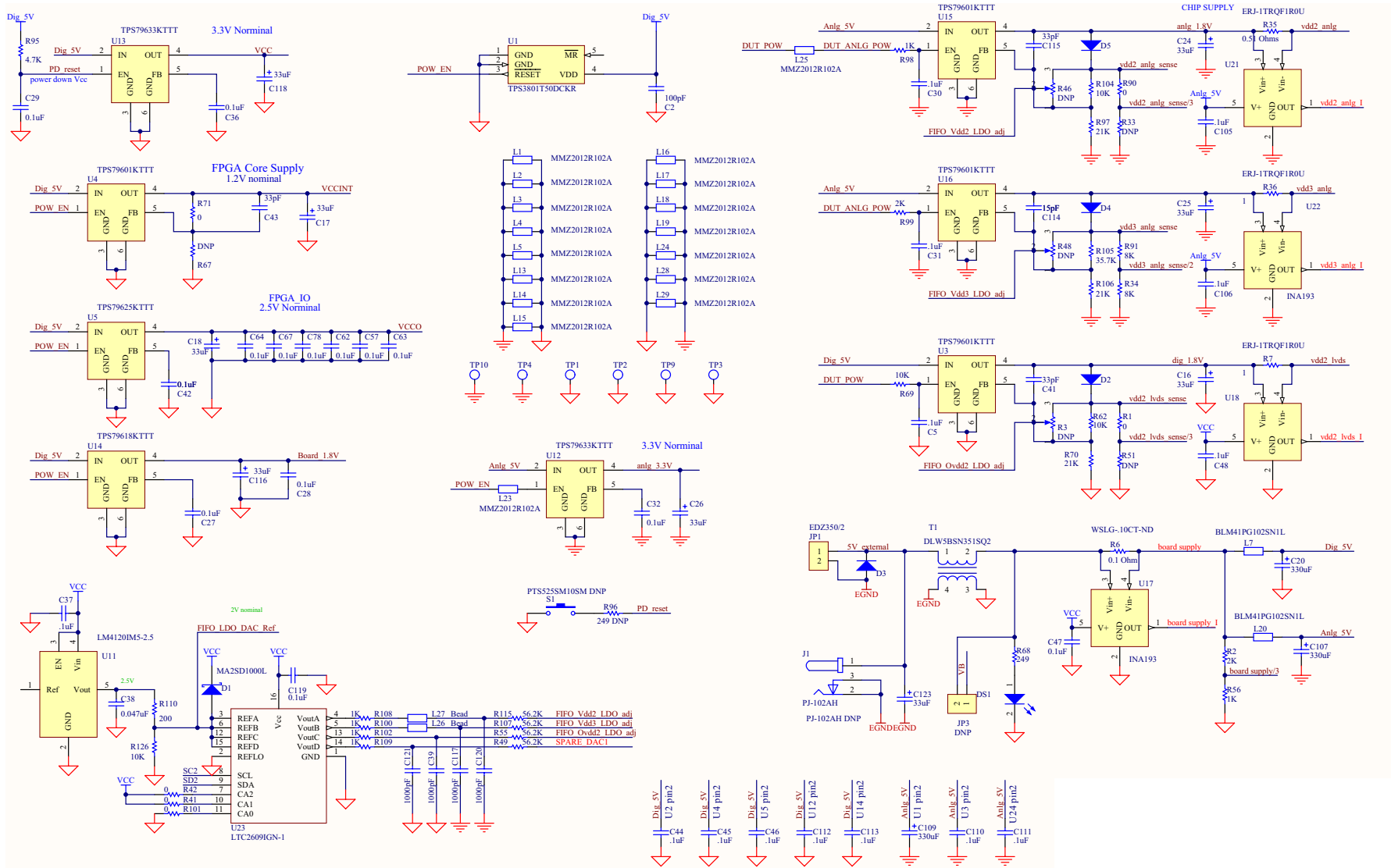


FIGURE 2. POWER

KMB001CEVAL Schematics (Continued)

OGP

Populate these resistors for OGP

FPGA spare 2	R117	DNP	R116	DNP	PC4
FPGA spare 1	R119	DNP	R118	DNP	PC7
RAM A20	R121	DNP	R120	DNP	PC2
RAM A19	R123	DNP	R122	DNP	PC5
RAM A18	R125	DNP	R124	DNP	PC6

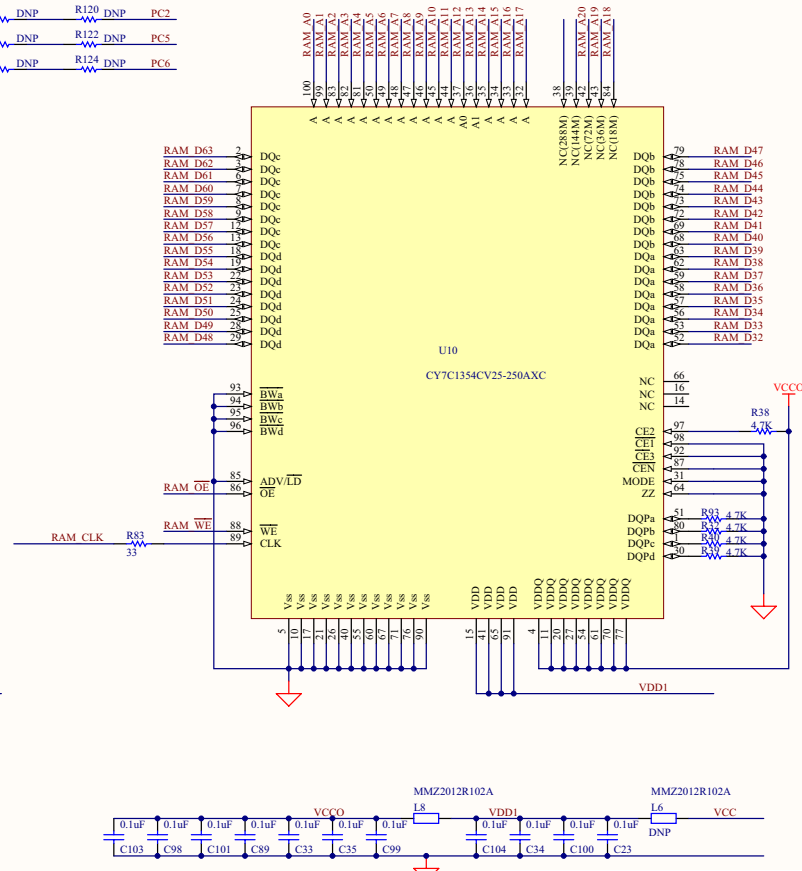
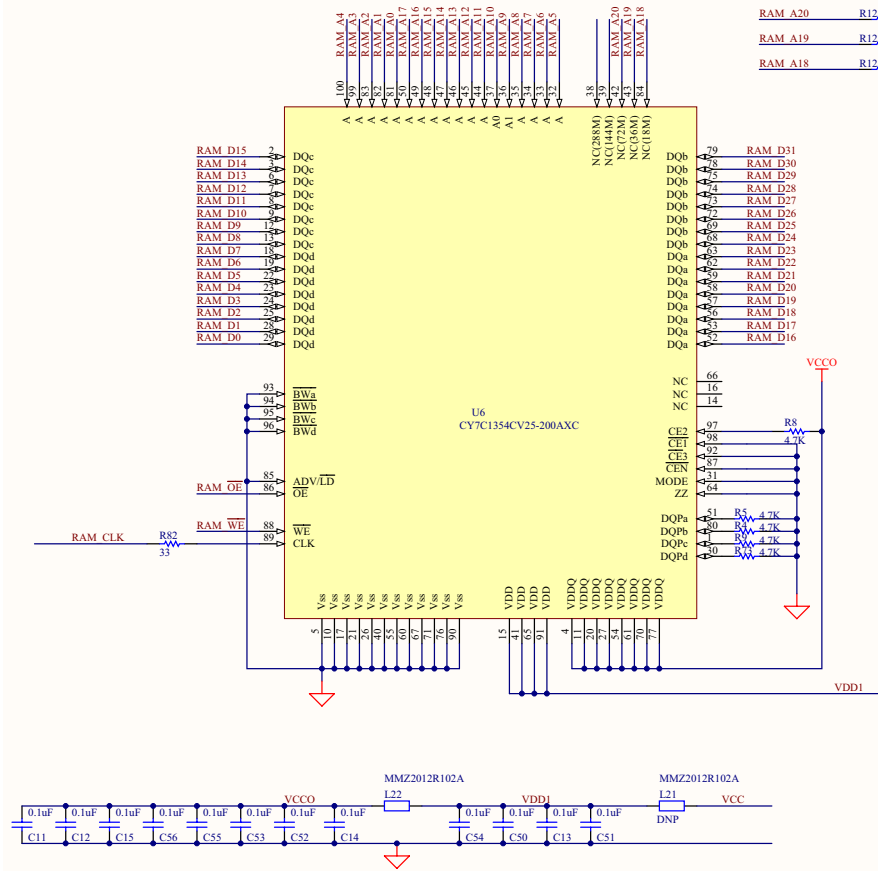


FIGURE 3. MEMORY

KMB001CEVAL Schematics (Continued)

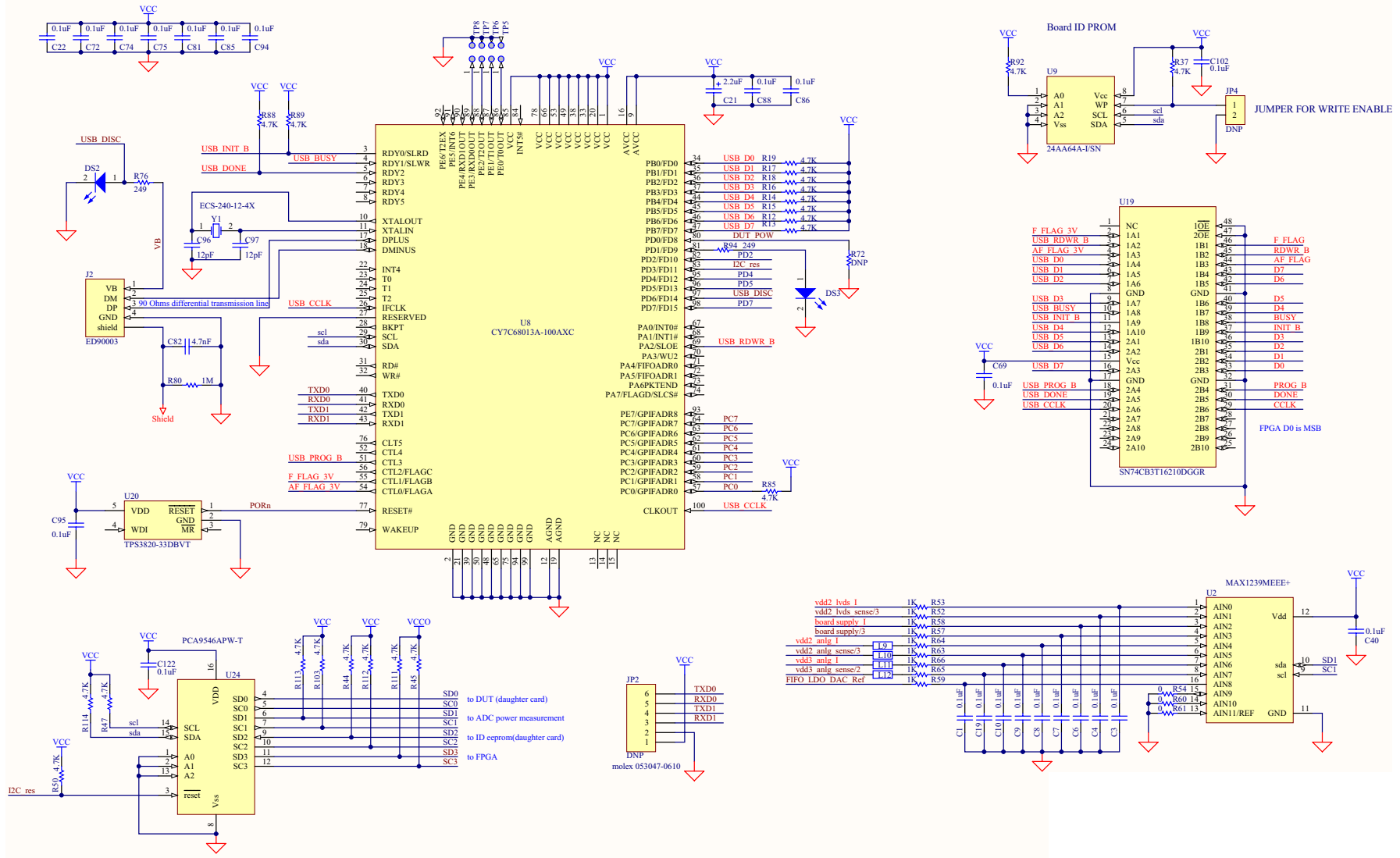


FIGURE 4. USB, MISC.

KMB001LEVAL Schematics

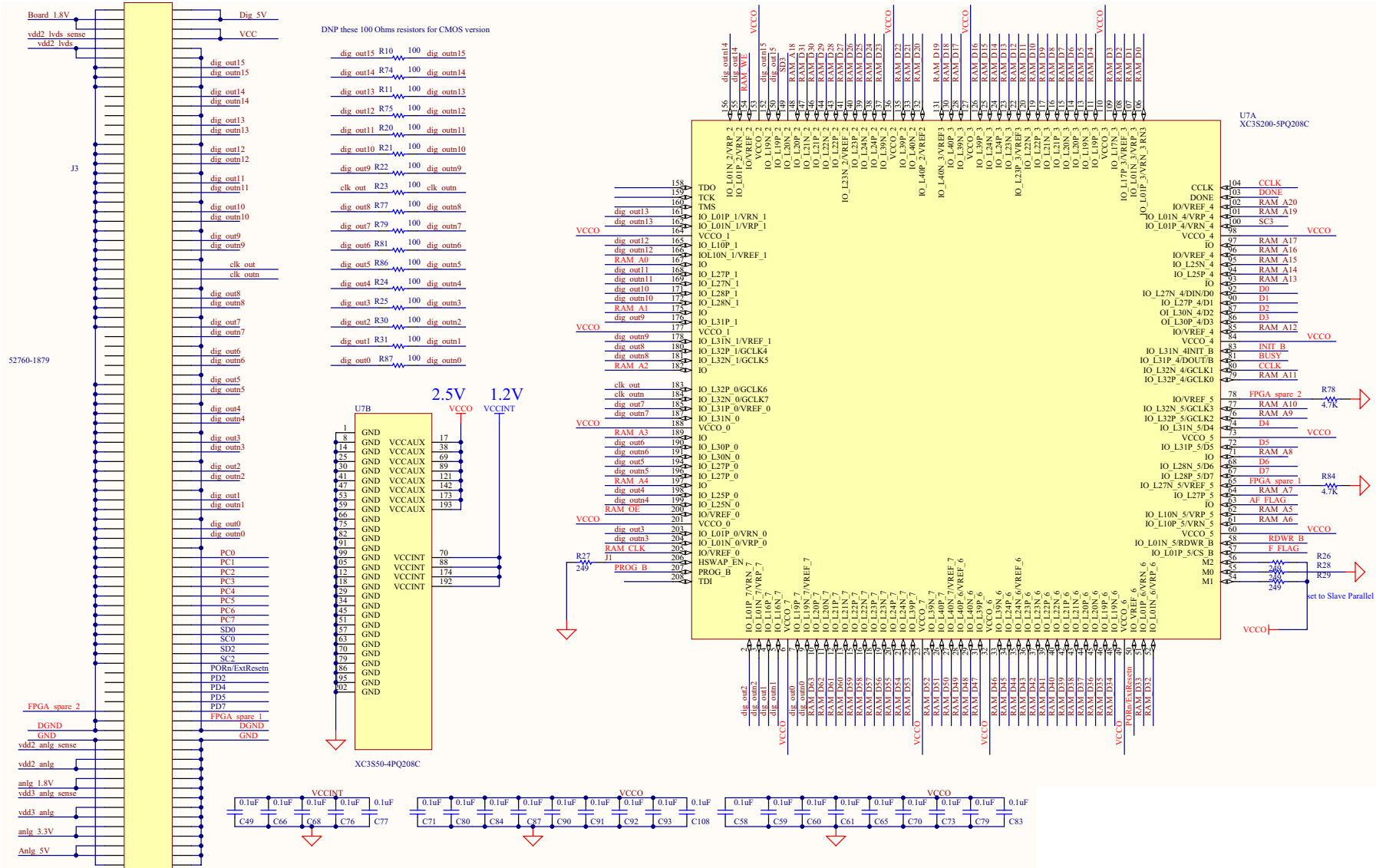


FIGURE 5. FPGA, INPUT/OUTPUT MEZZANINE CONNECTOR

KMB001LEVAL Schematics (Continued)

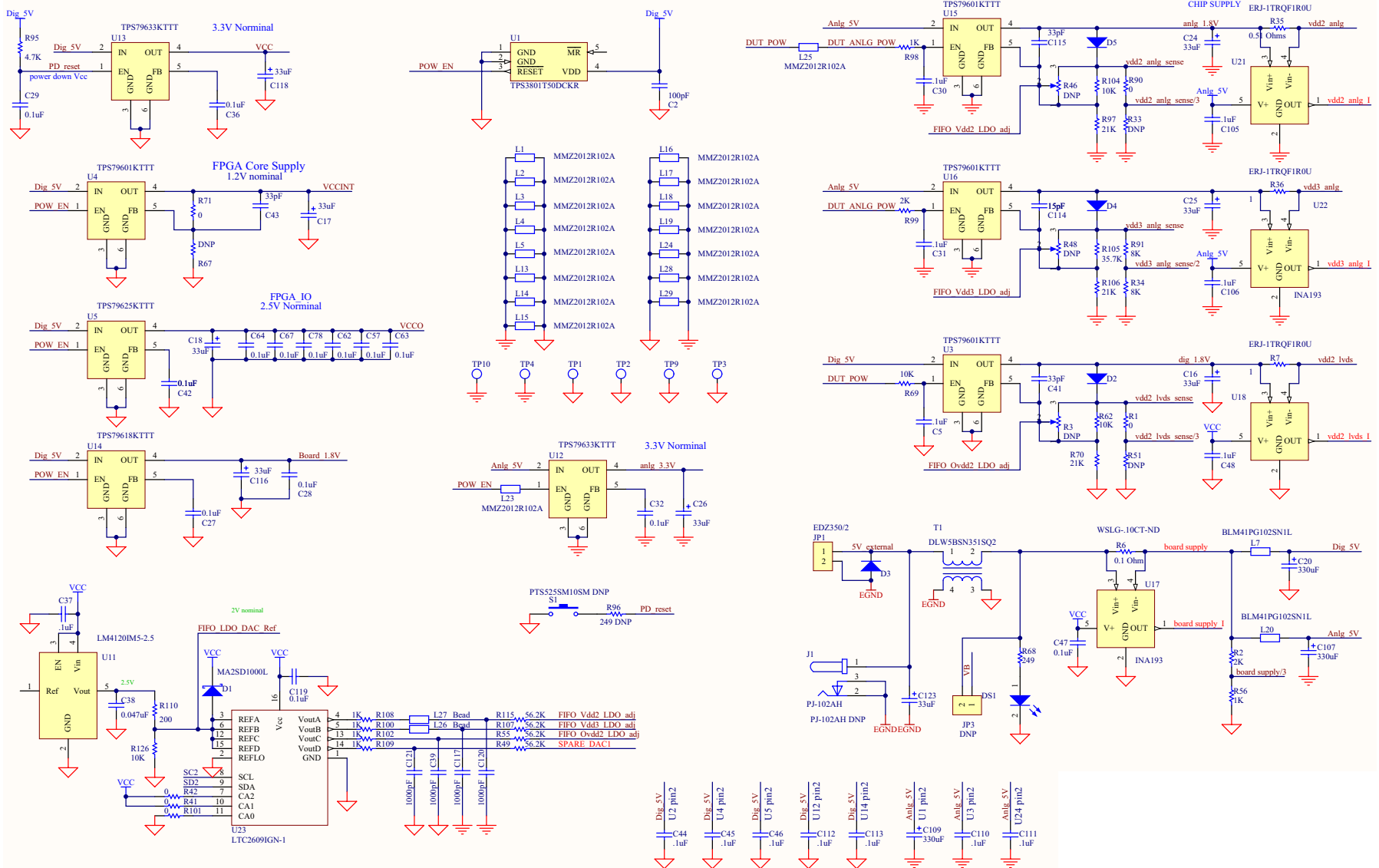


FIGURE 6. POWER

KMB001LEVAL Schematics (Continued)

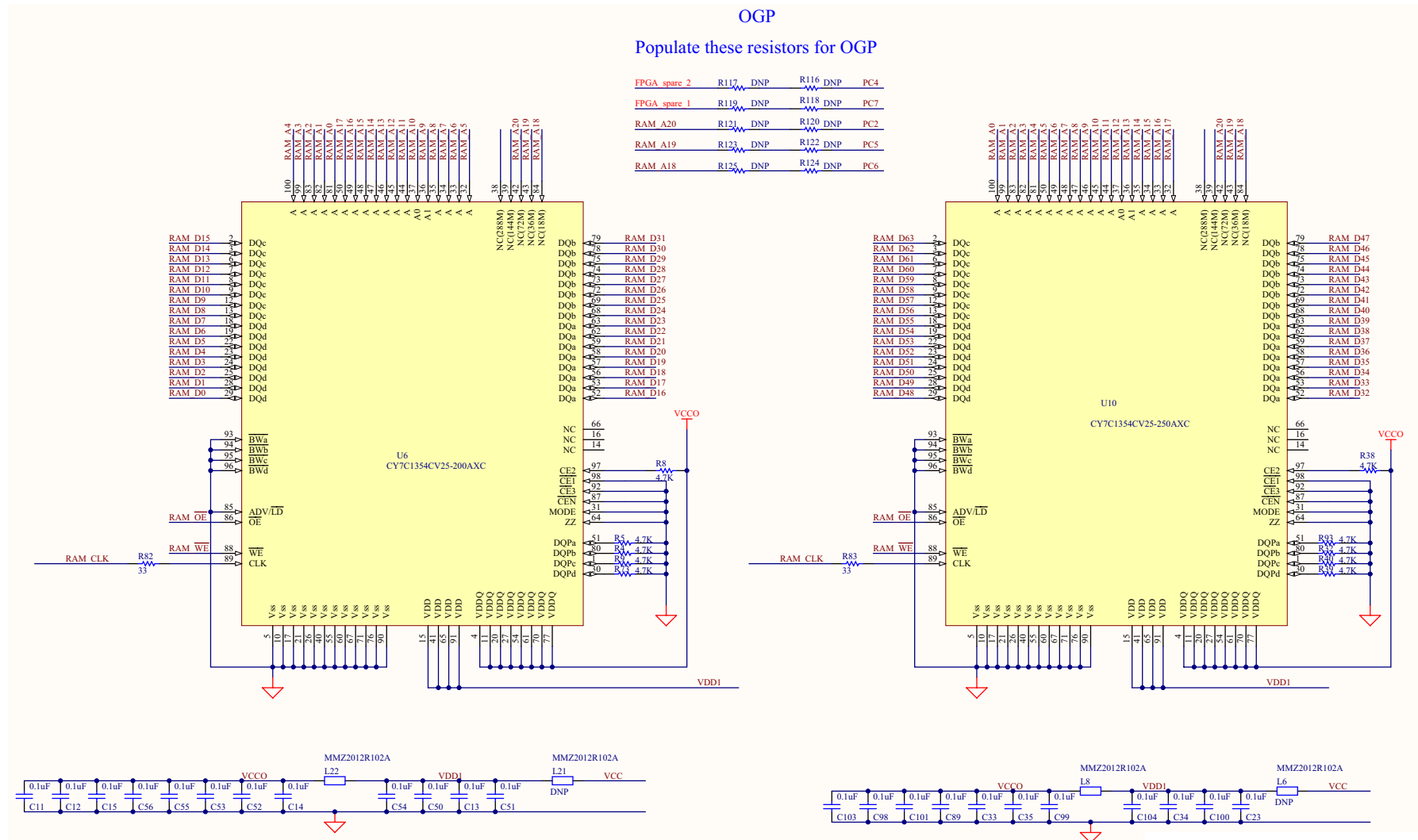


FIGURE 7. MEMORY





KMB001CEVAL Layers

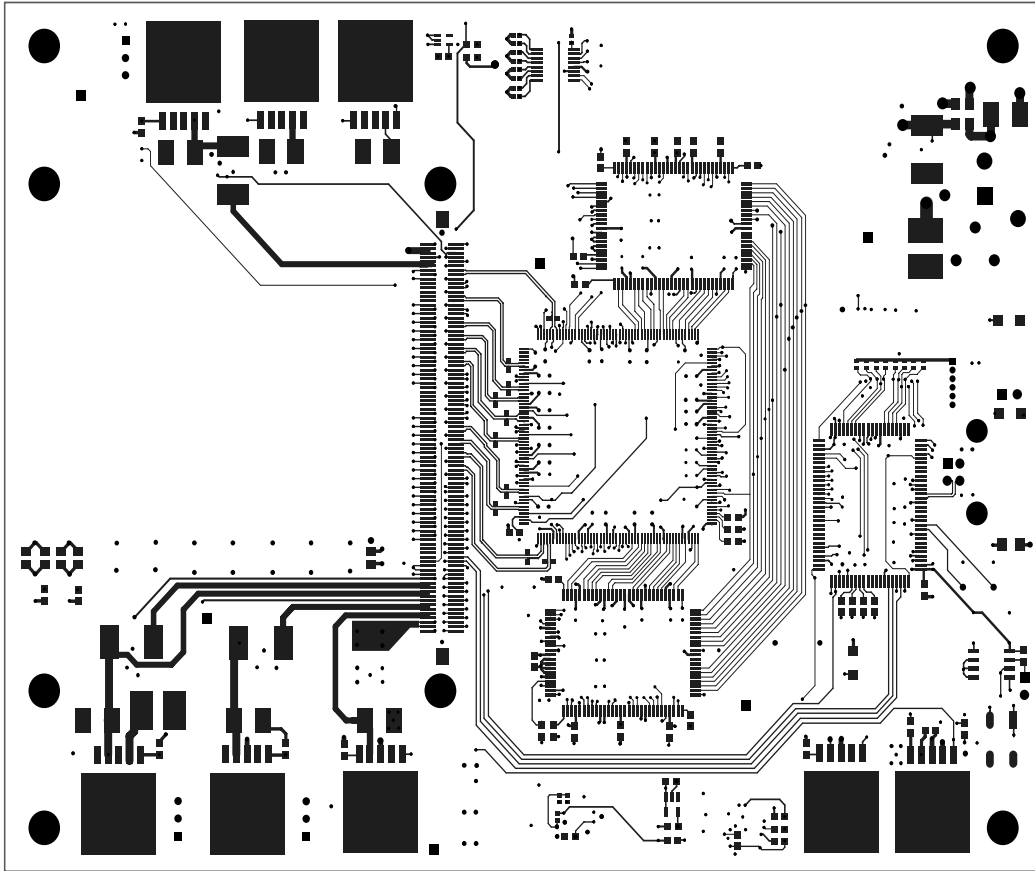


FIGURE 9. TOP LAYER

KMB001CEVAL Layers (Continued)

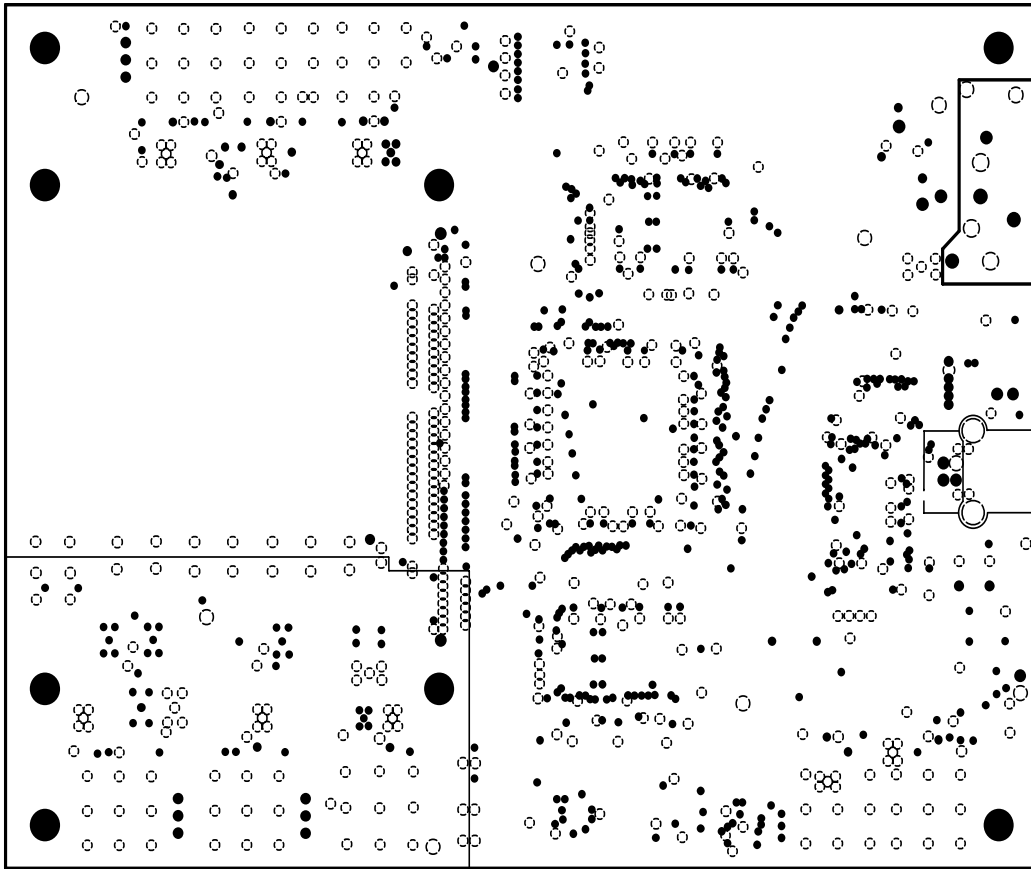


FIGURE 10. GND PLANE

KMB001CEVAL Layers (Continued)

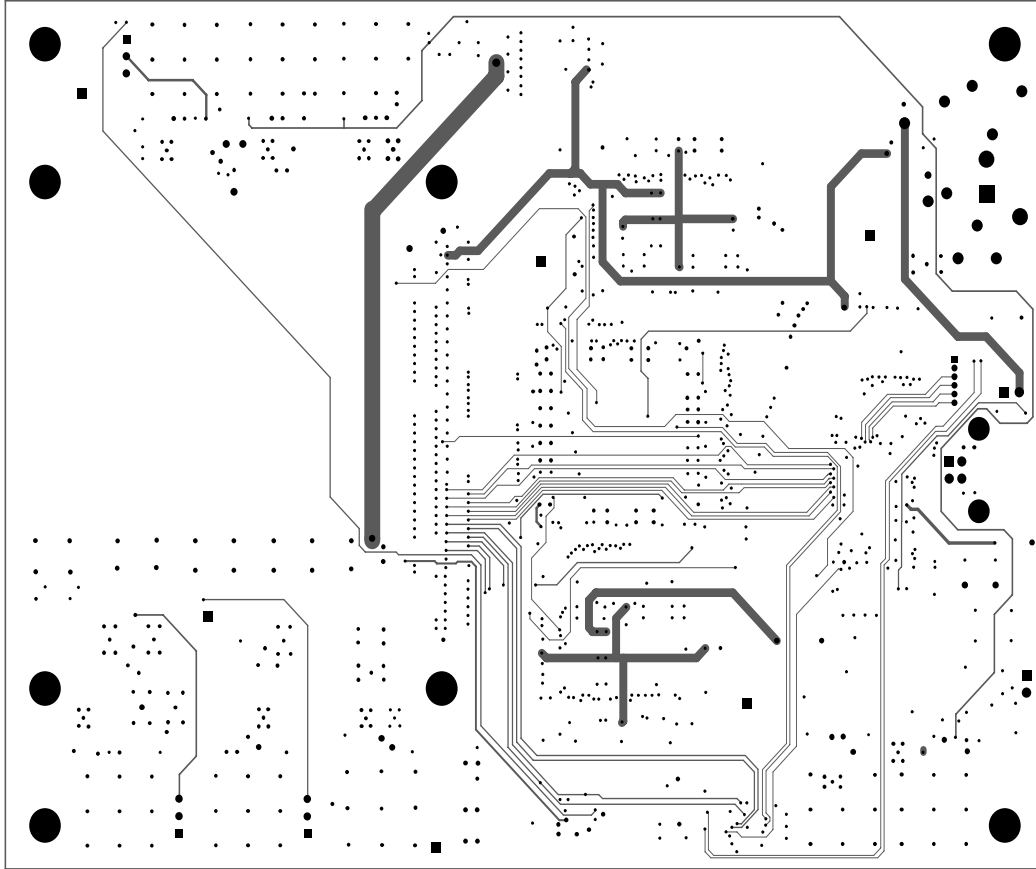


FIGURE 11. MID LAYER 1

KMB001CEVAL Layers (Continued)

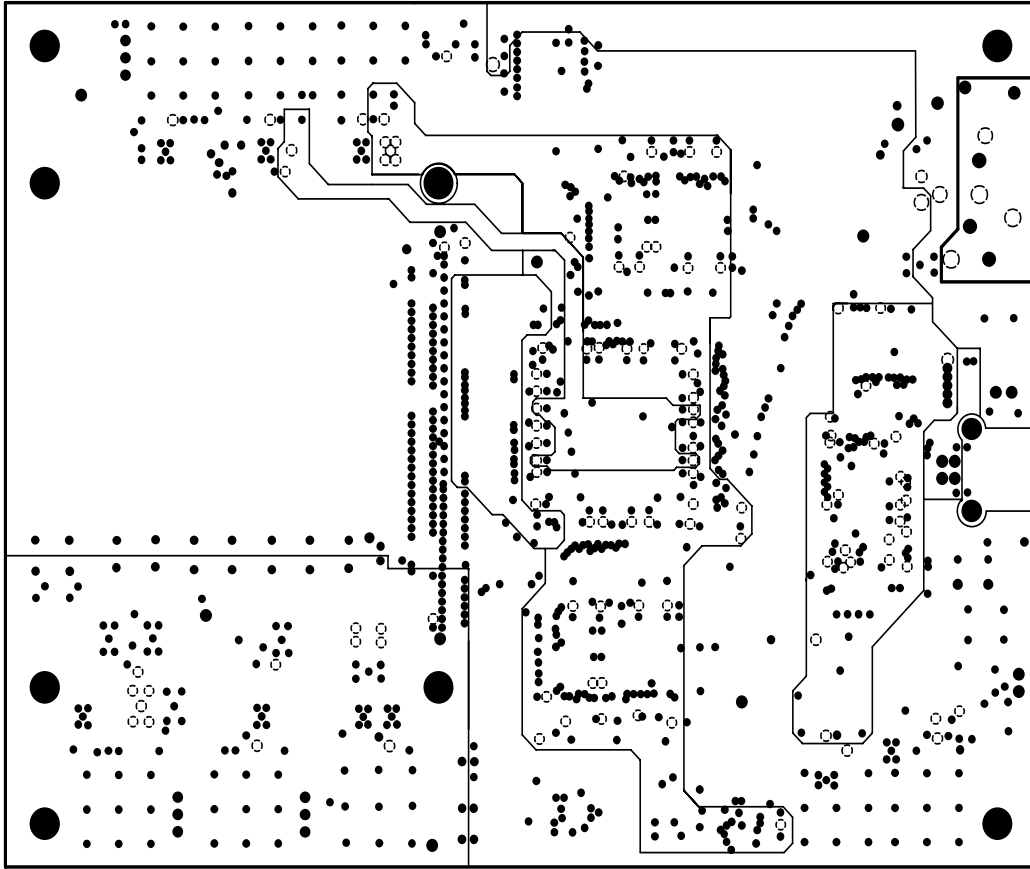


FIGURE 12. POWER PLANE

KMB001CEVAL Layers (Continued)

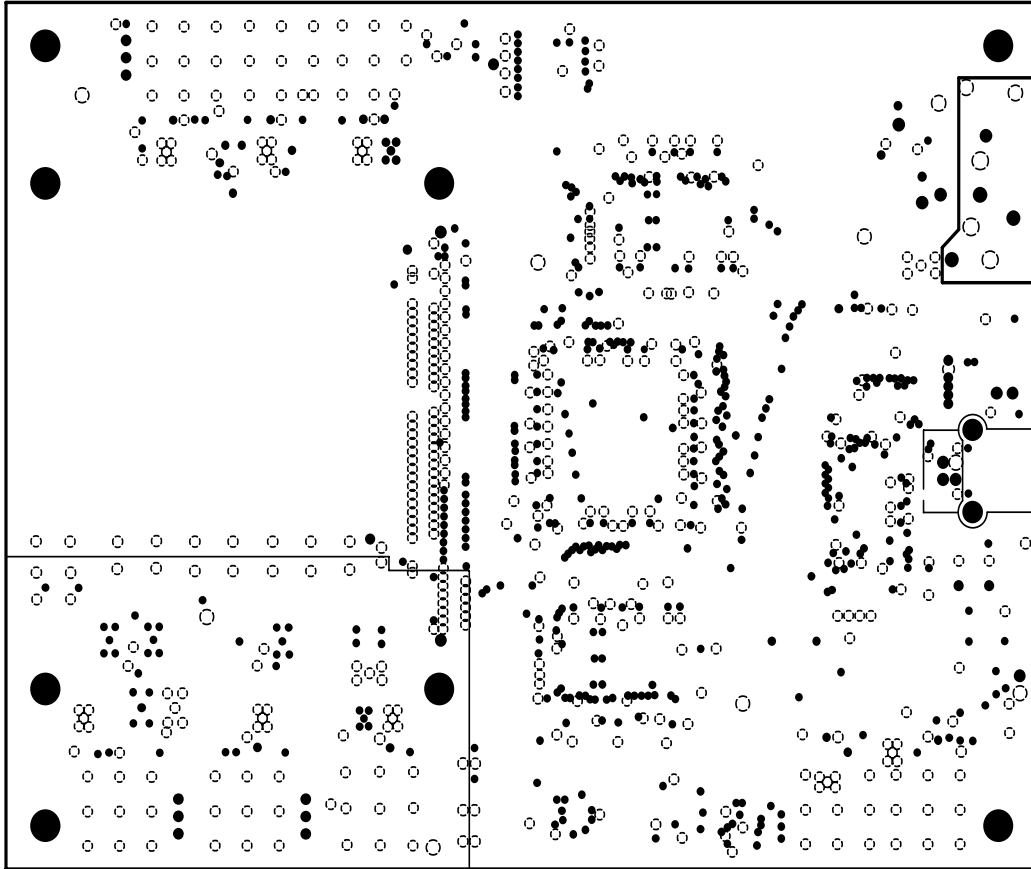


FIGURE 13. GND PLANE 2

KMB001CEVAL Layers (Continued)

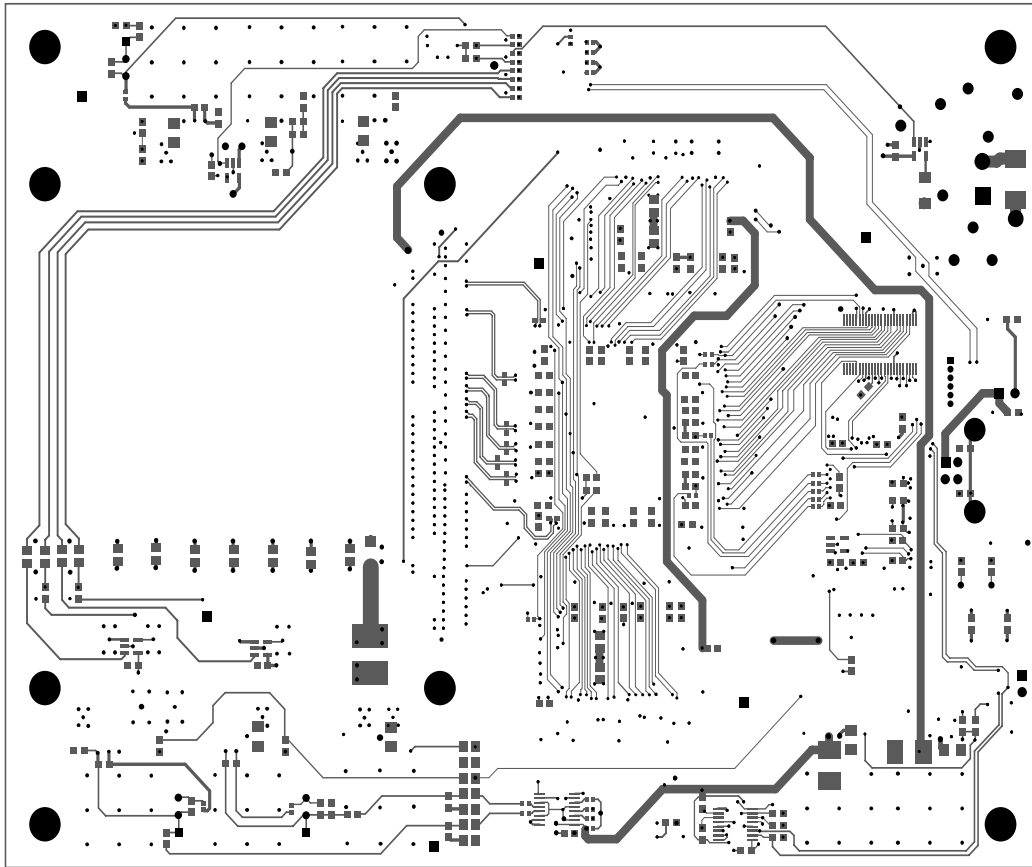


FIGURE 14. BOTTOM LAYER

KMB001CEVAL Layers (Continued)

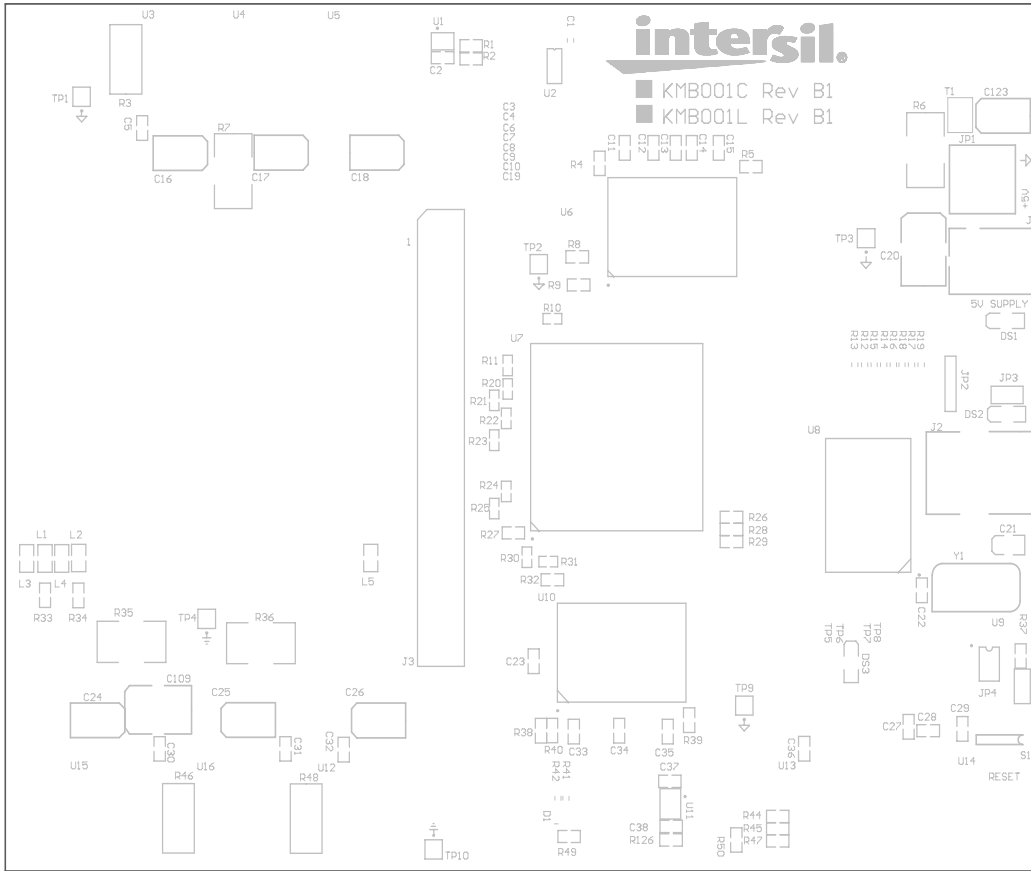


FIGURE 15. TOP OVERLAY

KMB001CEVAL Layers (Continued)

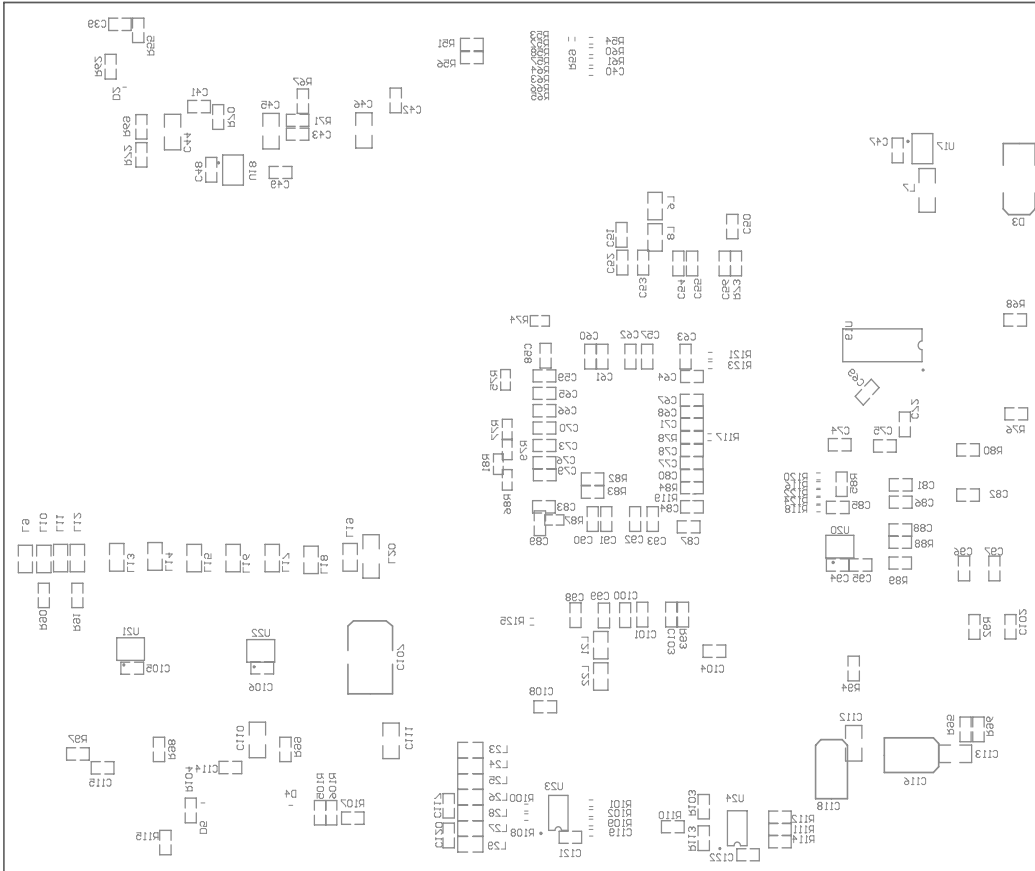


FIGURE 16. BOTTOM OVERLAY

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