KDC5512EVAL, KDC5512HEVAL, KDC5512-50EVAL, KDC5514EVAL Schematics

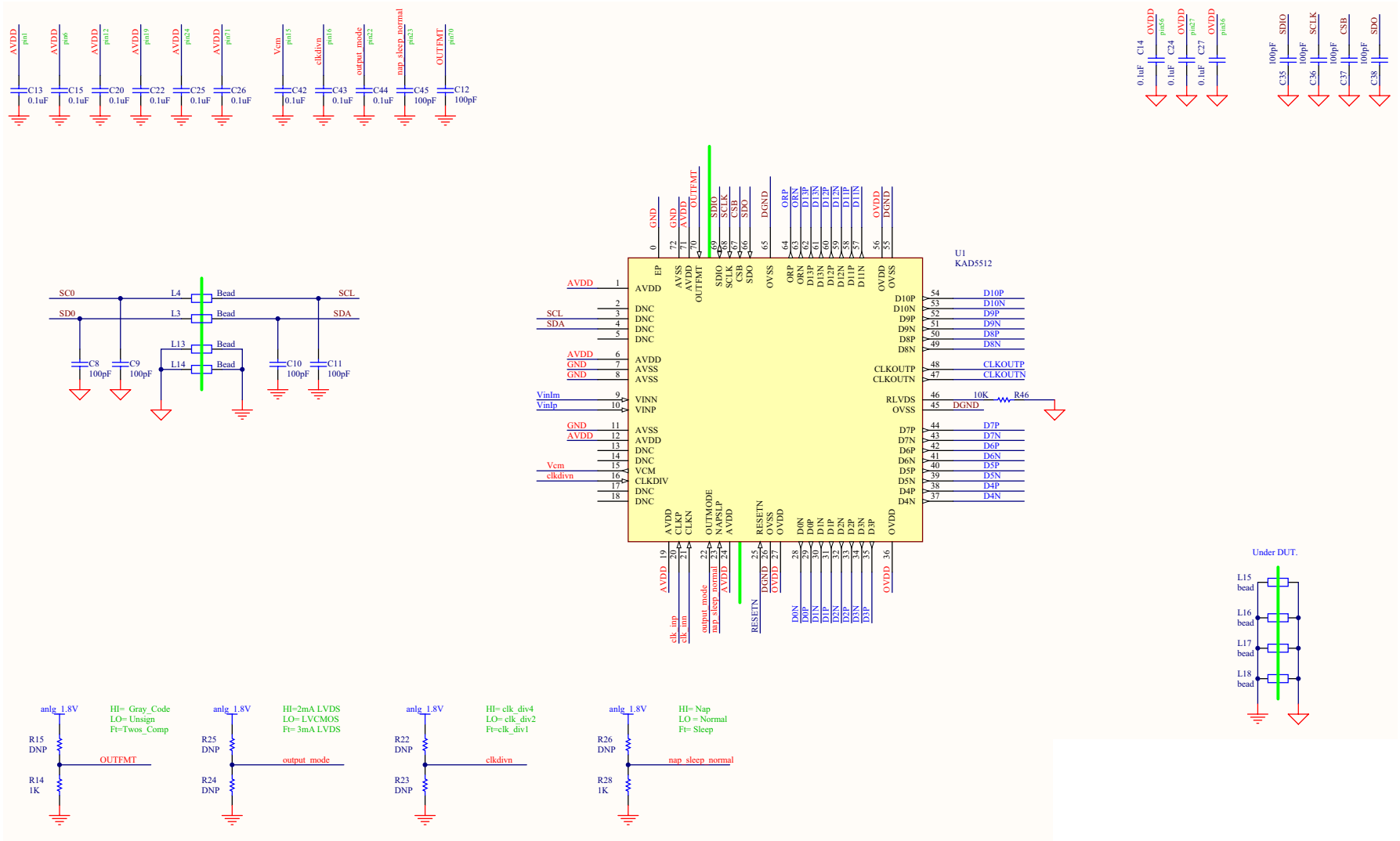

FIGURE 1. ADC, MODE PINS AND POWER SUPPLY BYPASS

KDC5512EVAL, KDC5512HEVAL, KDC5512-50EVAL, KDC5514EVAL Schematics (Continued)

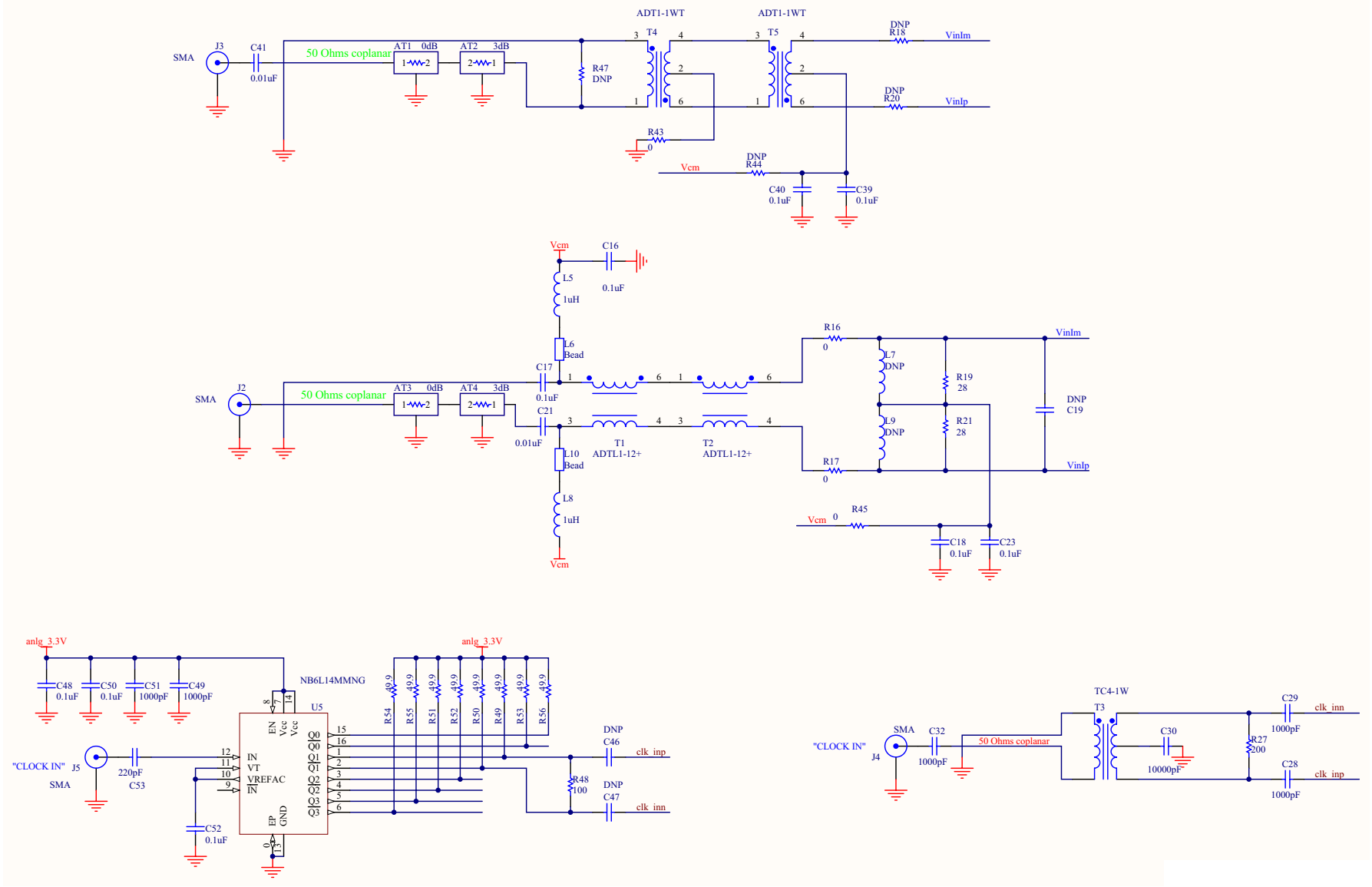

FIGURE 2. CLOCK AND ANALOG INPUTS

KDC5512EVAL, KDC5512HEVAL, KDC5512-50EVAL, KDC5514EVAL Schematics (Continued)

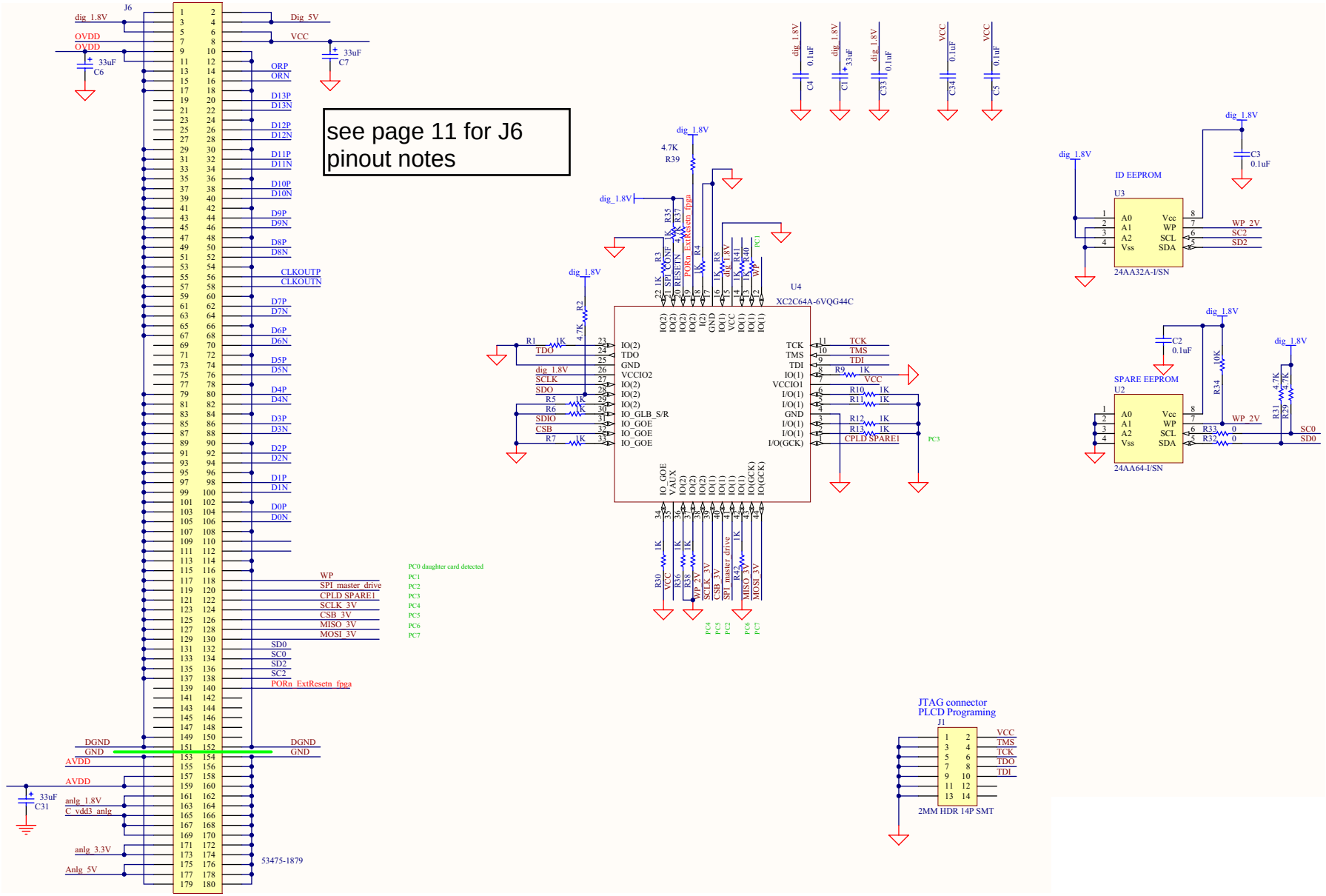

FIGURE 3. INPUT/OUTPUT MEZZANINE CONNECTOR

KDC5512EVAL, KDC5512HEVAL, KDC5512-50EVAL, KDC5514EVAL REV B Layers

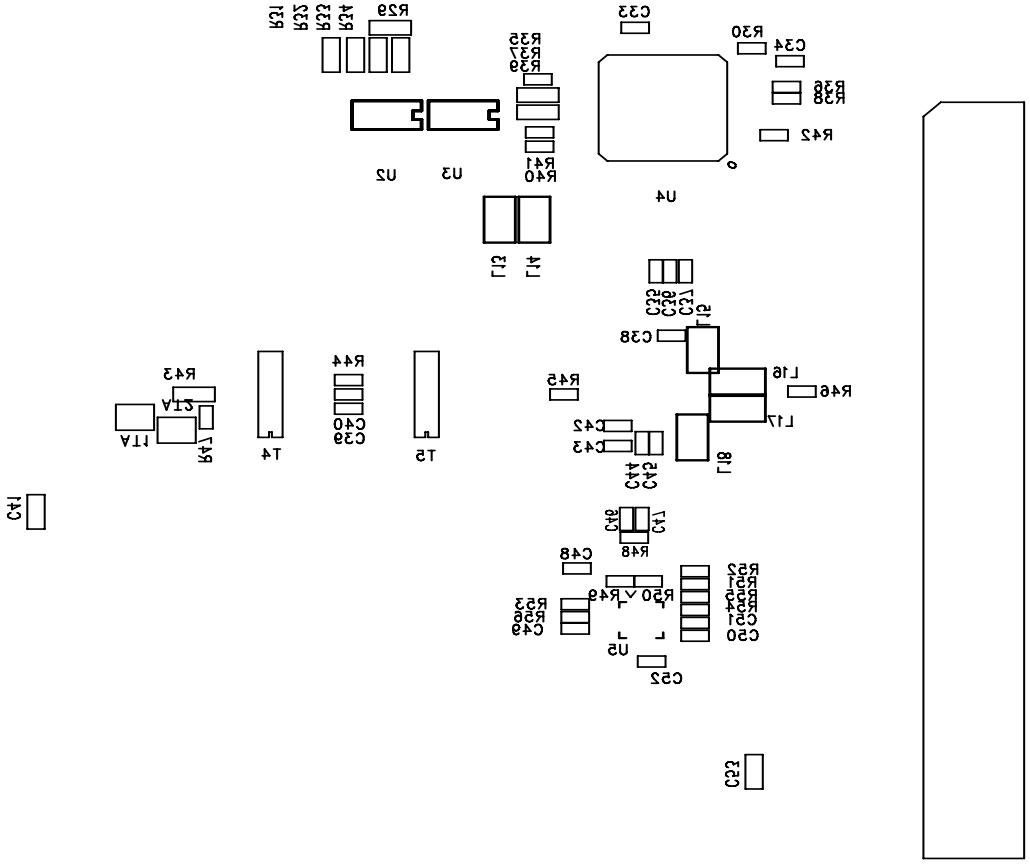

FIGURE 4. LAYER - SECONDARY SIDE SILKSCREEN

KDC5512EVAL, KDC5512HEVAL, KDC5512-50EVAL, KDC5514EVAL REV B Layers (Continued)

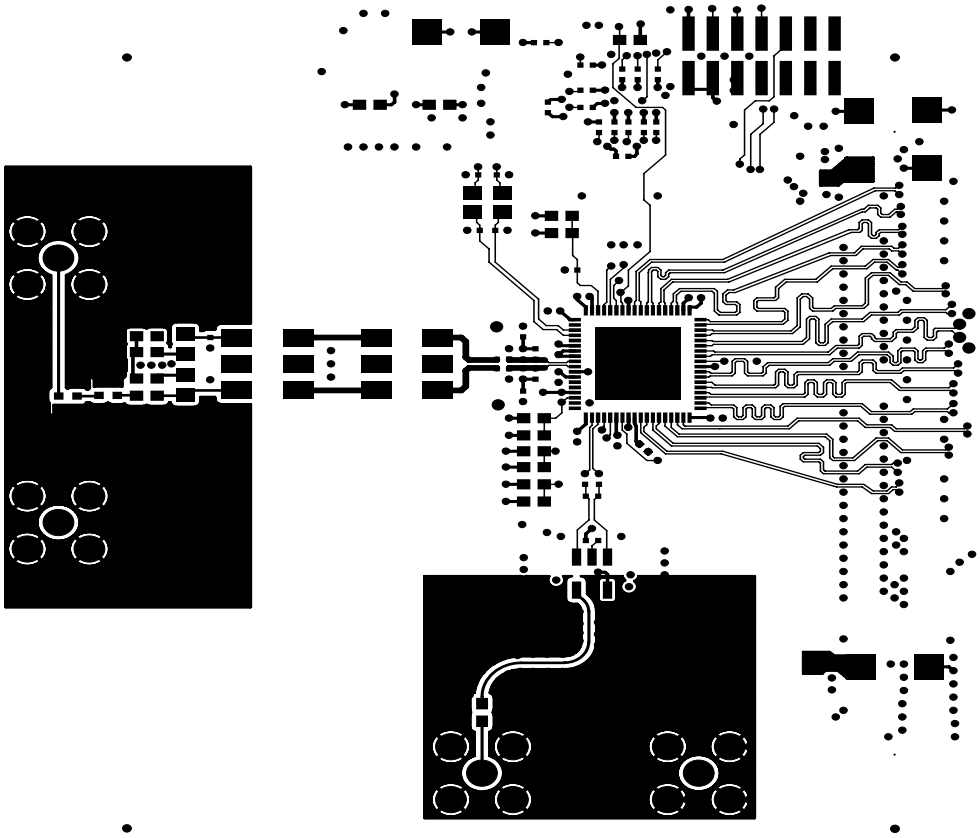

FIGURE 5. LAYER 1 - PRIMARY SIDE

KDC5512EVAL, KDC5512HEVAL, KDC5512-50EVAL, KDC5514EVAL REV B Layers (Continued)

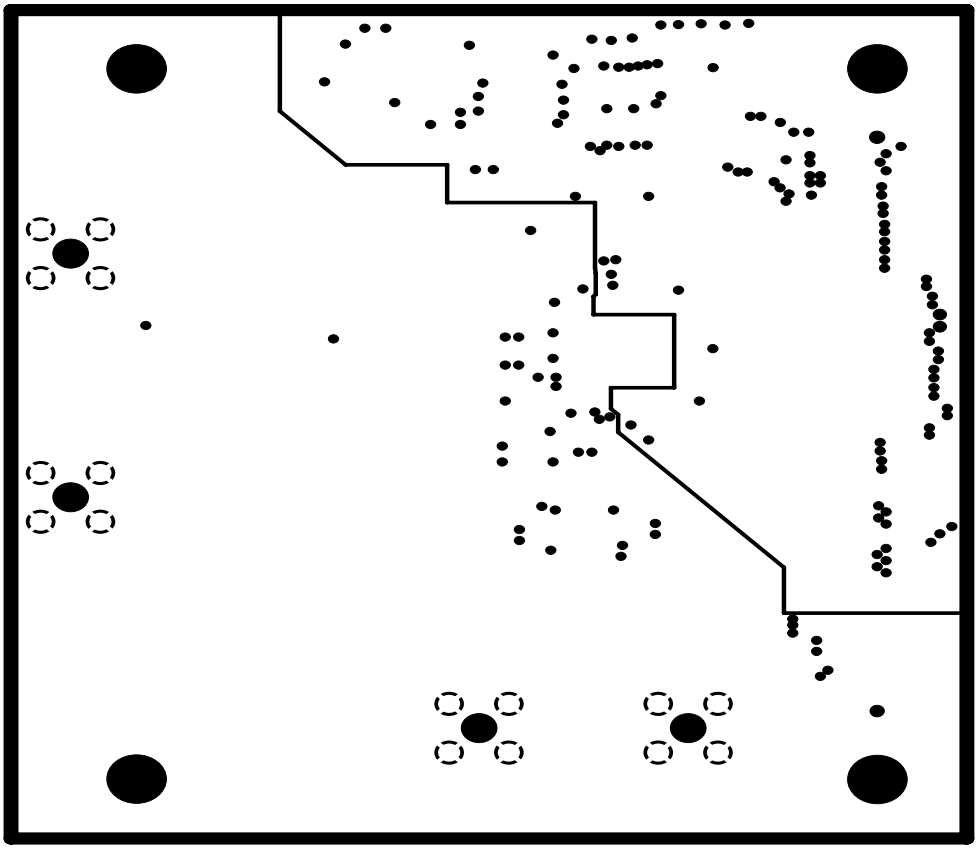

FIGURE 6. LAYER 2 - GND PLANE 1

KDC5512EVAL, KDC5512HEVAL, KDC5512-50EVAL, KDC5514EVAL REV B Layers (Continued)

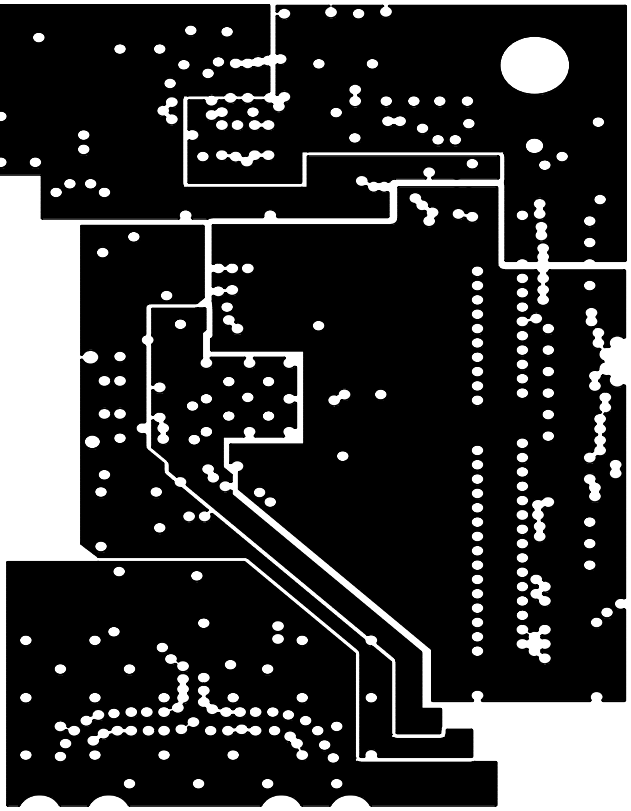

FIGURE 7. LAYER 3 - PWR PLANE

KDC5512EVAL, KDC5512HEVAL, KDC5512-50EVAL, KDC5514EVAL REV B Layers (Continued)

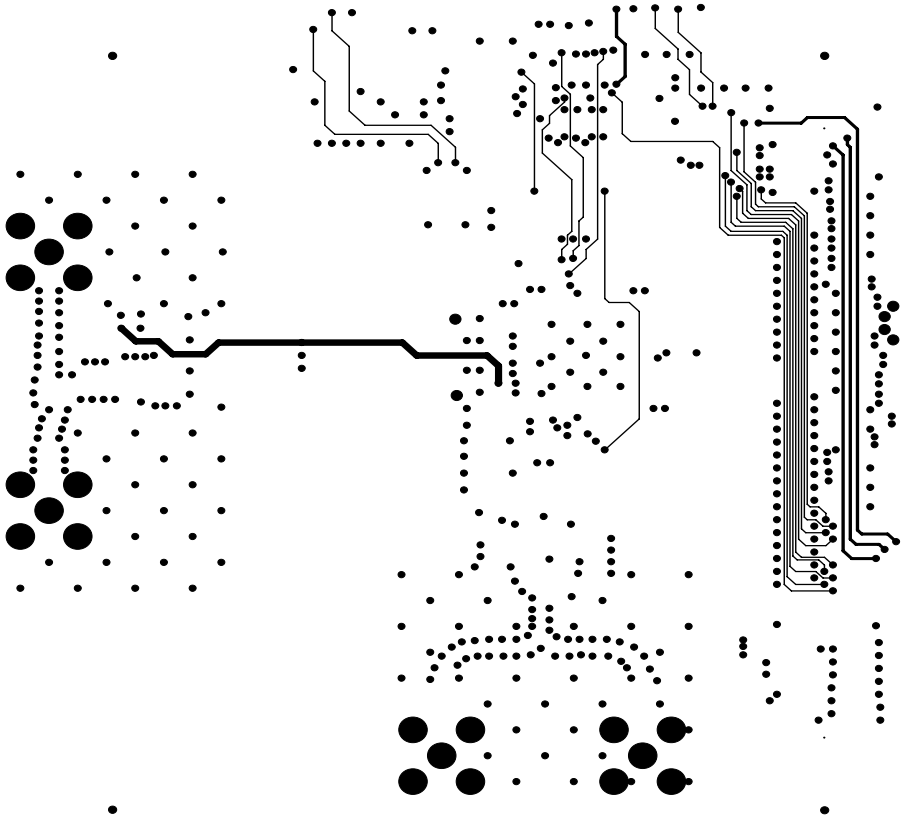

FIGURE 8. LAYER 4 - INTERNAL SIGNAL

KDC5512EVAL, KDC5512HEVAL, KDC5512-50EVAL, KDC5514EVAL REV B Layers (Continued)

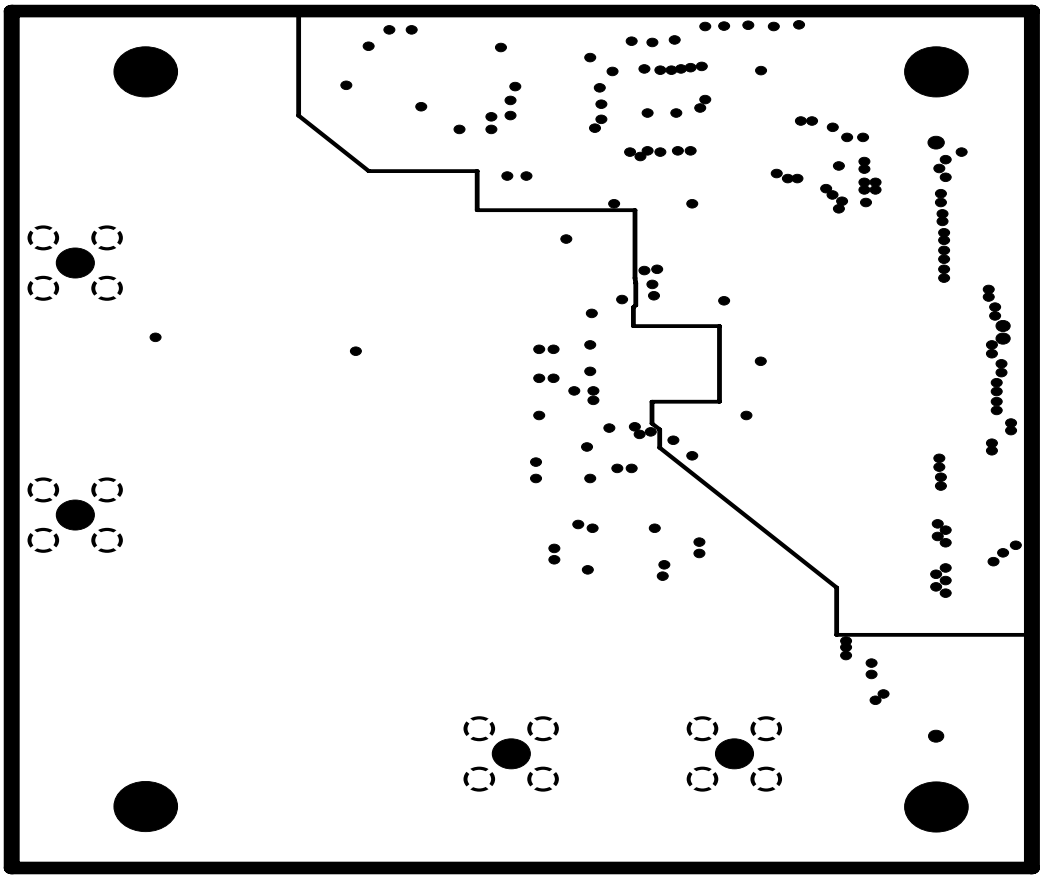

FIGURE 9. LAYER 5 - GND PLANE 2

KDC5512EVAL, KDC5512HEVAL, KDC5512-50EVAL, KDC5514EVAL REV B Layers (Continued)

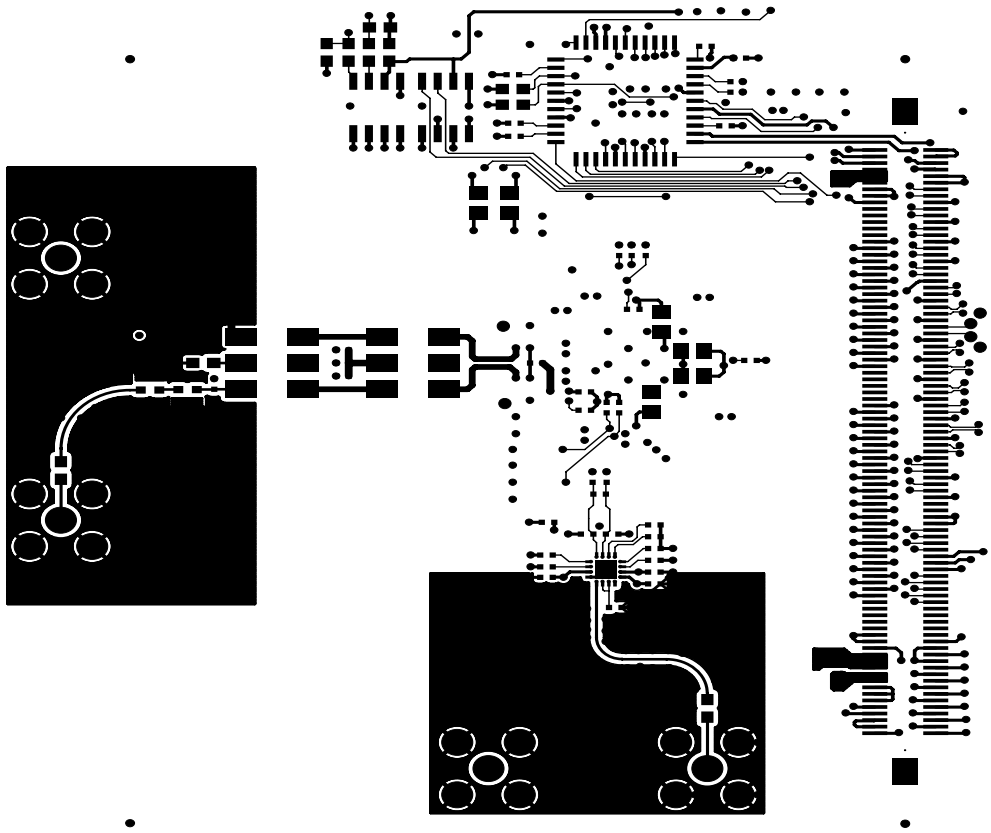

FIGURE 10. LAYER 6 - SECONDARY SIDE

KDC5512EVAL, KDC5512HEVAL, KDC5512-50EVAL, KDC5514EVAL REV B Layers (Continued)

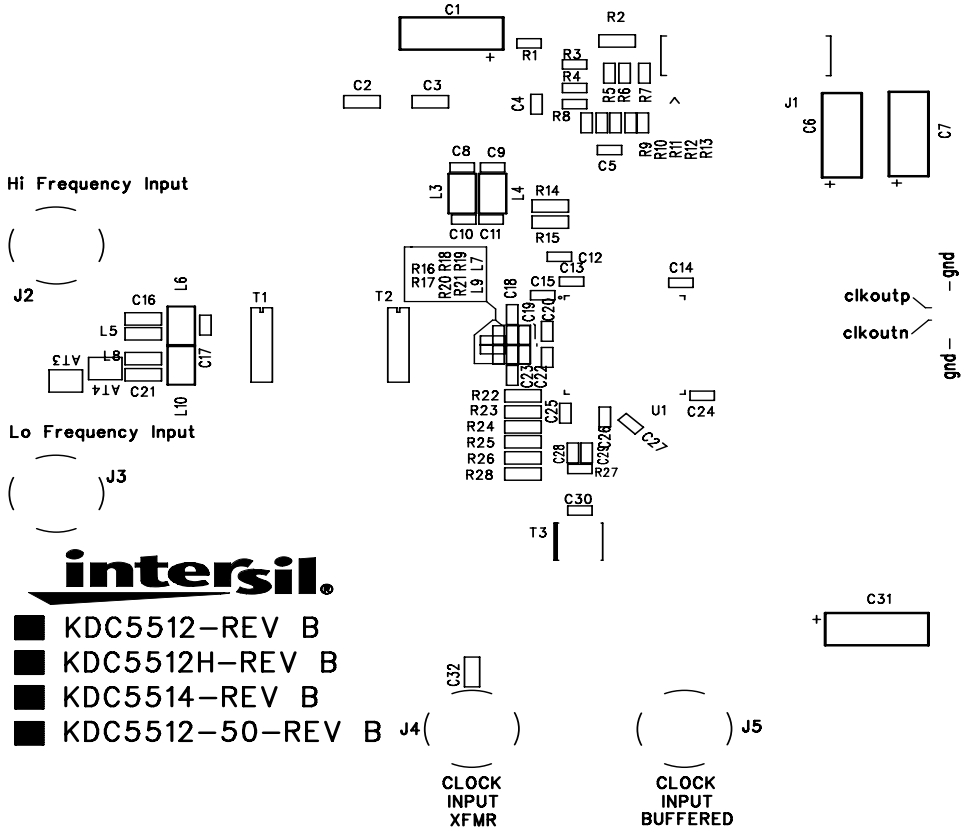

FIGURE 11. LAYER - PRIMARY SIDE SILKSCREEN

J6 pinout is shown for 14bit device. ADC Output Data pins are MSB justified at J6. Pins 20, 22 at J6 are the MSB for 14 ,12, 10 and 8 bit devices (MSB = D13, D11, D9, and D7 for 14,12,10, and 8 bit devices respectively. J6 pins 26,28 are MSB -1. Contact factory for additional information if needed.