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1. Internal Memory

1.1 Block Diagram

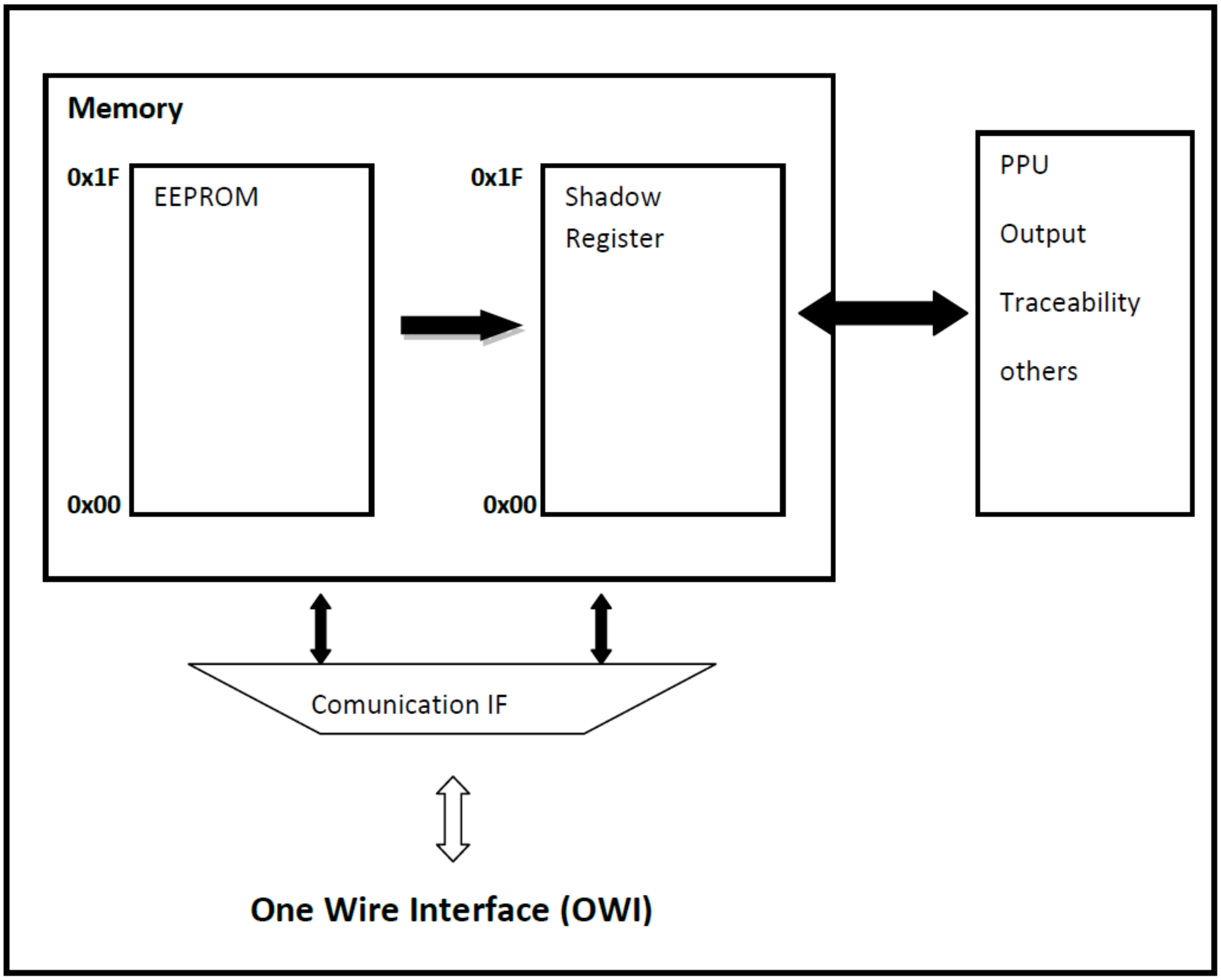

Figure 1. Internal Memory of the ZMID520x

Figure 1 shows the internal memory topology of the ZMID520x products which is split up into a non-volatile EEPROM (E2P) and a volatile shadow ram (SWR) section. After chip start up the E2P content is copied into the SWR. During IC operation in OWI mode, changes in the SWR will take immediate effect whereas changes in the E2P require an IC power cycle. (Power off/Power on).

Definitions:

0b Binary number prefix.

0x Hexadecimal number prefix.

Table 1. Internal Memory

Address	Name	Type	Location	Function
0x00	Offset	R/W	E2P/SWR	14-bit zero- Zero Angle offset of output signal
0x01	Slope	R/W	E2P/ SWR	13-bit slope value of output signal

Address	Name	Type	Location	Function
0x02	Clamping	R/W	E2P/SWR	Clamp values of output signal
0x03	LinInt0	R/W	E2P/SWR	Linear interpolation of output signal corr1@12.5% (45°) - bit15…8 corr0@0%(0°) - bit7…0
0x04	LinInt1	R/W	E2P/SWR	Linear interpolation of output signal corr3@37.5% (135°) - bit15…8 corr2@25%(90°) - bit7…0
0x05	LinInt2	R/W	E2P/SWR	Linear interpolation of output signal corr5@62.5% (225°) - bit15…8 corr4@50%(180°) - bit7…0
0x06	LinInt3	R/W	E2P/SWR	Linear interpolation of output signal corr7@87.5% (315°) - bit15…8 corr6@75%(270°) - bit7…0
0x07	LinInt4	R/W	E2P/SWR	Linear interpolation of output signal not used - bit15…8 corr8@100%(360°) - bit7…0
0x08	Coil offset	R/W	E2P/SWR	Signal Offset correction of the demodulated input signals - sin and cos (r1,r2 - Ycos,Xsin); Only apply if constant input gain setting is activated.
0x09	CalMode	R/W	E2P/SWR	Calibration mode register contains control bits for output Mode like linear or modulo360 mode sensor; linear correction mode like pre-&post-calibration; Angle offset for linearity correction like 0° or -22.5°; Swap receiver coils polarity ….
0x0A	Output	R/W	E2P/SWR	Output register is used for configuration of the output SENT CRC, SENT Pause, PWM slope current, PWM freq, Analog diagnostic level.
0x0B	Trimming	R/W	E2P/SWR	This register contains control parameters for: PWM slope time, OSR, LC oscillator current, VDDT voltage calibration
0x0C	AGC0	R/W	E2P/SWR	Basic configurations of the analog front-end in terms of timing and gain e.g: Automated gain scheduling in number of samples; Integrator gain stage;
0x0D	AGC1	R/W	E2P/SWR	Configurations of excitation coil frequency limits (alarm setting); CORDIC magnitude limits; Interlink mode (integration time adaption and gain adaption)
0x0E	Mask	R/W	E2P/SWR	Diagnostic mask register is controlling which alarms are generating an output diagnostic flag e.g: Receiver coil1 open/short; Excitation coil break;
0x0F	Trace0	R/W	E2P	factory traceability code 0
0x10	Trace1	R/W	E2P	factory traceability code 1
0x11	Misc	R/W	E2P/SWR	Configuration of voltage regulators and oscillators; e.g. switch off VDDT regulator in case of excitation coil alarm
0x13	Afe_agc	R	SWR	Analog front-end/ Automatic gain regulation. Polarity of R1 & R2 ADC gain. AGC nr. of integration cycles
0x14	Xsine	R	SWR	13-bit Cordic raw input signal
0x15	Ycosine	R	SWR	13-bit Cordic raw input signal
0x16	Angle	R	SWR	15-bit Cordic output angle (0° to 90°)
0x17	Cordic Magnitude	R	SWR	15-bit Cordic output magnitude
0x18	Spa	R	SWR	Spatial angle 16-bit output angle (0° to 360°) before output calibration and linear error correction.
0x19	Pos0	R	SWR	Position0 16-bit output angle (0° to 360°) after output calibration; If linearization done before output calibration this value = Position1; If linearization done after output calibration this value ≠ Position1
0x1A	Pos1	R	SWR	Position1 16-bit output angle (0° to 360°) after output calibration and linearization; This value is always affected by

1.2 Offset

Address of register: 0x00.

Default value: 0x0000.

The offset parameter is used for the calibration of the position transfer function. The notation of the offset parameter depends on the output mode (see 1.12). Two output modes can be selected (modulo360 or linear).

Output mode: Modulo360 (set out_mod = 0b1 (1.10), for selecting the output mode “360Modulo”)

Table 2. Offset Register Description

Bits	Symbol	Description	
Off.15 - Off.14	Reserved	Not used, read as 0 (SWR).	
Off.13 - Off.0	Offset	Offset of output transfer function.	
		Offset Value	**Value in Degree**
		0x0000	0
		0x0800	45
		0x1000	90
		0x1800	135
		0x2000	180
		0x2800	225
		0x3000	270
		0x3800	315
		0x3FFF	360

Note: The reserved bits off.15 & off.14 can be written and read to/from the block E2P. The copy process copies only bits (off.13 down to off.0) to the SWR.

Output mode: Linear (set out_mod = 0b0 (see section 1.11.1), for selecting Linear Output mode).

Table 3. Offset Register Description Modulo 360

Bits	Symbol	Description	
Off.15 - Off.14	Reserved	Not used, read as 0 (SWR).	
Off.13 - Off.0	Offset	Offset of output transfer function.	
		Offset Value	**Value in Degree**
		0x0000	180
		0x0400	360
		0x0800	540
		0x0C00	720
		0x1000	900
		0x1400	1080
		0x1800	1260
		0x1C00	1440
		0x1FFF	1620
		0x2000	180
		0x2400	0
		0x2800	-180
		0x2C00	-360
		0x3000	-540
		0x3400	-720
		0x3800	-900
		0x3C00	-1080
		0x3FFF	-1260

Note: The reserved bits off.15 & off.14 can be written and read to/from the block E2P. The copy process copies only bits (off.13 down to off.0) to the SWR.

1.3 Slope

Address of register: 0x01.

Default value: 0x0400.

1.3.1. Slope of Transfer Function

The slope parameter is used for the calibration of the position transfer function. It is a multiplication factor for the spatial angle. The slope notation is independent from the out_mode parameter (see section 1.12).

Table 4. Slope Register Description

<table>
<tr><th>Bits</th><th>Symbol</th><th>Description</th></tr>
<tr><td>slp.15 - slp.13</td><td>Reserved</td><td>Not used, read as 0 (SWR)</td></tr>
<tr><td>slp.12 - slp.0</td><td>Slope</td><td>Slope of output transfer function.
<table>
<tr><th>Offset Value</th><th>Value in Degree</th></tr>
<tr><td>0x0000</td><td>0.0</td></tr>
<tr><td>0x0100</td><td>0.25</td></tr>
<tr><td>0x0200</td><td>0.5</td></tr>
<tr><td>0x0300</td><td>0.75</td></tr>
<tr><td>0x0400</td><td>1.0</td></tr>
<tr><td>0x0800</td><td>2.0</td></tr>
<tr><td>0x0C00</td><td>3.0</td></tr>
<tr><td>0x0FFF</td><td>3.999</td></tr>
<tr><td>0x1000</td><td>-0.0</td></tr>
<tr><td>0x1100</td><td>-0.25</td></tr>
<tr><td>0x1200</td><td>0.5</td></tr>
<tr><td>0x1300</td><td>0.75</td></tr>
<tr><td>0x1400</td><td>-1.0</td></tr>
<tr><td>0x1800</td><td>-2.0</td></tr>
<tr><td>0x1C00</td><td>-3.0</td></tr>
<tr><td>0x1FFF</td><td>-3.999</td></tr>
</table></td></tr>
</table>

Note: The reserved bits slp.15, slp.14 and slp.13 can be written and read to/from the block E2P.

1.3.2. Slope example

Slope value coded on 13bits with a range between -4 to +4, 1 bit is the sign and defines the sign of (slope).

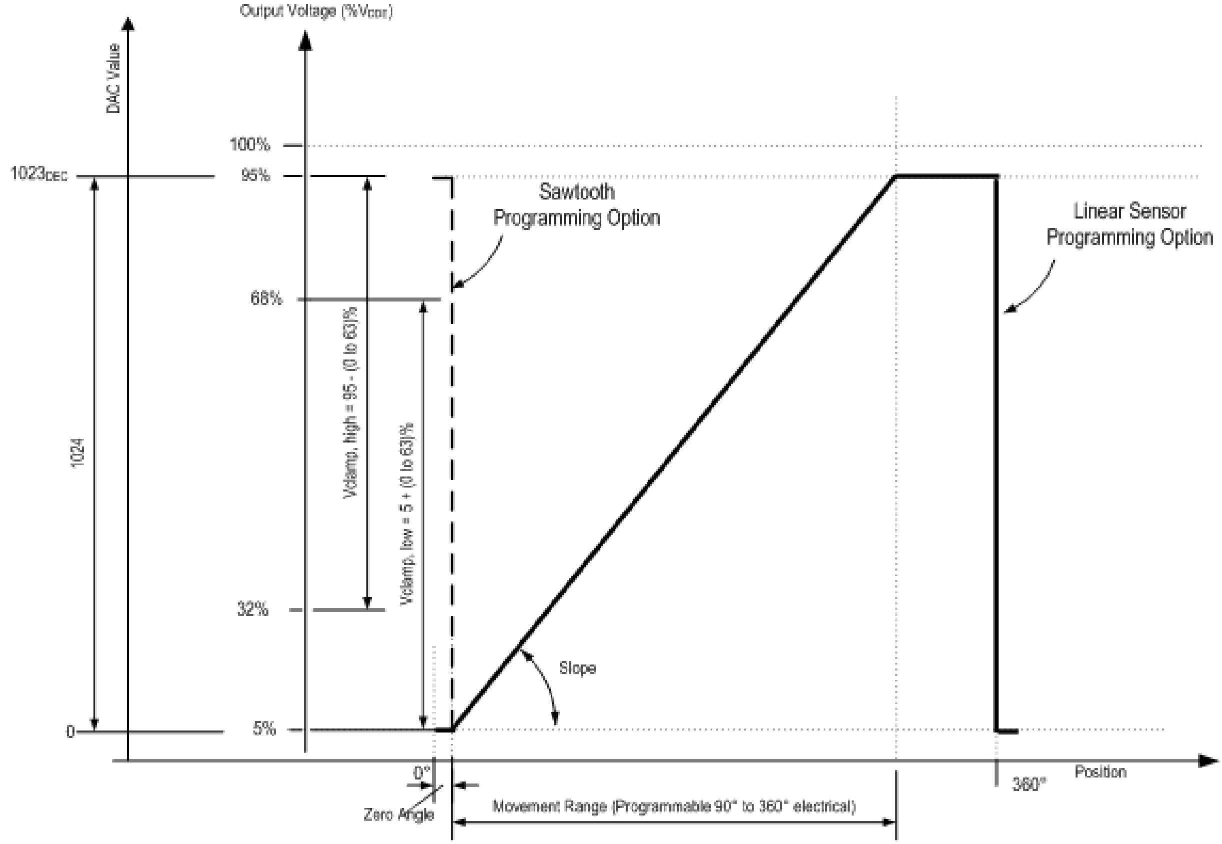

Figure 2. Internal Memory of the ZMID520x

Figure 2 shows the internal memory topology of the ZMID520x products which is split up into a non-volatile EEPROM (E2P) and a volatile shadow ram (SWR) section. After chip start up the E2P content is copied into the SWR. During IC operation in OWI mode, changes in the SWR will take immediate effect whereas changes in the E2P require an IC power cycle. (Power off/Power on).

1.4 Clamping

Address of register: 0x02.

Default value: 0x0000.

The clamping parameters clamp_low and clamp_high are located in the clamp memory. These two parameters are used for position calibration if the output protocol mode is for ZMID5201 and 02. For the Analog output mode the complete 100% position range is mapped to 5% to 95% of the VDD. The stepping rate of the clamping parameters is 0.9%VDD. The diagnostic low level is less or equal 4% VDD, the high level is higher or equal 96% VDD.

For the PWM output mode the position range is mapped to the Pulse Pause Ratio (PPR) of a periodic analog output signal. 100% position range is mapped to the PPR-range from 5% to 95%. When a clamping step of 1% is mapped to a PPR change of 0.9% (e.g. clamp_low = 10% & pos <= clamp_low --> PPR = 5% + 9%). The diagnostic low level is mapped to 2.5% PPR, the high level is mapped to 97.5% PPR.

Table 5. CLAMP Register Description

Bits	Symbol	Description
clamp. 15 -clamp. 14	Reserved	Not used, read as 0 (SWR)

<table>
<tr><th>Bits</th><th>Symbol</th><th>Description</th></tr>
<tr><td>clamp. 13 - clamp. 8</td><td>clamp_high</td><td>Position output clamp high descend from 95%VDD(Analog) resp. 95% (PWM).
<table>
<tr><th>clamp_high (CLAMP13 - CLAMP08)</th><th>Rate (%)</th></tr>
<tr><td>0x00</td><td>0</td></tr>
<tr><td>0x01</td><td>1</td></tr>
<tr><td>0x02</td><td>2</td></tr>
<tr><td>….</td><td>….</td></tr>
<tr><td>….</td><td>….</td></tr>
<tr><td>….</td><td>….</td></tr>
<tr><td>….</td><td>….</td></tr>
<tr><td>0x3F</td><td>63</td></tr>
</table></td></tr>
<tr><td>clamp. 7 - clamp.6</td><td>Reserved</td><td>Not used, read as 0 (SWR)</td></tr>
<tr><td>clamp. 5 - clamp. 0</td><td>clamp_low</td><td>Position output clamp low rising from 5%VDD (Analog) resp. 5% (PWM)
<table>
<tr><th>clamp_low (CLAMP5 - CLAMP00)</th><th>Rate (%)</th></tr>
<tr><td>0x00</td><td>0</td></tr>
<tr><td>0x01</td><td>1</td></tr>
<tr><td>0x02</td><td>2</td></tr>
<tr><td>….</td><td>….</td></tr>
<tr><td>….</td><td>….</td></tr>
<tr><td>….</td><td>….</td></tr>
<tr><td>….</td><td>….</td></tr>
<tr><td>0x3F</td><td>63</td></tr>
</table></td></tr>
</table>

Note: The reserved bits clamp.15, clamp.14, clamp.7 and clamp.6 can be written and read to/from the block E2P. The copy process copies only bits (clamp.13 down to clamp.8) and (clamp.5 down to clamp.0) to the SWR.

1.4.1. Clamping Example

Clamps (applicable for Analog (ZMID5201) and PWM (ZMID5202), not for SENT (ZMID5203)).

Clamp_low (6 bits): min value is 5%, steps of 1% of the span from minimum value. Max Clamp_low value is: 68%.

Clamp_high (6 bits): max value is 95%, steps of -1% of the span from max value. Min Clamp_high value is: 32%.

In the below example the clamping levels are 5% and 95%.

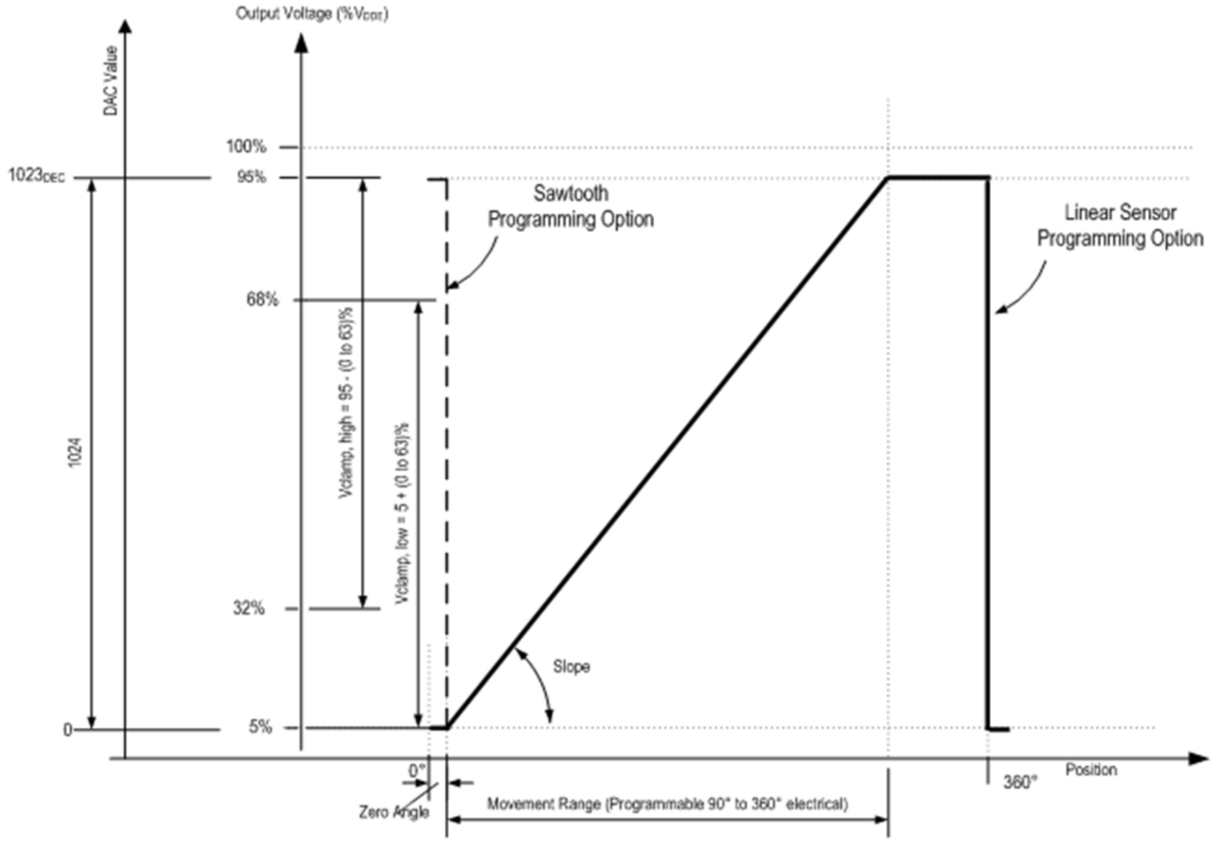

Figure 3. Clamping Example

1.5 LinInt0

Address of register: 0x03.

Default value: 0x0000.

The linearity of the position transfer function can be modified by a 9-point correction curve over the whole position range. The correction curve is defined by 9 points: corr0....corr8. The correction factor can be calculated by a linear interpolation over the 9 corresponding points. The correction factor is applied on the 11 most significant position bits.

Table 6. LinInt0 Register Description

<table>
<tr><th>Bits</th><th>Symbol</th><th>Description</th></tr>
<tr><td>linint0.15 - linint0.8</td><td>corr1</td><td>Correction factor 1 for position 12.5% (45 deg).
<table>
<tr><th>Corr0 (linint7 - linint0)</th><th>Correction Factor</th></tr>
<tr><td>0x00</td><td>0</td></tr>
<tr><td>0x01</td><td>1</td></tr>
<tr><td>….</td><td>….</td></tr>
<tr><td>….</td><td>….</td></tr>
<tr><td>….</td><td>….</td></tr>
<tr><td>0x7F</td><td>127</td></tr>
<tr><td>0x10</td><td>-0</td></tr>
<tr><td>0x11</td><td>-1</td></tr>
<tr><td>….</td><td>….</td></tr>
<tr><td>….</td><td>….</td></tr>
<tr><td>….</td><td>….</td></tr>
<tr><td>0xFF</td><td>-127</td></tr>
</table></td></tr>
</table>

Bits	Symbol	Description	
Linint0.7 -linint0.0	corr0	Correction factor 0 for position 0% (0 deg)	
		Corr0 (linint7 - linint0)	**Correction Factor**
		0x00	0
		0x01	1
		….	….
		….	….
		….	….
		0x7F	127
		0x10	-0
		0x11	-1
		….	….
		….	….
		….	….
		0xFF	-127

Note: The notation of the correction factor is sign & abs. with a range of +127...+-0.....-127.

1.5.1. Linear Error Correction

The linear error correction function has 9 equidistant fixed correction points (one dimensional). Between each pair of grid points a linear interpolation function evaluates the correction factor.

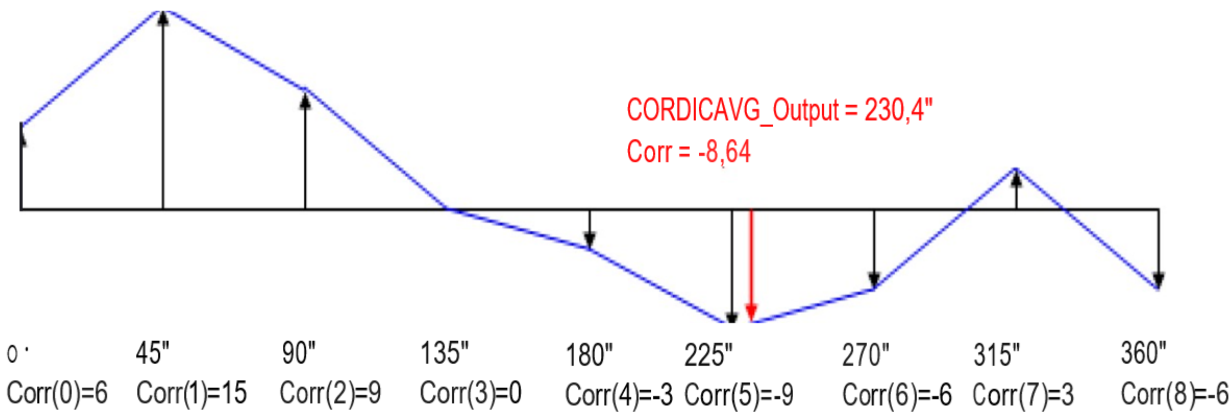

Figure 4. Linear Error Correction Example

1.6 LinInt1

Address of register: 0x04.

Default value: 0x0000.

The linearity of the position transfer function can be modified by a correction curve over the whole position range. The correction curve is defined by 9 points: corr0....corr8. The correction factor can be calculated by a linear interpolation over the 9 corresponding points. The correction factor is applied on the 11 most significant position bits.

Table 7. LinInt1 Register Description

Bits	Symbol	Description	
Linint1.15 - linint1.8	Corr3	Correction factor 3 for position 37.5% (135 deg).	
		Corr3 (linint15 - linint8)	**Correction Factor**
		0x00	0
		0x01	1
		….	….
		….	….
		….	….
		0x7F	127
		0x10	-0
		0x11	-1
		….	….
		….	….
		….	….
		0xFF	-127
Linint1.7 - linint1.0	Corr2	Correction factor 2 for position 25% (90 deg).	
		Corr2 (linint7 - linint0)	**Correction Factor**
		0x00	0
		0x01	1
		….	….
		….	….
		….	….
		0x7F	127
		0x10	-0
		0x11	-1
		….	….
		….	….
		….	….
		0xFF	-127

Note: The notation of the correction factor is sign & abs. with a range of +127...+- 0.....-127.

1.7 LinInt2

Address of register: 0x05.

Default value: 0x0000.

The linearity of the position transfer function can be modified by a correction curve over the whole position range. The correction curve is defined by 9 points: corr0....corr8. The correction factor can be calculated by a linear interpolation over the 9 corresponding points. The correction factor is applied on the 11 most significant position bits.

Table 8. LinInt2 Register Description

<table>
<tr><th>Bits</th><th>Symbol</th><th>Description</th></tr>
<tr><td>Linint2.15 - linint2.8</td><td>Corr5</td><td>Correction factor 5 for position 62.5% (225 deg).
<table>
<tr><th>Corr5 (linint15 - linint8)</th><th>Correction Factor</th></tr>
<tr><td>0x00</td><td>0</td></tr>
<tr><td>0x01</td><td>1</td></tr>
<tr><td>….</td><td>….</td></tr>
<tr><td>….</td><td>….</td></tr>
<tr><td>….</td><td>….</td></tr>
<tr><td>0x7F</td><td>127</td></tr>
<tr><td>0x10</td><td>-0</td></tr>
<tr><td>0x11</td><td>…</td></tr>
<tr><td>….</td><td>….</td></tr>
<tr><td>….</td><td>….</td></tr>
<tr><td>….</td><td>….</td></tr>
<tr><td>0xFF</td><td>-127</td></tr>
</table></td></tr>
<tr><td>Linint2.7 - linint2.0</td><td>Corr4</td><td>Correction factor 4 for position 50% (180 deg).
<table>
<tr><th>Corr4 (linint7 - linint0)</th><th>Correction Factor</th></tr>
<tr><td>0x00</td><td>0</td></tr>
<tr><td>0x01</td><td>1</td></tr>
<tr><td>….</td><td>….</td></tr>
<tr><td>….</td><td>….</td></tr>
<tr><td>….</td><td>….</td></tr>
<tr><td>0x7F</td><td>127</td></tr>
<tr><td>0x10</td><td>-0</td></tr>
<tr><td>0x11</td><td>…</td></tr>
<tr><td>….</td><td>….</td></tr>
<tr><td>….</td><td>….</td></tr>
<tr><td>….</td><td>….</td></tr>
<tr><td>0xFF</td><td>-127</td></tr>
</table></td></tr>
</table>

Note: The notation of the correction factor is sign & abs. with a range of +127 ... +- 0.....-127.

1.8 LinInt3

Address of register: 0x06.

Default value: 0x0000.

The linearity of the position transfer function can be modified by a correction curve over the whole position range. The correction curve is defined by 9 points: corr0....corr8. The correction factor can be calculated by a linear interpolation over the 9 corresponding points. The correction factor is applied on the 11 most significant position bits.

Table 9. LinInt3 Register Description

<table>
<tr><th>Bits</th><th>Symbol</th><th>Description</th></tr>
<tr><td>Linint3.15 - linint3.8</td><td>Corr7</td><td>Correction factor 7 for position 87.5% (315deg).
<table>
<tr><th>Corr7 (linint3.15 - linint3.8)</th><th>Correction Factor</th></tr>
<tr><td>0x00</td><td>0</td></tr>
<tr><td>0x01</td><td>1</td></tr>
<tr><td>….</td><td>….</td></tr>
<tr><td>….</td><td>….</td></tr>
<tr><td>….</td><td>….</td></tr>
<tr><td>0x7F</td><td>127</td></tr>
<tr><td>0x10</td><td>-0</td></tr>
<tr><td>0x11</td><td>-1</td></tr>
<tr><td>….</td><td>….</td></tr>
<tr><td>….</td><td>….</td></tr>
<tr><td>….</td><td>….</td></tr>
<tr><td>0xFF</td><td>-127</td></tr>
</table></td></tr>
<tr><td>Linint3.7 - linint3.0</td><td>Corr6</td><td>Correction factor 6 for position 75% (270deg).
<table>
<tr><th>Corr6 (linint3.7 - linint3.0)</th><th>Correction Factor</th></tr>
<tr><td>0x00</td><td>0</td></tr>
<tr><td>0x01</td><td>1</td></tr>
<tr><td>….</td><td>….</td></tr>
<tr><td>….</td><td>….</td></tr>
<tr><td>….</td><td>….</td></tr>
<tr><td>0x7F</td><td>127</td></tr>
<tr><td>0x10</td><td>-0</td></tr>
<tr><td>0x11</td><td>-1</td></tr>
<tr><td>….</td><td>….</td></tr>
<tr><td>….</td><td>….</td></tr>
<tr><td>….</td><td>….</td></tr>
<tr><td>0xFF</td><td>-127</td></tr>
</table></td></tr>
</table>

Note: The notation of the correction factor is sign & abs. with a range of +127 ... +- 0..... -127.

1.9 LinInt4

Address of register: 0x07.

Default value: 0x0000.

The linearity of the position transfer function can be modified by a correction curve over the whole position range. The correction curve is defined by 9 points: corr0....corr8. The correction factor can be calculated by a linear interpolation over the 9 corresponding points. The correction factor is applied on the 11 most significant position bits.

Table 10. LinInt4 Register Description

Bits	Symbol	Description
Linint4.15 - linint4.8	Reserved	Not used, read as 0 (SWR)

<table>
<tr><th>Bits</th><th>Symbol</th><th>Description</th></tr>
<tr><td>Linint4.7 - linint4.0</td><td>Corr8</td><td>Correction factor 8 for position 100% (360deg)
<table>
<tr><th>Corr8 (linint4.15 - linint4.8)</th><th>Correction Factor</th></tr>
<tr><td>0x00</td><td>0</td></tr>
<tr><td>0x01</td><td>1</td></tr>
<tr><td>….</td><td>….</td></tr>
<tr><td>….</td><td>….</td></tr>
<tr><td>….</td><td>….</td></tr>
<tr><td>0x7F</td><td>127</td></tr>
<tr><td>0x10</td><td>-0</td></tr>
<tr><td>0x11</td><td>-1</td></tr>
<tr><td>….</td><td>….</td></tr>
<tr><td>….</td><td>….</td></tr>
<tr><td>….</td><td>….</td></tr>
<tr><td>0xFF</td><td>-127</td></tr>
</table>
</td></tr>
</table>

Note: The notation of the correction factor is sign & abs. with a range of +127 ...+-0.....-127.

1.10 Coil Offset

Address of register: 0x08.

Default value: 0x0000.

The defined register offset values are added/ subtracted to/from the amplitude values (13-bit) of the receiver coil R2 and coil R1 values. When using the signal offset compensation the automated gain control (AGC1) must be switched off. (agc_mode = 0b00 => Automatic gain OFF, integration time adaption OFF).

Table 11. Amplitude Offset Register Description

<table>
<tr><th>Bits</th><th>Symbol</th><th>Description</th></tr>
<tr><td>amp.15</td><td>mult_r1</td><td>Multiplication factor for amplitude offset_r1
<table>
<tr><th>mult_r1 (amp.15)</th><th>Multiplication Factor</th></tr>
<tr><td>0b0</td><td>2</td></tr>
<tr><td>0b1</td><td>4</td></tr>
</table>
</td></tr>
<tr><td>amp.14 - amp.8</td><td>offset_r1</td><td>Offset value which is added/subtracted to/from receiver coil R1 amplitude
<table>
<tr><th>mult_r1</th><th>offset_r1</th><th>Correction Factor (Decimal)</th></tr>
<tr><td rowspan="4">0b0</td><td>0b0111111</td><td>Ycosine + 126</td></tr>
<tr><td>0b0000000</td><td>Ycosine + 0</td></tr>
<tr><td>0b1000000</td><td>Ycosine - 0</td></tr>
<tr><td>0b1111111</td><td>Ycosine - 126</td></tr>
<tr><td rowspan="4">0b1</td><td>0b0111111</td><td>Ycosine + 252</td></tr>
<tr><td>0b0000000</td><td>Ycosine + 0</td></tr>
<tr><td>0b1000000</td><td>Ycosine - 0</td></tr>
<tr><td>0b1111111</td><td>Ycosine - 252</td></tr>
</table>
</td></tr>
<tr><td>amp.7</td><td>mult_r2</td><td>Multiplication factor for offset_r2
<table>
<tr><th>mult_r2 (amp.7)</th><th>Multiplication Factor</th></tr>
<tr><td>0b0</td><td>2</td></tr>
<tr><td>0b1</td><td>4</td></tr>
</table>
</td></tr>
<tr><td>amp.6 - amp.0</td><td>offset_r2</td><td>Offset value which is added/subtracted to/from receiver coil R2 amplitude.
<table>
<tr><th>mult_r2</th><th>offset_r2</th><th>Correction Factor (Decimal)</th></tr>
<tr><td rowspan="4">0b0</td><td>0b0111111</td><td>Xsine + 126</td></tr>
<tr><td>0b0000000</td><td>Xsine + 0</td></tr>
<tr><td>0b1000000</td><td>Xsine - 0</td></tr>
<tr><td>0b1111111</td><td>Xsine - 126</td></tr>
<tr><td rowspan="4">0b1</td><td>0b0111111</td><td>Xsine + 252</td></tr>
<tr><td>0b0000000</td><td>Xsine + 0</td></tr>
<tr><td>0b1000000</td><td>Xsine - 0</td></tr>
<tr><td>0b1111111</td><td>Xsine - 252</td></tr>
</table>
</td></tr>
</table>

Note: abs (Xsine + offset_r2) exceeds max.value of 0x1FFF → amplitude DSP overflow alarm is asserted.

1.11 CalMode

Address of register: 0x09.

Default value: 0x0000.

The calibration mode register contains some control bits which configure the calibration mode and evaluation of the correction curve.

Table 12. CalMode Register Description

<table>
<tr><th>Bits</th><th>Symbol</th><th>Description</th></tr>
<tr><td>calmod.15 - calmod.13</td><td>Reserved</td><td>Not used, read as 0 (SWR)</td></tr>
<tr><td>calmod.12</td><td>out_mod</td><td>Output Mode<table><tr><th>Out_mod</th><th>Output Mode</th></tr><tr><td>0b0</td><td>Linear</td></tr><tr><td>0b1</td><td>Modulo360</td></tr></table></td></tr>
<tr><td>calmod.11 – calmod.9</td><td>Reserved</td><td>Not used, read as 0 (SWR)</td></tr>
<tr><td>calmod.8</td><td>corr_mod</td><td>Correction Mode.
Defines how the correction curve has to be applied to correct the linearity of the output transfer function.<table><tr><th>Corr_mod</th><th>Correction Mode</th></tr><tr><td>0b0</td><td>Linear error correction pre-calibration</td></tr><tr><td>0b1</td><td>Linear error correction post-calibration</td></tr></table></td></tr>
<tr><td>calmod.7 – calmod.5</td><td>Reserved</td><td>Not used, read as 0 (SWR)</td></tr>
<tr><td>calmod.4</td><td>angle_offset</td><td>Linearization angle offset.
If (angle_offset) = 1, -22,5° offset is added to the CORDIC calculation only in the case of an Interpolation correction before the Slope calibration (Corr_MOD) = 0<table><tr><th>Angle_offset</th><th>Angle Offset in Degree</th></tr><tr><td>0b0</td><td>0</td></tr><tr><td>0b1</td><td>-22.5</td></tr></table></td></tr>
<tr><td>calmod.3</td><td>swap_rc_pol</td><td>Testing bits for Renesas</td></tr>
<tr><td>calmod.2</td><td>swap_rc_amp</td><td>Testing bits for Renesas</td></tr>
<tr><td>calmod.1</td><td>invppr2</td><td>Testing bits for Renesas</td></tr>
<tr><td>calmod.0</td><td>invppr1</td><td>Testing bits for Renesas</td></tr>
</table>

1.11.1. Output Mode

Linear (Out_Mod = 0): Linear Output Mode is a non-repeating output mode in which the sensor output signal is clamped at the mechanical end points with a range of -1260° ... + 1620°.

Modulo 360 (Out_Mod = 1): The Modulo 360 Output (Sawtooth Output) Mode is a repeating output mode in which the sensor output signal is not clamped at the mechanical end points, but is switched back to its origin with a range between 0° to 360°.

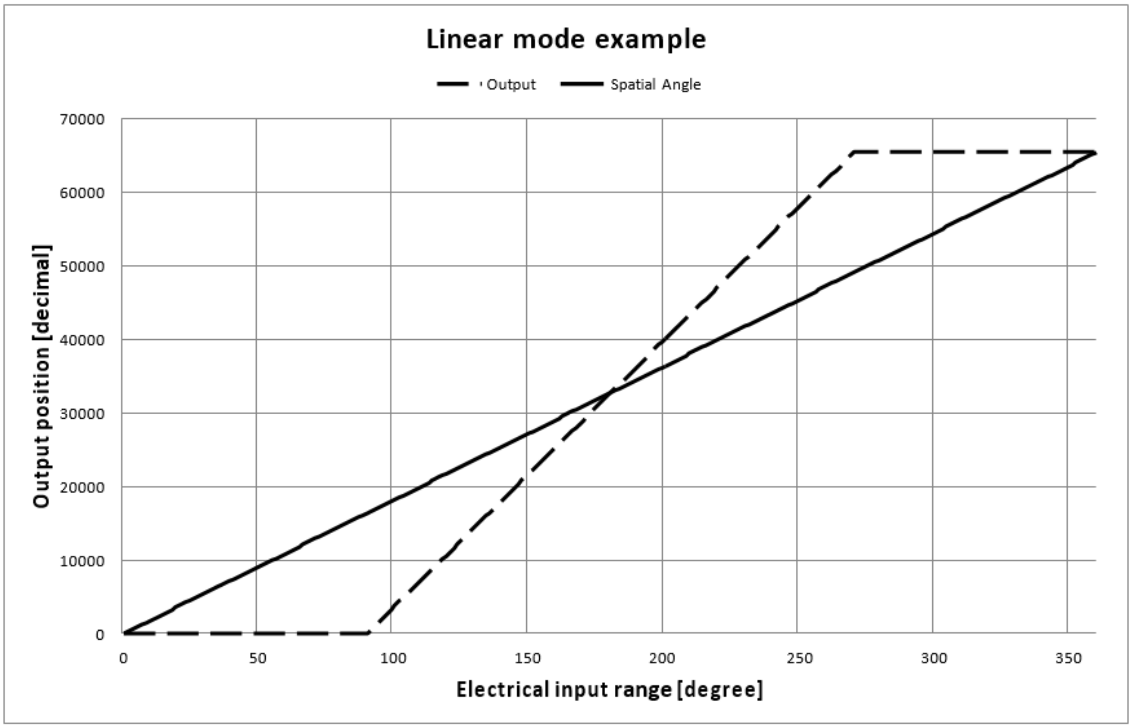

Figure 5. Linear Output Mode Example with Slope = 2, Offset = 90°

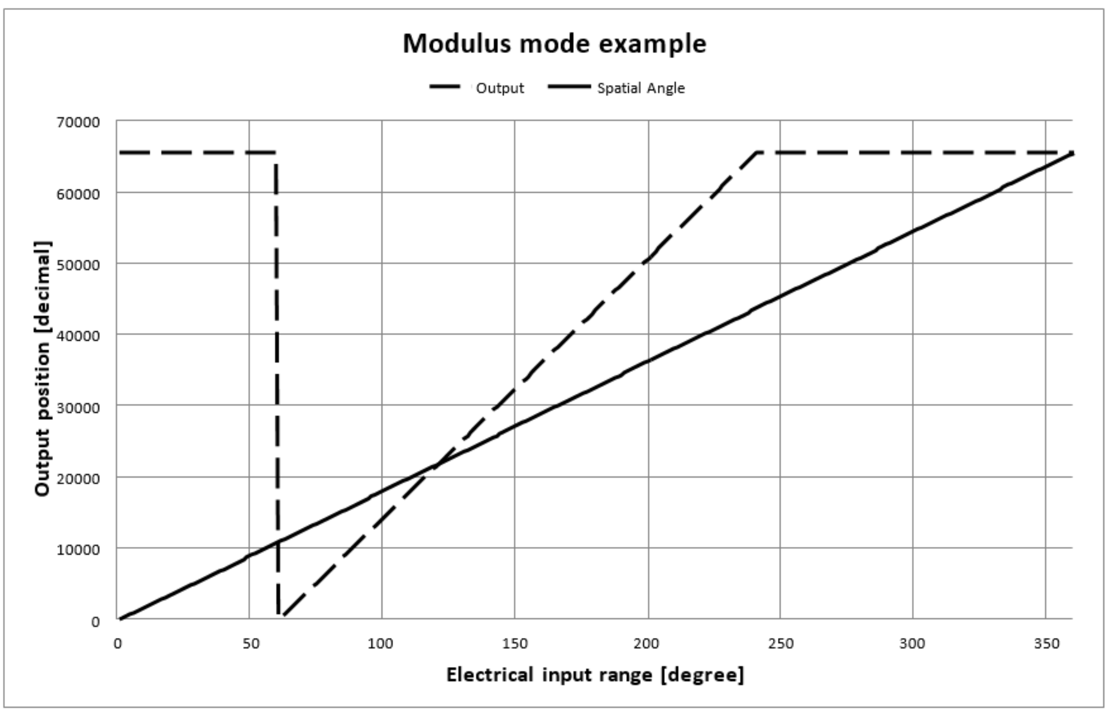

Figure 6. Modulus Output Example with Slope = 2, Offset = 60°

1.11.2. Correction Mode

Pre Calibration: if (Corr_MOD) = 0 then linearity correction is done before "Slope & Offset".

The pre-calibration should be used if the electric input covers a range of a 360°. Using pre-calibration is an advantaged when slope and offset needs to be changed after linearization.

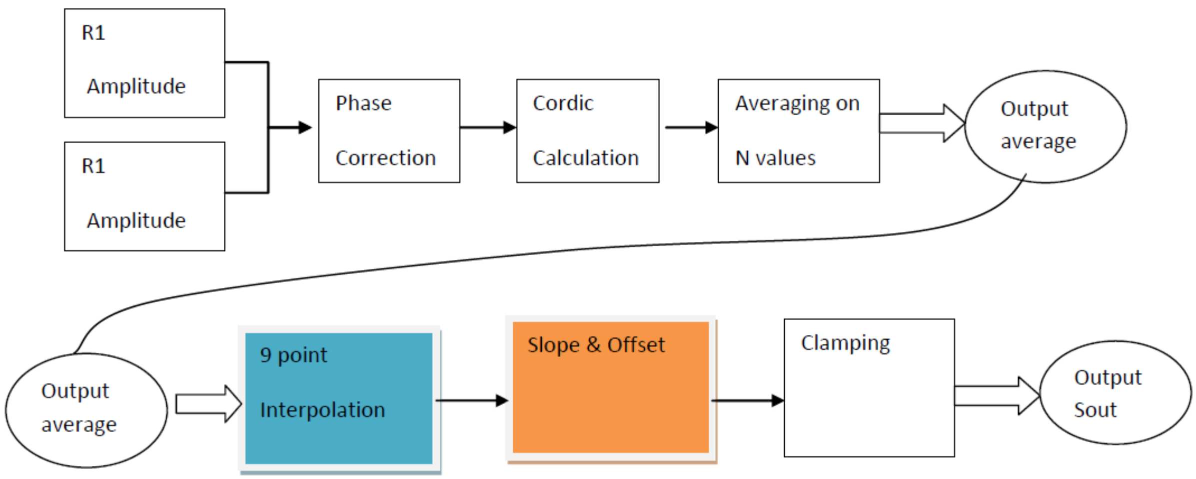

Figure 7. Pre-Calibration Process

Post Calibration; if (Corr_MOD) = 1 then linearity correction is done after " Slope & Offset ". The post-calibration should be the default standard type of calibration.

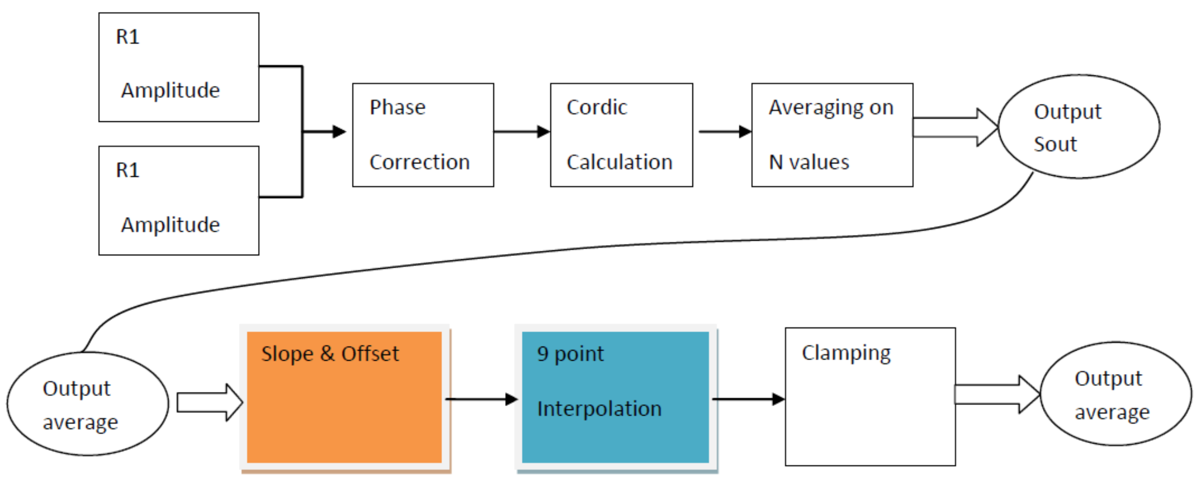

Figure 8. Post-Calibration Process

Note: The reserved bits can be written and read to/from the block E2P. The copy process copies only bits (calmod.12, calmod.8, calmod.4, calout1 and calmod.0) to the SWR.

Note: Individual swapping of receiver polarity & amplitude is only for testing purpose. For application mode both control bits have to be set 0b1 respectively 0b0.

1.12 Output

Address of register: 0x0A Default value: 0x0800

The output register configuration.

Table 13. Output Register Description

<table>
<tr><th>Bits</th><th>Symbol</th><th>Description</th></tr>
<tr><td>out.15</td><td>Reserved</td><td>Not used, read as 0 (SWR)</td></tr>
<tr><td>output.14</td><td>sent_crc</td><td>Only for ZMID5203
SENT CRC
The SENT CRC bit switched between CRC calculation according Legacy implementation of SAE J 2716.
<table><tr><th>SENT CRC</th><th>CRC Calculation</th></tr><tr><td>0b0</td><td>CRC calculation according rev. Feb 2008</td></tr><tr><td>0b1</td><td>CRC calculation according SAE J 2716, Rev 3</td></tr></table></td></tr>
<tr><td>output.13</td><td>sent_pause</td><td>Only for ZMID5203
SENT Pause
The sent pause bit switches between a constant SENT frame length according SAE J 2716 rev3 by including a pause pulse and a variable SENRT frame length according rev2.
<table><tr><th>Sent_pause</th><th>Frame Length</th></tr><tr><td>0b0</td><td>SENT frame according to SAE J 2716 Rev.2</td></tr><tr><td>0b1</td><td>SENT frame length according to SAE J 2716, Rev3.</td></tr></table></td></tr>
<tr><td>output.12</td><td>sent_ssn</td><td>Only for ZMID5203 SENT SSN
The sensor payload is transferred by the 3 data nibbles of signal1. The payload structure of signal2 depends on the SENT single secure nibble bit.
<table><tr><th>SENT SSN</th><th>Frame Length</th></tr><tr><td>0b0</td><td>nibble #4, #5, #6 set to zero</td></tr><tr><td>0b1</td><td>nibble #4 & nibble #5 = value of 8-bit
rolling counter with rollover back to zero.nibble #6 = inverted copy of nibble #1.</td></tr></table></td></tr>
<tr><td>output.11 - output.8</td><td>pwm_slope_curr</td><td>Only for ZMID5202
PWM slope current
The fall time of the PWM output signal is controlled by several current sources related to a master current source. The current of the master source can be programmed.
<table><tr><th>Pwm_slope_curr</th><th>PWM Slope Current</th></tr><tr><td>0x0</td><td>Minimum</td></tr><tr><td>0xF</td><td>Maximum</td></tr></table></td></tr>
<tr><td>output.7</td><td></td><td>Not Used, read as 0</td></tr>
<tr><td>output.6 - output.4</td><td>pwm_freq</td><td>Only for ZMID5202 PWM frequency
<table><tr><th>Pwm_freq</th><th>PWM Frequency (Hz)</th></tr><tr><td>0b000</td><td>2023</td></tr><tr><td>0b001</td><td>1517</td></tr><tr><td>0b010</td><td>1214</td></tr><tr><td>0b011</td><td>1011</td></tr><tr><td>0b100</td><td>758</td></tr><tr><td>0b101</td><td>506</td></tr><tr><td>0b110</td><td>253</td></tr><tr><td>0b111</td><td>126</td></tr></table></td></tr>
<tr><td>output.3</td><td>pwm_diag</td><td>Only for ZMID5202
The output protocol PWM allows two PPR for the diagnostic flag: low or high. The bit allows to select one of the two levels if diagnostic alarm is asserted.
<table><tr><th>pwm_diag</th><th>Diagnostic Level</th></tr><tr><td>0b0</td><td>Low, PPR= 2.5%</td></tr><tr><td>0b1</td><td>High, PPR= 97.5%</td></tr></table></td></tr>
</table>

Bits	Symbol	Description	
output.2	ana_diag	Only for ZMID5201 ANALOG diagnostic level The output protocol ANALOG allows two voltage ranges for the diagnostic flag: low or high. The bit allows to select one of the two levels if diagnostic alarm is asserted.	
		ana_diag	**Diagnostic Level**
		0b0	Low, SOUT voltage from 0V to 4% of VDD
		0b1	High, SOUT voltage from 96 % VDD to 100% VDD
output.1- output.0	reserved	Renesas internal	

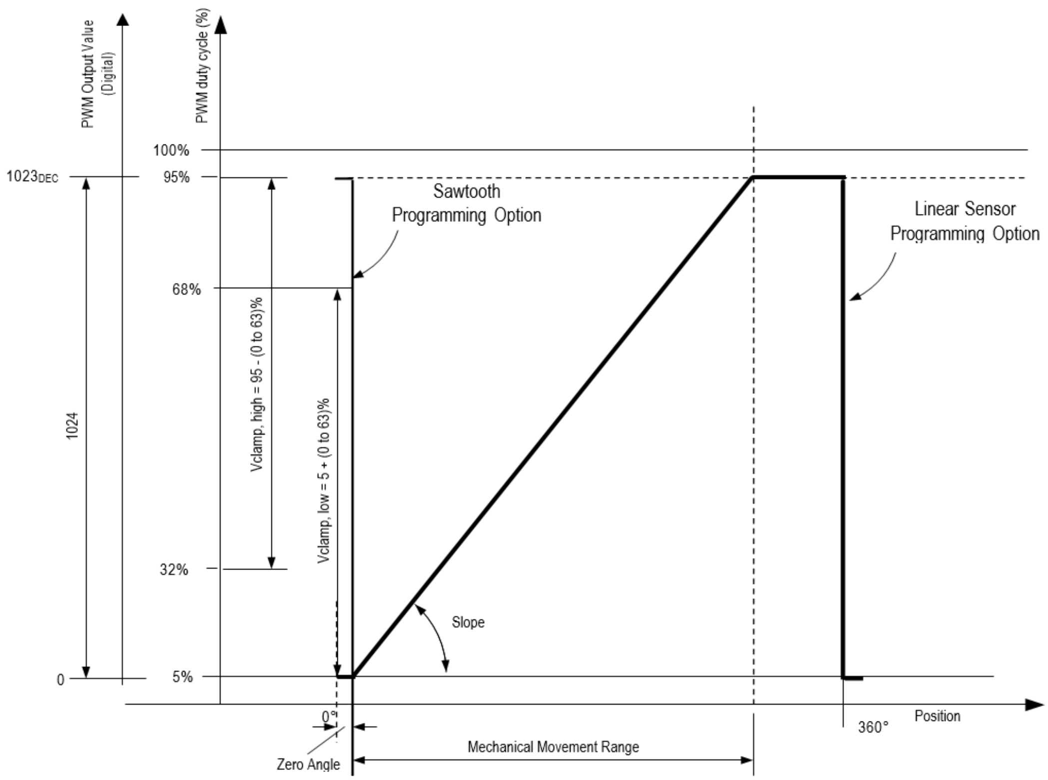

Figure 9. Output PWM Diagnostic Level

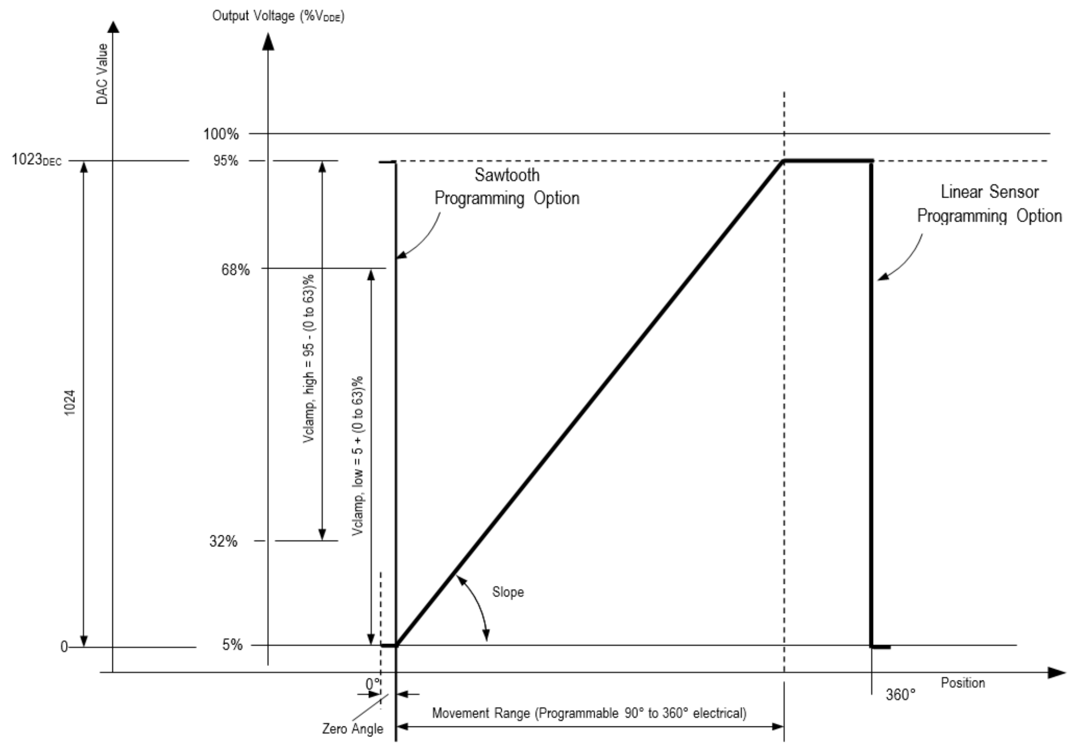

Figure 10. Output Analog Diagnostic Level

Note: The reserved bits can be written and read to/from the block E2P. The copy process copies only defined bits to the SWR.

Note: PWM & SENT timing parameters are based on the ZMID520X internal oscillator period. To fulfill the electrical specification the oscillator has to be calibrated to 16MHz (see 1.14).

1.13 Trimming

Address of register: 0x0B Default value: 0x8107

Trimming and OSR

The Trimming parameters controls the Ic current and the vddt voltage regulator. The OSR parameter defines the decimation of ADC samples for calculating the position processing update rate.

Table 14. Trim0 Register Description

<table>
<tr><th>Bits</th><th>Symbol</th><th>Description</th></tr>
<tr><td>trim0.15 - trim0.14</td><td>pwm_slope_time</td><td>PWM slope time
The fall time of the PWM output signal is controlled by current sources. The current sources are switched on in 5 consecutive steps. The time between the steps is defined by the pwm_slope_time parameter.
pwm_slope_time= 0b00. 435ns / step pwm_slope_time= 0b01.580ns / step</td></tr>
<tr><td>trim0.13 - tirm0.12</td><td>osr</td><td>Oversampling Rate
The oversampling rate defines the number of samples per receive channel which are accumulated and used for the PPU.
<table><tr><th>OSR</th><th>Samples/Channel</th></tr><tr><td>0b00</td><td>4</td></tr><tr><td>0b01</td><td>8</td></tr><tr><td>0b10</td><td>16</td></tr><tr><td>0b11</td><td>32</td></tr></table></td></tr>
<tr><td>trim0.11 - trim0.9</td><td>Reserved</td><td>Not used, read as 0 (SWR)</td></tr>
</table>

<table>
<tr><th>Bits</th><th>Symbol</th><th>Description</th></tr>
<tr><td>trim0.8 - trim0.4</td><td>lc_cal</td><td>LC Oscillator Calibration (excitation coil)
<table>
<tr><th>lc_cal</th><th>Current (Excitation Coil)</th></tr>
<tr><td>0b0.0000</td><td>Min (0 mA)</td></tr>
<tr><td>0b1.1111</td><td>Max (15 mA)</td></tr>
</table></td></tr>
<tr><td>trim0.3</td><td>Reserved</td><td>Not used, read as 0 (SWR)</td></tr>
<tr><td>trim0.2 - trim0.0</td><td>vddt_trim</td><td>Renesas internal parameter for testing</td></tr>
</table>

1.14 AGC0

Address of register: 0x0C Default value: 0x0836

Basic configurations of the analog front end (R1/2 input receive path) gain regulation are controlled by the AGC register. The incoming time division multiplexed signals are amplified by the integrator and the S&H circuit (Figure 6). Both parameters 'ext' and 'gain' will modify the amplification factor of the sampled signals.

The parameter 'smpl_cycle' is a 'timing-factor' in number of sample periods for the adaptive gain regulation to determine the point time for gain / integration time setting. A change of the smpl_cycle parameter should only be done in dependency of the OSR parameter.

Parameter smp_cycle zero indexed: smpl_cycle = 0 .1st sample. smpl_cycle = 1 .2nd sample.

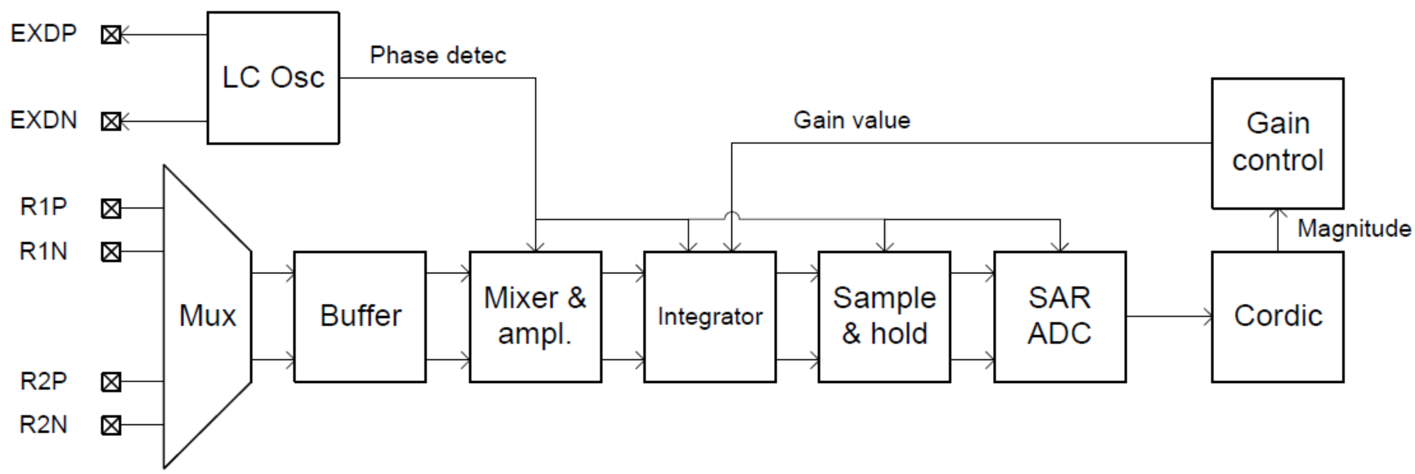

Figure 11. Gain Control

Table 15. AGC0 Register Description

<table>
<tr><th>Bits</th><th>Symbol</th><th>Description</th></tr>
<tr><td>agc0.15</td><td>Reserved</td><td>Not used, read as 0 (SWR)</td></tr>
<tr><td>agc0.14 - agc0.9</td><td>smpl_cycle</td><td>The OSR and the smpl_cycle are dependent on each other. Whenever the OSR is changed, the smpl_cycle must be changed accordingly.
<table>
<tr><th>OSR</th><th>Samples/Channel</th><th>2 × Channel</th><th>Recommended smpl_cycle Setting</th></tr>
<tr><td>0b00</td><td>4</td><td>8</td><td>0b00.0100</td></tr>
<tr><td>0b01</td><td>8</td><td>16</td><td>0b00.1100</td></tr>
<tr><td>0b10</td><td>16</td><td>32</td><td>0b01.1100</td></tr>
<tr><td>0b11</td><td>32</td><td>64</td><td>0b11.1100</td></tr>
</table></td></tr>
</table>

<table>
<tr><th>Bits</th><th>Symbol</th><th>Description</th></tr>
<tr><td>agc0.8 -agc0.4</td><td>ext</td><td>Extend integration cycle related to excitation clock period
Effective integration time = (7 + ext) x lc_period
<table>
<tr><th>ext</th><th>Integrator Time</th></tr>
<tr><td>0b00000</td><td>(7 + 0) x lc_period</td></tr>
<tr><td>0b00001</td><td>(7 + 1) x lc_period</td></tr>
<tr><td>0b00010</td><td>(7 + 2) x lc_period</td></tr>
<tr><td>0b00011</td><td>(7 + 3) x lc_period</td></tr>
<tr><td>…</td><td></td></tr>
<tr><td>…</td><td></td></tr>
<tr><td>0b11111</td><td>(7 + 31) x lc_period</td></tr>
</table></td></tr>
<tr><td>agc0.3 - agc0.0</td><td>gain_stage</td><td>Integrator gain stage
<table>
<tr><th>Gain_stage</th><th>Integrator Gain Stage</th></tr>
<tr><td>0x0</td><td>Minimum gain</td></tr>
<tr><td>…</td><td>…</td></tr>
<tr><td>…</td><td>…</td></tr>
<tr><td>0xC</td><td>Maximum gain</td></tr>
<tr><td>…</td><td>Maximum gain</td></tr>
<tr><td>…</td><td>Maximum gain</td></tr>
<tr><td>0xF</td><td>Maximum gain</td></tr>
</table>
<table>
<tr><th>AGC Mode (AGC1.13, AGC1.12) in AGC1</th><th>Intergrator Gain</th></tr>
<tr><td>Gain regulation OFF (0b00, 0b01)</td><td>Fixed gain stage setting.</td></tr>
<tr><td>Gain regulation ON (0b10)</td><td>Maximum gain stage value for gain regulation. This is limiting the gain regulation. It clamps the upper gain stage value. First applicable value for AGC is fixed 0x3.</td></tr>
<tr><td>Integrator time adaptation and gain stage adaptation on (0b11)</td><td>Maximum gain stage value for gain regulation. This is limiting the gain regulation. It clamps the upper gain stage value. After start-up Integration Tim adaptation is active with gain stage 0x6. Consecutive gains target adaptation starts with gain stage 0x3.</td></tr>
</table></td></tr>
</table>

1.15 AGC1

Address of register: 0x0D Default value: 0x0255.

Automatic Gain Control.

Table 16. AGC1 Register Description

<table>
<tr><th>Bits</th><th>Symbol</th><th>Description</th></tr>
<tr><td>agc1.15</td><td>agc_suppress</td><td>Renesas internal</td></tr>
<tr><td>agc1.14</td><td>agc_interlink</td><td>Renesas internal</td></tr>
<tr><td>agc1.13 - agc1.12</td><td>agc_mode</td><td>Extend integration cycle related to excitation clock period effective integration time = (7 + ext) x lc_period.
<table>
<tr><th>Agc_mode</th><th>Automatic Gain</th><th>Integration Gain Adaptation</th></tr>
<tr><td>0b00</td><td>Off</td><td>Off</td></tr>
<tr><td>0b01</td><td>Off</td><td>On</td></tr>
<tr><td>0b10</td><td>On</td><td>Off</td></tr>
<tr><td>0b11</td><td>On</td><td>On</td></tr>
</table></td></tr>
</table>

<table>
<tr><th>Bits</th><th>Symbol</th><th>Description</th></tr>
<tr><td>agc1.11 - agc1.10</td><td>exc_freq_high</td><td>High limit for excitation coil frequency range alarm.
<table>
<tr><th>Exc_freq_high</th><th>Excitation Coil Frequency [MHz]</th></tr>
<tr><td>0b00</td><td>6.0</td></tr>
<tr><td>0b01</td><td>6.5</td></tr>
<tr><td>0b10</td><td>7.0</td></tr>
<tr><td>0b11</td><td>8.0</td></tr>
</table>
An additional variance of about +/- 20% has to be taken into account to frequency variation of ZMID502X internal oscillator over temperature and voltage. The measurement time is ~ 100 us.</td></tr>
<tr><td>agc1.9 - agc1.8</td><td>exc_freq_low</td><td>Low limit for excitation coil frequency range alarm.
<table>
<tr><th>Exc_freq_low</th><th>Excitation Coil Frequency [MHz]</th></tr>
<tr><td>0b00</td><td>1.0</td></tr>
<tr><td>0b01</td><td>1.5</td></tr>
<tr><td>0b10</td><td>2.0</td></tr>
<tr><td>0b11</td><td>2.5</td></tr>
</table>
An additional variance of about +/- 20% has to be taken into account to frequency variation of ZMID520X internal oscillator over temperature and voltage. The measurement time is ~ 100 us.</td></tr>
<tr><td>agc1.7</td><td>Reserved</td><td>Not used, read as 0 (SWR).</td></tr>
<tr><td>agc1.6 - agc1.4</td><td>cordmagul</td><td>Cordic magnitude upper level. (100% ....0x34B6......13494d)
<table>
<tr><th>Cordmagul</th><th>Magnitude Upper Level [%]</th></tr>
<tr><td>0b111</td><td>90</td></tr>
<tr><td>0b110</td><td>85</td></tr>
<tr><td>0b101</td><td>80</td></tr>
<tr><td>0b100</td><td>75</td></tr>
<tr><td>0b011</td><td>70</td></tr>
<tr><td>0b010</td><td>65</td></tr>
<tr><td>0b001</td><td>60</td></tr>
<tr><td>0b000</td><td>55</td></tr>
</table></td></tr>
<tr><td>agc1.3</td><td>Reserved</td><td>Not used, read as 0 (SWR).</td></tr>
<tr><td>agc1.2 - agc1.0</td><td>cordmagll</td><td>Cordic magnitude lower level.
<table>
<tr><th>Cordmagll</th><th>Magnitude Lower Level [%]</th></tr>
<tr><td>0b111</td><td>55</td></tr>
<tr><td>0b110</td><td>50</td></tr>
<tr><td>0b101</td><td>45</td></tr>
<tr><td>0b100</td><td>40</td></tr>
<tr><td>0b011</td><td>35</td></tr>
<tr><td>0b010</td><td>30</td></tr>
<tr><td>0b001</td><td>25</td></tr>
<tr><td>0b000</td><td>20</td></tr>
</table></td></tr>
</table>

Notes: The reserved bits can be written and read to/from the block E2P. The copy process copies only defined bits to the SWR. The Cordic magnitude upper level should be higher than the lower level.

1.16 Mask

Address of register: 0x0E Default value: 0xBFFF.

The diagnostic mask, in the case that the output is set in the diagnostic state allows to prevent a diagnostic flag. The status of the latched diagnostic flags can be monitored by reading the diagnostic register.

Table 17. Mask Register Description

<table>
<tr><th>Bits</th><th>Symbol</th><th>Description</th></tr>
<tr><td>mask.15</td><td>agc_low gain</td><td>AGC low gain status
<table>
<tr><th>Agc_low Gain</th><th>AGC Low Gain Alarm</th></tr>
<tr><td>0b0</td><td>Enable</td></tr>
<tr><td>0b1</td><td>Disable</td></tr>
</table></td></tr>
</table>

<table>
<tr><th>Bits</th><th>Symbol</th><th>Description</th></tr>
<tr><td>mask.14</td><td>ee_ded</td><td>EEPROM double error detection<table><tr><th>Ee_ded</th><th>Double Error Alarm</th></tr><tr><td>0b0</td><td>Enable</td></tr><tr><td>0b1</td><td>Disable</td></tr></table></td></tr>
<tr><td>mask.13</td><td>r2_coil_fail</td><td>Receiver coil2 short/open check status<table><tr><th>R2_coil_fail</th><th>Receiver Coil2 Short/Open Check Status</th></tr><tr><td>0b0</td><td>Enable</td></tr><tr><td>0b1</td><td>Disable</td></tr></table></td></tr>
<tr><td>mask.12</td><td>r1_coil_fail</td><td>Receiver coil1 short/open check status<table><tr><th>R1_coil_fail</th><th>Receiver Coil1 Short/Open Check Status</th></tr><tr><td>0b0</td><td>Enable</td></tr><tr><td>0b1</td><td>Disable</td></tr></table></td></tr>
<tr><td>mask.11</td><td>Open</td><td>R1 or R2 receiver coil open<table><tr><th>Open</th><th>R1 or R2 Receiver Coil Open</th></tr><tr><td>0b0</td><td>Enable</td></tr><tr><td>0b1</td><td>Disable</td></tr></table></td></tr>
<tr><td>mask.10</td><td>rc_coil_short</td><td>R1 or R2 receiver coil short<table><tr><th>Rc_coil_short</th><th>R1 or R2 Receiver Coil Short</th></tr><tr><td>0b0</td><td>Enable</td></tr><tr><td>0b1</td><td>Disable</td></tr></table></td></tr>
<tr><td>mask.9</td><td>rc_gnd_short</td><td>R1 or R2 receiver coil short to gnd<table><tr><th>Rc_gnd_short</th><th>R1 or R2 Receiver Coil Short to GND</th></tr><tr><td>0b0</td><td>Enable</td></tr><tr><td>0b1</td><td>Disable</td></tr></table></td></tr>
<tr><td>mask.8</td><td>exc_break_p</td><td><table><tr><th>Excitation Coil Break P
Exc_break_p</th><th>Excitation Coil Break P</th></tr><tr><td>0b0</td><td>Enable</td></tr><tr><td>0b1</td><td>Disable</td></tr></table></td></tr>
<tr><td>mask.7</td><td>exc_break_n</td><td><table><tr><th>Excitation Coil Break N
Exc_break_n</th><th>Excitation Coil Break N</th></tr><tr><td>0b0</td><td>Enable</td></tr><tr><td>0b1</td><td>Disable</td></tr></table></td></tr>
<tr><td>mask.6</td><td>srb_parity</td><td>Shadow Register bank parity<table><tr><th>Srb_pairity</th><th>Shadow Register Bank Parity</th></tr><tr><td>0b0</td><td>Enable</td></tr><tr><td>0b1</td><td>Disable</td></tr></table></td></tr>
<tr><td>mask.5</td><td>adc_dsp_ovfl</td><td>ADC digital signal processing overflow<table><tr><th>Adc_dsp_ovfl</th><th>ADC Digital Signal Processing Overflow (Alarm)</th></tr><tr><td>0b0</td><td>Enable</td></tr><tr><td>0b1</td><td>Disable</td></tr></table></td></tr>
<tr><td>mask.4</td><td>amp_dsp_ovfl</td><td>Amplitude digital signal processing overflow<table><tr><th>Amp_dsp_ovfl</th><th>Amplitude Digital Signal Processing Overflow</th></tr><tr><td>0b0</td><td>Enable</td></tr><tr><td>0b1</td><td>Disable</td></tr></table></td></tr>
<tr><td>mask.3</td><td>lc_osc_fail</td><td>LC oscillator range check<table><tr><th>Lc_osc_fail</th><th>LC Oscillator Range Check</th></tr><tr><td>0b0</td><td>Enable</td></tr><tr><td>0b1</td><td>Disable</td></tr></table></td></tr>
<tr><td>mask.2</td><td>lc_osc_stuck</td><td>LC oscillator stuck check<table><tr><th>Lc_osc_stuck</th><th>LC Oscillator Stuck Check</th></tr><tr><td>0b0</td><td>Enable</td></tr><tr><td>0b1</td><td>Disable</td></tr></table></td></tr>
</table>

<table>
<tr><th>Bits</th><th>Symbol</th><th>Description</th></tr>
<tr><td>mask.1</td><td>mag_low</td><td>Cordic magnitude is below threshold (lower limit, see section 1.15)<table><tr><th>mag_low</th><th>Cordic Magnitude is Below Threshold</th></tr><tr><td>0b0</td><td>Enable</td></tr><tr><td>0b1</td><td>Disable</td></tr></table></td></tr>
<tr><td>mask.0</td><td>mag_high</td><td>Cordic magnitude is above threshold (upper limit, see section 1.15)<table><tr><th>mag_high</th><th>Cordic Magnitude is Above Threshold</th></tr><tr><td>0b0</td><td>Enable</td></tr><tr><td>0b1</td><td>Disable</td></tr></table></td></tr>
</table>

1.17 Traceability0

E2P

Address of register: 0X0F.

Default value: none, read only.

Renesas identification and version number.

Table 18. Traceability0 Register Description

Bits	Symbol	Description
trace0.15 - trace0.0	IDT _id	Renesas Identification and version number.

1.18 Traceability1

E2P

Address of register: 0x10.

Default value: none, read only.

Renesas identification and version number.

Table 19. Traceability1 Register Description

Bits	Symbol	Description
Trace1.15 - Trace1.0	IDT _id	Renesas Identification and version number.

1.19 Misc

Address of register: 0x11.

Default value: 0x00C2.

Table 20. Misc Register Description

<table>
<tr><th>Bits</th><th>Symbol</th><th>Description</th></tr>
<tr><td>misc.15 - misc.9</td><td>IDT</td><td>Renesas internal</td></tr>
<tr><td>misc.8</td><td>agc_offset_sat_mode</td><td>AGC offset saturation mode.
If this mode is activated an offset saturation detection forces the gain regulation to decrement the gain step to decrease the ADC input signal level.<table><tr><th>agc_offset_sat_mode</th><th>AGC Offset Saturation Mode</th></tr><tr><td>0b0</td><td>Extension off</td></tr><tr><td>0b1</td><td>Extension on</td></tr></table></td></tr>
<tr><td>misc.7</td><td>exc_type</td><td>Excitation coil alarm type selection (exc_break_p, exc_break_n)<table><tr><th>exc_type</th><th>Coil Alarm Type Selection</th></tr><tr><td>0b0</td><td>Event alarm type</td></tr><tr><td>0b1</td><td>Latched alarm type</td></tr></table></td></tr>
<tr><td>misc.6- misc.0</td><td>IDT</td><td>Renesas internal</td></tr>
</table>

1.20 Afe_Agc

Address of register: 0x13.

Default value: none, read only.

The integration time regulation adapts the number of integration time cycles that a constant integration time independent of the LC-frequency is achieved. The adjusted cycle number can be monitored by reading the parameter agc_intgr. The automatic gain regulation process (AGC1) modify the gain by a decision circuit which compares the actual cordic magnitude with the programmed cordic magnitude limits. The adjusted gain value can be monitored by reading the register. The phase information is the polarity of the incoming R1/R2 signal respectively the polarity of the decimated samples R1/2.

Table 21. Afe_Agc Register Description

<table>
<tr><th>Bits</th><th>Symbol</th><th>Description</th></tr>
<tr><td>afe_agc.15 -
afe_agc.13</td><td>Reserved</td><td>Not used, read as 0 (SWR).</td></tr>
<tr><td>afe_agc.12 -
afe_agc.8</td><td>agc_intgr</td><td>AGC adjusted number of integration cycles effective integration time = (7 + agc_intgr) x lc clock period.</td></tr>
<tr><td>afe_agc.7 -
afe_agc.4</td><td>agc_gain stage</td><td>AGC adjusted gain stage value range 0x0...0xC.</td></tr>
<tr><td>afe_agc.3</td><td>r1_polarity</td><td>Polarity of receiver coil R1<table><tr><th>R1_polarity</th><th>Polarity of Receiver Coil R1</th></tr><tr><td>0b0</td><td>Negative</td></tr><tr><td>0b1</td><td>Positive</td></tr></table></td></tr>
<tr><td>afe_agc.2</td><td>r2_polarity</td><td>Polarity of receiver coil R2<table><tr><th>R2_polarity</th><th>Polarity of Receiver Coil R2</th></tr><tr><td>0b0</td><td>Negative</td></tr><tr><td>0b1</td><td>Positive</td></tr></table></td></tr>
<tr><td>afe_agc.1</td><td>y_cos_pol</td><td>Phase polarity of Ycosine amplitude parameter. The sensor position is calculated based on the receiver amplitude (see sections 1.21 and 1.22) and related phase polarity.</td></tr>
<tr><td>afe_agc.0</td><td>x_sin_pol</td><td>Phase polarity of Xsine amplitude parameter. The sensor position is calculated based on the receiver amplitude (see sections 1.21 and 1.22) and related phase polarity.</td></tr>
</table>

1.21 Xsine

Address of register: 0x14.

Default value: none, read only.

The amplitude of the receiver coils after decimation and amplitude offset evaluation (sampler output) can be monitored by reading the register Xsine.

Table 22. Xsine Register Description

Bits	Symbol	Description
xsine.15 -xsine.13	Reserved	Not used, read as 0 (SWR).
xsine.12 -xsine.0	x_sin_amp	Amplitude of receiver coil. Absolute amplitude after decimation and amplitude offset evaluation.

1.22 Ycosine

Address of register: 0x15.

Default value: none, read only.

The amplitude of the receiver coil after decimation and amplitude offset evaluation (sampler output) can be monitored by reading the register Ycosine.

Table 23. Ycosine Register Description

Bits	Symbol	Description
xsine.15 -xsine.13	Reserved	Not used, read as 0 (SWR).
xsine.12 –xsine.0	y_cos_amp	Amplitude of receiver coil absolute amplitude after decimation and amplitude offset evaluation.

1.23 Angle

Address of register: 0x16.

Default value: None; read only.

The sensor position is calculated based on the x_sin_amp (see section 1.21) and y_cos_amp (see section 1.22) parameter. The result of 90 degree angle is calculated by arctan $(\frac{x\_sin\_amp}{y\_cos\_amp})$.

The trigonometric function is implemented by an iterative CORDIC (Coordinate Rotation Digital Computer) architecture. The chosen number of iteration steps is 16. CORDIC works by rotating the coordinate system through constant angles until the angle is reduced to zero and the result vector is aligned with the X axis. The result of the vectoring operation is a rotation angle (0deg <= angle <= 90deg) and the scaled magnitude of the original vector. The calculated rotation angle is mapped to a 15-bit vector and can be monitored by the angle register read access.

Table 24. Angle Register Description

<table>
<tr><th>Bits</th><th>Symbol</th><th>Description</th></tr>
<tr><td>angle.15</td><td>Reserved</td><td>Not used, read as 0 (SWR).</td></tr>
<tr><td>angle.14 – angle.0</td><td>cordic angle</td><td>Rotational CORDIC angle from 0 degree to 90 degree.
<table>
<tr><th>Cordic Angle</th><th>Angle [Degree]</th></tr>
<tr><td>0x0000</td><td>0</td></tr>
<tr><td>.......</td><td>.......</td></tr>
<tr><td>0x7FFF</td><td>90</td></tr>
</table></td></tr>
</table>

1.24 Cordic Magnitude

Address of register: 0x17

Default value: None: read only

The CORDIC algorithm in vectoring mode works by seeking to minimize the Ycosine component of the residual vector at each rotation. The result of the vectoring operation is a rotation angle (see section 1.23) and the scaled magnitude of the original vector $\sqrt{Xsine^2 + Ycosine^2}$.

The aggregate constant of all 16 iteration steps resp. the scale factor is $\frac{1}{0.707}$

It follows for the cordic magnitude:

$$\text{Cordic magnitude} = \frac{\sqrt{Xsine^2 + Ycosine^2}}{0.607}$$

Assumption: Saturation of both receiver channels:

$$Xsine = Ycosine = 0x1FFF$$

$$\text{cordic magnitude(sat)} = 0x4A8B$$

Assumption: Signals of both receive channels at ideal amplification (below saturation).

$$Xsine = 0x1FFF\ Ycosine \quad Ycosine = 0x0000$$

$$\text{cordic magnitude(opt)} = 0x34B6$$

Conclusion: The cordic magnitude is a monitor for gain respectively integration time setting. It is important that the magnitude does not exceed the optimum level. Otherwise this will lead to a failure in the position calculation (nonlinearity).

Table 25. Mag Register Description

<table>
<tr><th>Bits</th><th>Symbol</th><th colspan="2">Description</th></tr>
<tr><td>angle.15</td><td>Reserved</td><td colspan="2">Not used, read as 0 (SWR).</td></tr>
<tr><td rowspan="5">angle.14 – angle.0</td><td rowspan="5">cordic angle</td><td colspan="2">Rotational CORDIC magnitude from minimum magnitude saturation.</td></tr>
<tr><th>Cordic Mag</th><th>Magnitude</th></tr>
<tr><td>0x4A8B</td><td>Sat</td></tr>
<tr><td>0x34B6</td><td>Opt</td></tr>
<tr><td>0x0000</td><td>Min</td></tr>
</table>

1.25 SPA

Address of register: 0x18.

Default value: None: read only.

The CORDIC processor output angle is expanded by the phase polarity information (y_cos_pol & x_sin_pol) to a range from 0 deg to 360 deg. The ZMID520X internal notation is a 17-bit vector (4 x angle 15-bit). Due to the 16-bit wide data structure of the OWI interface, the spatial angle vector is truncated to 16 bits (17 down to 1) for the read-access.

Table 26. Spa Register Description

<table>
<tr><th>Bits</th><th>Symbol</th><th colspan="2">Description</th></tr>
<tr><td rowspan="4">spa.15 - spat.0</td><td rowspan="4">spatial angle</td><td colspan="2">Spatial angle
Expanded cordic angle to 360 degree range. The value is before calibration and linear error correction. The ZMID520X internal notation is a 17-bit wide vector. From 0 deg to 360 deg.</td></tr>
<tr><th>Spatial Angle</th><th>Spatial Angle [Degree]</th></tr>
<tr><td>0x0000</td><td>0 min</td></tr>
<tr><td>0xFFFF</td><td>360 max</td></tr>
</table>

Note: Due to the truncation of the spatial angle number range to 16-bit (OWI access), the number range of the cordic angle has to be also truncated by one bit (14 down to 1) for direct comparison of this two parameters.

1.26 Pos0

Address of register: 0x19.

Default value: None: read only.

The spatial angle is modified by the calibration parameter slope & offset (see sections 1.2 and 1.3) and the linearity error correction. The pos0 value is the calculated value with linearity error correction before calibration (see section 1.11, corr_mod = 0).

Table 27. Pos0 Register Description

<table>
<tr><th>Bits</th><th>Symbol</th><th colspan="2">Description</th></tr>
<tr><td rowspan="4">pos0.15 -

pos0.0</td><td rowspan="4">pos_so_corr0</td><td colspan="2">Position before calibration & linearity error correction (linear error correction pre-calibration corr_mode = 0), see section 1.11.</td></tr>
<tr><th>Spatial Angle</th><th>Spatial Angle [Degree]</th></tr>
<tr><td>0x0000</td><td>0</td></tr>
<tr><td>0xFFFF</td><td>360</td></tr>
</table>

1.27 Pos1

Address of register: 0x1A Default value: None: read only.

The spatial angle is modified by the calibration parameter slope & offset (see sections 1.2 and 1.3) and the linearity error correction. The pos1 value is the calculated value with linearity error correction after calibration (see section 1.11, corr_mod = 1).

Table 28. Pos1 Register Description

<table>
<tr><th>Bits</th><th>Symbol</th><th>Description</th></tr>
<tr><td>pos0.15 - pos0.0</td><td>pos_so_corr1</td><td>Position after calibration & linearity error correction (linear error correction post-calibration, corr_mod= 1), see section 1.11.
<table><tr><th>Spatial Angle</th><th>Spatial Angle [Degree]</th></tr><tr><td>0x0000</td><td>0</td></tr><tr><td>0xFFFF</td><td>360</td></tr></table></td></tr>
</table>

Note: For the different output protocols the calculated position is truncated from MSB down to 1/5/7. For the SENT respectively PWM/Analog the remainder is rounded.

Note: If corr_mod = 0b0 (1.10, calout.3) pos_so_corr1 is equal pos_so_corr0 (1.25).

2. Glossary

Acronym	Definition
ADC	Analog Digital Converter
ATE	Automatic Test Equipment
ATPG	Automatic Test Pattern Generation
PPU	Position Processing Unit
E2P	Electrically Erasable Programmable Read Only Memory
ECU	Electronic Control Unit
ECC	Error Correction Code
FEC	Forward Error Correction
GND	Ground
IC	Integrated Circuit
LSB	Least Significant Bit
MSB	Most Significant Bit
OWI	One Wire Interface
OSR	Over Sampling Rate
PPR	Pulse Pause Ratio
SWR	Shadow Word Register bank
TDM	Time Division Multiplexer

3. Revision History

Revision Date	Description of Change
October 04, 2022	Output register descriptions updated in Table 13.
April 20, 2020	Initial release

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