NEC

μPD98413

(NEASCOT-P65)

QUAD 622M ATM/POS SONET FRAMER

Preliminary User's Manual rev0.1

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SUMMARY OF CONTENTS

[MEMO]

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[MEMO]

CHAPTER 1 GENERAL

The μPD98413 is a quad 622Mbits/s SONET STS-12c / SDH STM-4c framer. The μPD98413 performs all functions necessary to insert and extract ATM cells or POS (PPP over SONET) packets into and from SONET/SDH payload. Applications include ATM/IP switches, Routers, and Access concentrators.

1.1 Features

General

- Quad SONET STS-12c / SDH STM-4 (622Mbps) framing function in compliance with ITU-T G.707, ANSI T1.105 and Bellcore GR-253-CORE
- Mapping ATM cell or Packet into SONET/SDH payload
- Generic 32-bit microprocessor interface for device control and status monitoring
- 32-bit 104MHz LVTTL interface to be connected with ATM device (UTOPIA level3) or POS device (POS-PHY level3)
- Four serial 622MHz PECL line interface
- Integrated SERDES, Clock data recovery and Clock synthesis
- Provides loopback functions (line and equipment loopback)
- 1024-byte FIFO for each transmit and receive FIFO
- Provides IEEE 1149.1 JTAG testing
- Industrial temperature range (-40 to 85)
- 576 BGA package and 2.5V power supply

SONET

- Detects LOS, OOF, LOF, Line AIS, Line RDI, LOP, Path AIS, Path RDI (Enhanced and One-bit), Path PLM and Path UNEQ
- Inserts, detects and counts B1, B2, B3, Line REI and Path REI
- Detects signal fail (SF) and signal degrade (SD) conditions
- Provides buffers to transmit and receive the 16 or 64 bytes section trace (J0) and path trace (J1) message, also detects Section TIM and Path TIM
- Provides insertion and extraction registers for APS (K1, K2) byte, also detects PSBF
- Generates and interprets payload pointer
- Inserts and extracts registers of overhead bytes, ex. C2 byte
- Inserts and extracts Section and Line DCCs by serial interface
- Inserts and extracts whole overhead bytes by dedicated interface

ATM

- Detects OCD and LCD
- Provides idle/unassigned cell insertion
- Provides cell delineation from SONET/SDH payload and idle/unassigned cell filtering
- Cell scrambling and descrambling
- HEC generation, detection and correction
- Provides performance counters

  Transmit valid cell, Receive valid cell, Receive idle cell, HEC error correct cell, HEC error drop cell, Receive FIFO overflow drop cell

POS

- PPP/HDLC processing compliant with RFC 2615(1619) and 1662
- Inserts flag sequence between each POS packet
- Provides packet delineation from SONET/SDH payload by detection flag sequence
- Byte stuffing and destuffing
- Generates and checks 32/16-bit FCS
- Data scrambling and descrambling
- Inserts address and control fields and detects address and control error
- Detects minimum and maximum size packet errors
- Provides performance counters

  Transmit valid packet and byte, Transmit abort packet, Transmit FIFO underflow packet, Receive valid packet and byte, Receive abort packet, Receive address error packet, Receive FCS error packet, Receive short packet, Receive long packet, Receive FIFO overflow drop packet

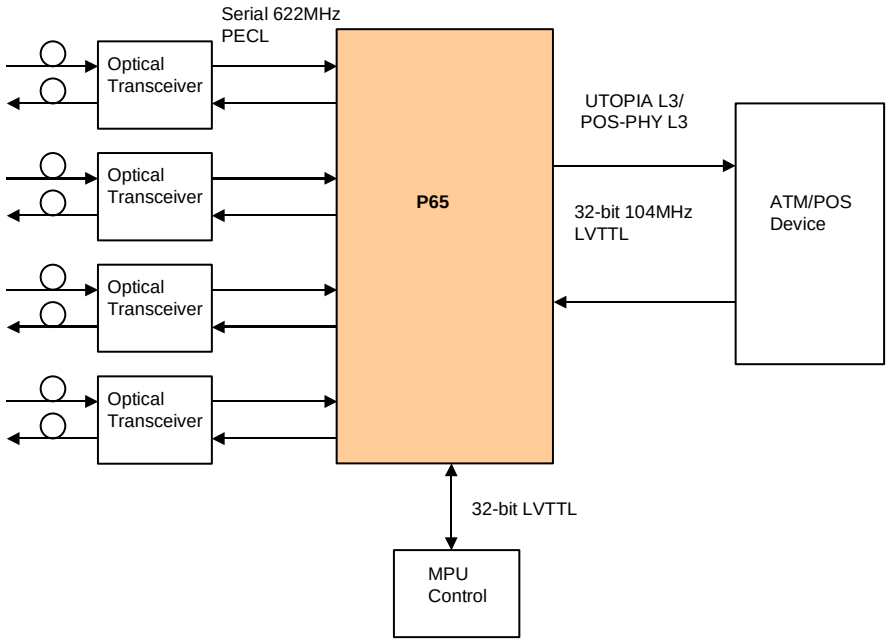
1.2 Ordering Information

TBD

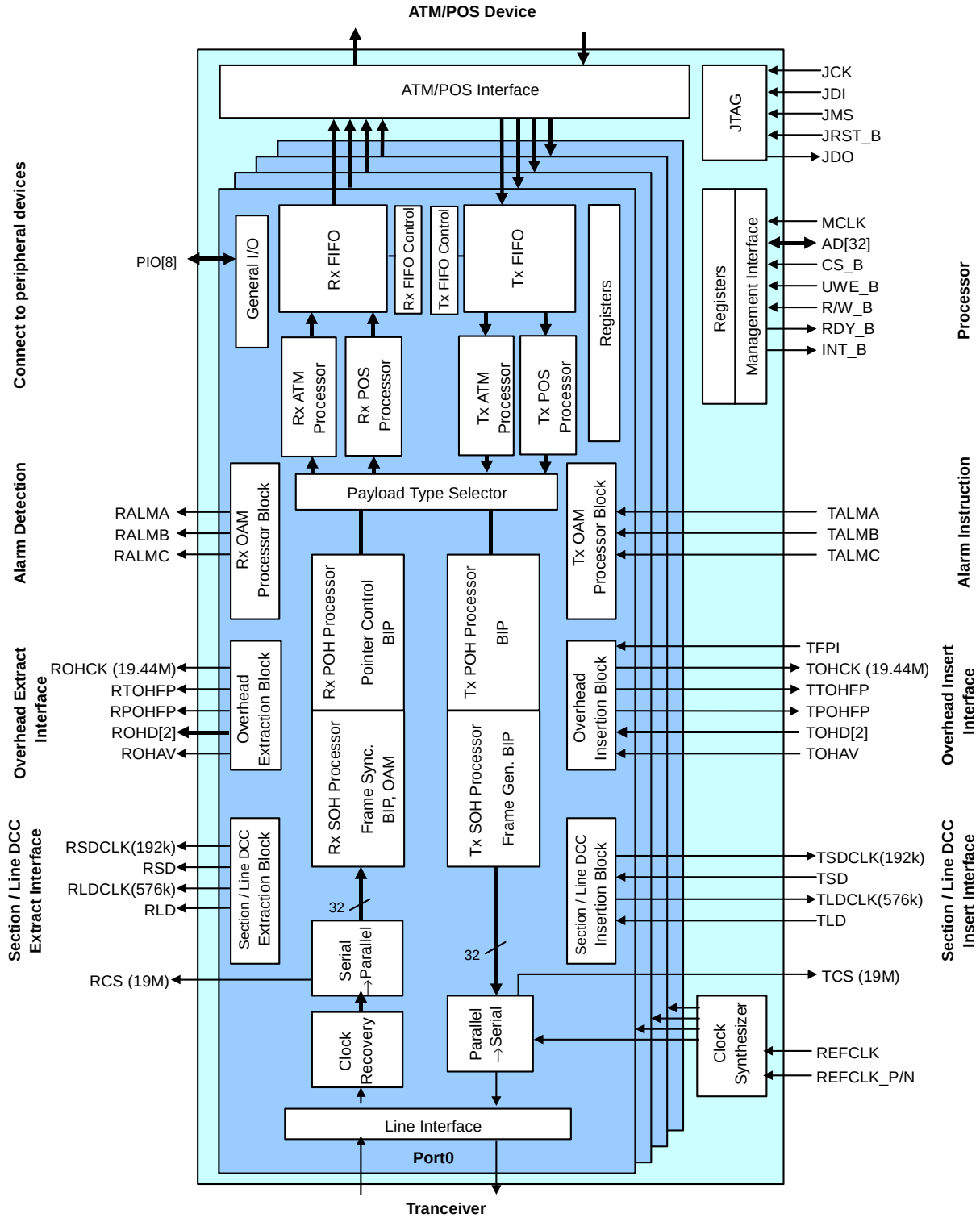
1.3 Application

- Routers
- ATM switches
- Access concentrators
- Add/drop multiplexers and Digital cross connects

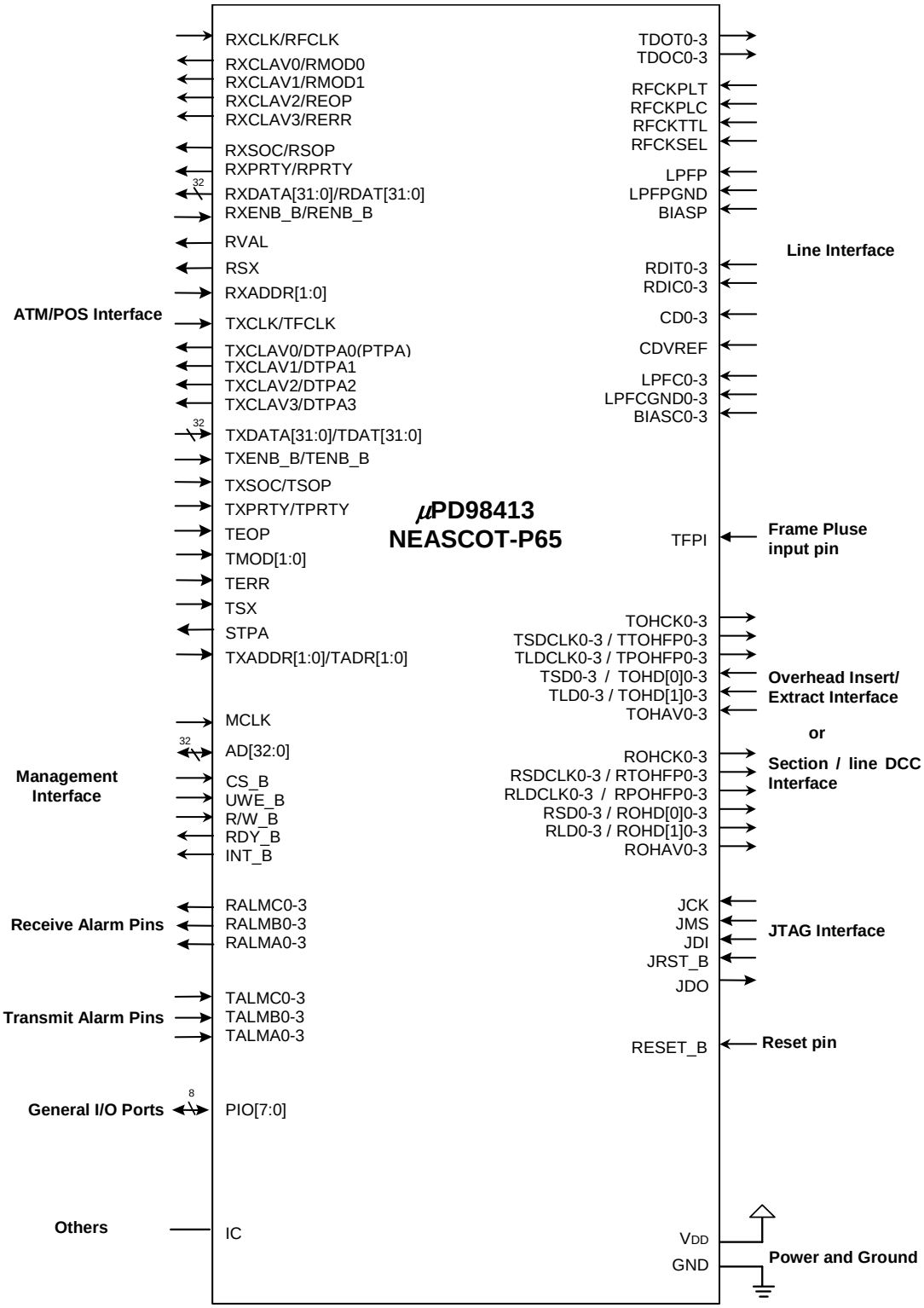
Typical Application



1.4 Block Diagram



1.5 Pin Configuration



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- ANSI - T1.105 “Synchronous Optical Network (SONET)-Basic Description including Multiplex Structure, Rate, and Format ”, 1995
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CHAPTER 2 PIN FUNCTION

2.1 Pin Configuration

TBD

Pin Arrangement Table

TBD

2.2 Pin Function

2.2.1 Line Interface

The line interface connects with an optical transceiver.

(1/2)

Pin Name	Serial No.	Address No.	I/O Level	Function
TDOT0-3			O	Transmit serial data output pins.
TDOC0-3			2.5V Differential PECL	Transmit data is output from these pins.
RFCKPLT			I 2.5V Differential PECL	The differential reference clock inputs. Inputs the reference clock for both the CDR and the synthesizer PLL circuits. RFCKPLT must be connected to a logic one and RFCKPLC to a logic zero state when RFCKTTL is used.
RFCKPLC				
RFCKTTL			I LVTTL	TTL reference clock input. TTL reference clock inputs for both the CDR and the TxPLL circuits. RFCKTTL must be tied high if RFCKPLT/ RFCKLC is used.
LPFP			Analog	Loop Filter Capacitor for synthesizer PLL. The TxPLL loop filter capacitor is connected to this pin.
LPFPGND			Analog	Loop Filter Capacitor for synthesizer PLL. (GND) The TxPLL loop filter capacitor is connected to this pin.
BIASP			Analog	Bias pin for TxPLL Connects to analog VDD via 1.1KΩ register

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Pin Name	Serial No.	Address No.	I/O Level	Function
RDIT0-3			I 2.5V Differential PECL	Receive serial data input. The input data is sampled with the recovered clock from the internal CDR when the internal CDR mode.
RDIC0-3				
CD0-3			I 3.3V Single-ended PECL	Carrier Detect. The receive signal detect PECL input indicates the loss of receive signal power from the Optical module and it is active high. Each port has one pin. CD0 corresponds to PORT0, while CD3 corresponds to PORT3.
CDVREF			I 3.3V PECL	This pin input reference potentials (intermediate potentials) for single-ended PECL input signals (CD0-3).
LPFC0- LPFC3			Analog	Loop Filter Capacitor the CDR. The CDR loop filter capacitor is connected to this pin. Each port has one pin.
LPFCGND0- LPFCGND3			Analog	Loop Filter Capacitor the CDR.(GND) The CDR loop filter capacitor is connected to this pin. Each port has one pin.
BIASC0-3			Analog	Bias pin for CDR Connects to analog VDD via 1.1KΩ register

2.2.2 ATM/POS Interface

The ATM/POS interface transfers ATM cells or POS packets to and from an ATM/POS device.

ATM Interface

(1/2)

Pin Name	Serial No.	Address No.	I/O Level	Function
RXCLK			I LVTTL	Receive clock input. This pin inputs the clock, up to 104 MHz, used to transfer receive data.
RXDATA[31:0]			O LVTTL	Receive data output. These pins form a 32-bit data bus through which receives cell data is output to the ATM device. The data on this bus is updated at the rising edge of RXCLK. RXDATA31 is the MSB. RXDATA0 is the LSB.
RXSOC			O LVTTL	Receive cell start position signal output. This pin goes high during the clock cycle in which the first byte of the receive cell is output to RXDATA, to post notification to the ATM device.
RXENB_B			I LVTTL	Receive enable signal input. The ATM device enables or disables the receive cell data output by the µPD98413. The µPD98413 samples RXENB_B at the rising edge of RXCLK. When it detects the low level of RXENB_B, it updates the output of RSOC and RXDATA starting from the next clock cycle, and then transfers the receive cell data. If RXENB_B is high, the µPD98413 stops the output of RSOC and RXDATA, starting from the next clock cycle.
RXPRTY			O LVTTL	Receive data path parity. This pin generates an odd parity bit for the output data on RXDATA and outputs it from RXPRTY. The parity bit is always output. The parity bit to be generated can be changed to even parity depending on the setting of the PARM bit of MDAPIR register.
RXCLAV0-3			O LVTTL	Receive cell available. The µPD98413 drives RXCLAV high if one or more cells of receive data to be transferred exists in the receive FIFO, to post notification to the ATM device. RXCLAV is held high if one or more cells of valid data exists in the receive FIFO at the 2 clock cycle or later after the start of output of the cell; otherwise, RXCLAV goes low. RXCLAV0 corresponds to PORT0, while RXCLAV3 corresponds to PORT3.
RXADDR[1:0]			I LVTTL	Receive PHY address input. These pins are used to input a port address for requesting data output.

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Pin Name	Serial No.	Address No.	I/O Level	Function
TXCLK			I LVTTL	Transmit clock input. This pin inputs the clock, up to 104 MHz, used to transfer transmit data.
TXDATA[31:0]			I LVTTL	Transmit data input bus. These pins form a 32-bit data bus through which transmits cell data is input. The µPD98413 samples the data on this bus at the rising edge of TXCLK.
TXSOC			I LVTTL	Transmit start of cell input. This pin is inputted a signal that indicates the start position of a transmit cell. The µPD98413 recognizes the clock cycle in which TXSOC is high as the first word of a cell.
TXENB_B			I LVTTL	Transmit enable signal input. This signal indicates that the ATM device has output valid transmit cell data to TXDATA. The µPD98413 samples TXENB_B at the rising edge of TXCLK. If TXENB_B is low, it loads the data on TXSOC and TXDATA to the transmit FIFO at the edge of TXCLK. If TXENB_B is high, the data on TXSOC and TXDATA is not loaded to the transmit FIFO.
TXCLAV0-3			O LVTTL	Transmit cell buffer available. This signal posts notification of the vacancy of the transmit FIFO to the ATM device. If the number of cells stored in the transmit FIFO has reached the threshold value set by the APHIGH[7:0] bits of the FTHT1 register, the µPD98413 drives TXCLAV low. The subsequent cells are dropped and the µPD98413 reports an overflow of the transmit FIFO. TXCLAV0 corresponds to PORT0, while TXCLAV3 corresponds to PORT3.
TXPRTY			I LVTTL (Internal pull-up)	Transmit data path parity. This pin inputs the odd parity bit of the data input to TXDATA. The µPD98413 calculates parity based on the input data and parity bit. If it detects an error, it sets the PARE bit of the APIET register to report the error. An even parity can be also used depending on the setting of the MDAPIT register.
TXADDR[1:0]			I LVTTL	Transmit address input. These pins are used to input a port address for data transmission.

POS Interface

(1/4)

Pin Name	Serial No.	Address No.	I/O Level	Function
RFCLK			I LVTTL	Receive FIFO read clock. Clock signal of up to 104 MHz, supplied from the POS device. All signal operations in the data transfer of the reception interface are executed in synchronization with this clock signal.
RDAT[31:0]			O LVTTL	Receive packet data bus. 32-bit data bus for outputting receives packets. Receive data is output at a rising edge of RFCLK. If RSX is high at the start of transfer, RDAT[7:0] is used to specify the port address.
RSOP			O LVTTL	Receive start of packet. Signal indicating the start position of a receive packet. When RSOP is high, the data on RDAT is assumed to be the beginning of a packet.
RENB_B			I LVTTL	Receive read enable Signal used by the POS device to request a transfer interrupts. When RENB_B is low, the μPD98413 updates the RDAT, RMOD, RSOP, REOP, RERR, RPRTY, RVAL, and RSX signals at the next clock pulse. When RENB_B is high, the μPD98413 will remain unchanged the RDAT, RMOD, RSOP, REOP, RERR, RPRTY, RVAL, and RSX signals at the next clock pulse.
RPRTY			O LVTTL	Receive bus parity. When receive packet data is to be output from RDAT, odd or even parity data is generated and output from RPRTY.
REOP			O LVTTL	Receive end of packet. Signal indicating the end position of a receive packet. When REOP is high, the data on RDAT is assumed to be the end of a packet, and the effective bytes of the last word are indicated by RMOD.
RMOD[1:0]			O LVTTL	Receive word modulo. Signal indicating the effective bytes of the last word RDAT of a receive packet. RMOD is valid when REOP is high. When RMOD[1:0] is equal to 00, RDAT[31:0] is effective. When RMOD[1:0] is equal to 01, RDAT[31:8] is effective. When RMOD[1:0] is equal to 10, RDAT[31:16] is effective. When RMOD[1:0] is equal to 11, RDAT[31:24] is effective.

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Pin Name	Serial No.	Address No.	I/O Level	Function
RERR			O LVTTL	Receive error indicator signal. Signal indicating that the packet being transferred is an abort packet and should be discarded. Upon detecting a reception FIFO overflow, FCS error, or abort sequence, the μPD98413 causes RERR to go high. RERR and REOP must be asserted at the same time.
RVAL			O LVTTL	Receive data valid signal. Indicates whether the receive data (RDAT) and other signals are valid. When RVAL is high, the RDAT, RMOD, RSOP, REOP, RERR, and RPRTY signals are valid. RSX is valid when RVAL is low.
RSX			O LVTTL	Receive start of transfer. Signal for controlling the port address specification using RDAT[7:0] at the start of transfer. When RSX is high and RVAL is low, a port address can be output to RDAT[7:0] to select the port used to start transfer.

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Pin Name	Serial No.	Address No.	I/O Level	Function
TFCLK			I LVTTL	Transmit FIFO write clock. Clock signal at up to 104 MHz supplied from the POS device. All signal operations in the data transfer of the transmission interface are executed in synchronization with this clock signal.
TDAT [31:0]			I LVTTL	Transmit packet data bus. 32-bit data bus for inputting transmit packets. Transmit data is input at a rising edge of TFCLK. If TSX is high at the start of transfer, TDAT[7:0] is used to specify the port address.
TSOP			I LVTTL	Transmit start of packet. Signal indicating the start position of a transmit packet. When TSOP is high, the data on TDAT is assumed to be the beginning of a packet.
TENB_B			I LVTTL	Transmit write enable. Indicates whether the transmit data (TDAT) and other signals are valid. When TENB_B is low, the TDAT, TMOD, TSOP, TEOP, TERR, and TPRTY signals are valid. TSX is valid when TENB_B is high.
TPRTY			I LVTTL	Transmit bus parity. Signal for inputting the odd or even parity for the data to be input to TDAT. Upon detecting a parity error, the uPD98413 reports it with an interrupt. Even if a parity error is detected, data transfer continues without being affected.
TEOP			I LVTTL	Transmit end of packet. Signal indicating the end position of a transmit packet. When TEOP is high, the data on TDAT is assumed to be the end of a packet, and the effective bytes of the last word are indicated by TMOD.
TMOD[1:0]			I LVTTL	Transmit word modulo. Signal indicating the effective bytes of the last word TDAT of a transmit packet. TMOD is valid when TEOP is high. When TMOD[1:0] is equal to 00, TDAT[31:0] is effective. When TMOD[1:0] is equal to 01, TDAT[31:8] is effective. When TMOD[1:0] is equal to 10, TDAT[31:16] is effective. When TMOD[1:0] is equal to 11, TDAT[31:24] is effective.
TERR			I LVTTL	Transmit error. Signal for aborting a packet being transferred. When TERR goes high, the packet being transferred is sent as an abort packet. TERR and TEOP must be asserted at the same time.

TSX			I LVTTL	Transmit start of transfer. Signal for controlling the port address specification using TDAT[7:0] at the start of transfer. When TSX is high and TENB_B is high, the port used to start transfer can be selected with the port address input to TDAT[7:0].

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Pin Name	Serial No.	Address No.	I/O Level	Function
DTPA[3:0]			O LVTTL	Direct transmit packet available. In direct status indication, the signal indicating the status of the corresponding port. When high, DTPA indicates that the transmission FIFO has an enough free space and is capable of data transfer. When low, DTPA indicates that the transmission FIFO is full (or almost full) and is not capable of data transfer. The high/low transition of DTPA (transmission FIFO status) is programmable.
STPA			O LVTTL	Selected port transmit packet available. Signal indicating the status of the selected port. When high, STPA indicates that the transmission FIFO has enough free space and is capable of data transfer. When low, STPA indicates that the transmission FIFO is full (or almost full) and is not capable of data transfer. The high/low transition of STPA (transmission FIFO status) is programmable.
PTPA			O LVTTL	Polled port transmit packet available. In status polling, signal indicating the status of the polled port. It indicates the status of the port selected by TADR. When high, PTPA indicates that the transmission FIFO has enough free space and is capable of data transfer. When low, PTPA indicates that the transmission FIFO is full (or almost full) and is not capable of data transfer. The high/low transition of PTPA (transmission FIFO status) is programmable.
TADR[1:0]			I LVTTL	Transmit port address. Signal for specifying the address of the port to be polled to obtain the status of the transmission FIFO (full/not full). The transmission FIFO status for the port specified by TADR is reported by PTPA at the next clock pulse.

2.2.3 Management Interface

The management interface is used to access the registers of the μPD98413.

Pin Name	Serial No.	Address No.	I/O Level	Function
MCLK			I LVTTL	Microprocessor bus Clock This pin Input microprocessor bus Clock. All read and write operations in the Management interface are executed in synchronization with this clock signal.
AD31-0			I/O LVTTL	Address / data bus The AD31 to AD0 bus is a 32-bit, bi-directional, multiplexed address/data bus. During the first clock of a transaction, AD31 to AD0 contains a physical byte address. During subsequent clocks, AD31 to AD0 contains data. When the μPD98413 is not accessing the bus, it places the AD bus in the high impedance state.
CS_B			I LVTTL	I/O chip select signal When this signal is low, access to the internal registers of the μPD98413 is enabled.
UWE_B			I LVTTL	Upper word enable signal
R/W_B			I LVTTL	Read / write select signal
RDY_B			O 3-state LVTTL	Ready signal
INT_B			O LVTTL	Interrupt Output The INT_B output is used to inform the CPU that an (unmasked) interrupt bit was set in the INT.

2.2.4 Overhead Interface

The overhead interface is used to transfer the contents of the transport overhead (TOH) and path overhead (POH) that are exchanged between the peripheral device and μPD98413.

(1/2)

Pin Name	Serial No.	Address No.	I/O Level	Function
TOHCK0-3			O LVTTL	Transmit overhead interface clock output (19.44 MHz). This pin outputs a 19.44MHz obtained by internally dividing transmit clock TCLK (622.08 MHz) by 32. TTOHFP, TPOHFP and TOHD are output in sync with this divided clock.
TTOHFP0-3			O LVTTL	Transmit TOH frame pulse output. This signal is driven high 2 clock cycle before the inputs of transmit TOH data is started.
TPOHFP0-3			O LVTTL	Transmit POH frame pulse output. This signal is driven high 2 clock cycle before the inputs of transmit POH data is started.
TOHD[1:0]0-3			I LVTTL	Transmit TOH /POH data input 2-bit bus. This is a 2-bit data bus that inputs transmit TOH /POH data. It inputs the TOH / POH data on TOHD as 1 byte in 4 clock cycles, starting to data input from 2 clock cycle later TTOHFP is output.
TOHAV0-3			I LVTTL	Transmit TOH / POH data validity indication signal input. This signal informs the μPD98413 that valid TOH / POH data has been output to TOHD. The μPD98413 samples TOHAV at the rising edge of TOHCK at the first clock of the four clock cycles in which TOH / POH data is input. If TOHAV is high, the μPD98413 inputs the data on TOHD in that cycle and the next three cycles; when TOHAV is low, the μPD98413 does not input the data.

(2/2)

Pin Name	Serial No.	Address No.	I/O Level	Function
ROHCK0-3			O LVTTL	Receive overhead interface clock output (19.44 MHz) This pin outputs the 19.44-MHz clock obtained by internally dividing receive clock RCLK (622.08 MHz) by 32. RTOHFP, RPOHFP and ROHAV are output in sync with this divided clock.
RTOHFP0-3			O LVTTL	Receive TOH frame pulse output. This signal goes high coincident with the clock cycle in which output of the receive TOH data is started.
RPOHFP0-3			O LVTTL	Receive POH frame pulse output. This signal goes high coincident with the clock cycle in which output of receive POH data is started.
ROHD[1:0]0-3			O LVTTL	Receive TOH / POH data output 2-bit bus. This 2-bit bus outputs receive TOH / POH data. It starts output of the receive TOH / POH onto ROHD starting from the clock cycle at the same time RTOHFP is output.
ROHAV0-3			O LVTTL	Receive TOH / POH validity indication signal output. This signal indicates that valid receive TOH data is output to ROHD. In the clock cycle in which valid data is output to ROHD, ROHAV goes high. In the clock cycle in which valid data is not output, ROHAV goes low.

2.2.5 Section and Line DCC Interface

Pin Name	Serial No.	Address No.	I/O	Function
TSDCLK0-3			O LVTTL	Transmit section DCC clock (TSDCLK) This pin outputs a 216kHz clock. TSDCLK0 corresponds to PORT0, while TSDCLK3 corresponds to PORT3.
TSD0-3			I LVTTL	Transmit section DCC (TSD) signals contains the serial section data communications channel (D1, D2, and D3). TSD0 corresponds to PORT0, while TSD3 corresponds to PORT3.
TLDCLK0-3			O LVTTL	Transmit line DCC clock (TLDCLK) This pin outputs a 648kHz clock. TLDCLK0 corresponds to PORT0, while TLDCLK3 corresponds to PORT3.
TLD0-3			I LVTTL	Transmit line DCC (TKD) signals contains the serial line data communications channel (D4-D12). TLD0 corresponds to PORT0, while TLD3 corresponds to PORT3.
RSDCLK0-3			O LVTTL	Receive section DCC clock (RSDCLK) This pin outputs a 216kHz clock. RSDCLK0 corresponds to PORT0, while RSDCLK 3 corresponds to PORT3.
RSD0-3			O LVTTL	Receive section DCC (RSD) signal contains the serial section data communications channel (D1, D2, D3) extract from the incoming stream. RSD0 corresponds to PORT0, while RSD3 corresponds to PORT3.
RLDCLK0-3			O LVTTL	Receive line DCC clock (RLDCLK) This pin outputs a 648kHz clock. RLDCLK0 corresponds to PORT0, while RLDCLK 3 corresponds to PORT3.
RLD0-3			O LVTTL	Receive line DCC (RLD) signals contains the serial line data communications channel (D4-D12) extract from the incoming stream. RLD0 corresponds to PORT0, while RLD3 corresponds to PORT3.

2.2.6 Frame Pulse input pins

Pin Name	Serial No.	Address No.	I/O Level	Function
TFPI			I LVTTL	Frame pulse input. The active high framing position (TFPI) signal is used to align the SONET/SDH transport frame generated by the μPD98413 device to a system reference. TFPI must be tied low if such synchronization is not required.

2.2.7 General-Purpose I/O Port

Pin Name	Serial No.	Address No.	I/O	Function
PIO[7:0]			I/O LVTTL	**General-purpose input/output port.** These are general-purpose input or output pins that input or output the state signals of external peripheral devices. It is possible to change to input or output with the MDDGEN register GPIOM[7:0] bit setting. **General-purpose input** The signal levels of these pins are reflected on the bits of the internal GPIN register. Changes in the statuses of these bits can be used as interrupt causes. **General-purpose output** The settings of the bits of the internal GPOUT register are output to these pins as signal levels. These pins can be used to control external peripheral devices.

2.2.8 Alarm Signal Input / Output

Pin Name	Serial No.	Address No.	I/O Level	Function
RALMC0-3 RALMB0-3 RALMA0-3			O LVTTL	Alarm signal output. These pins output a signal indicating that an internally monitored error state has been detected. The pins can output an error either singly or in combination. The type of the error to be indicated is selected by setting the internal RALMR registers.
TALMC 0-3 TALMB 0-3 TALMA 0-3			I LVTTL	Alarm signal input The alarm, which it is possible to insertion, is LAIS, PAIS, LRDI, PRDI, PERDI (Payload defect, Server defect, Connectivity defect) and the following code corresponds to TALMCx-TALMAx 000: No Alarm 001: LAIS 010: PAIS 011: LRDI 100: One-bit PRDI mode - PRDI (one-bit PRDI, G1 bit5 : 1) Enhanced PRDI mode - PERDI Server defect (G1 bit5-7 : 101) 101: PERDI Connectivity defect (G1 bit5-7 : 110) 110: PERDI Payload defect (G1 bit5-7 : 010) 111: Reserved TALMx 0 corresponds to PORT0, while TALMx 3 corresponds to PORT3.

2.2.9 JTAG Boundary Scan

Pin Name	Serial No.	Address No.	I/O Level	Function
JCK			I LVTTL	Boundary scan clock input. Ground this pin when not used.
JDI			I LVTTL (Internal pull-up)	Boundary scan data input.
JDO			O 3-state LVTTL	Boundary scan data output. Open this pin when not used.
JMS			I LVTTL (Internal pull-up)	Boundary scan mode selects signal input.
JRST_B			I LVTTL (Internal pull-up)	Boundary scan reset signal input.

2.2.10 Reset pin

Pin Name	Serial No.	Address No.	I/O Level	Function
RESET_B			I LVTTL	Reset signal The RESET_B signal provides a means of initializing the μPD98413 (i.e. at power on). After the completion of a reset, the μPD98413 can start normal operation. Once RESET_B has been set to low, it resets the μPD98413 internal state machines and registers, and forces all 3-state signals to the high impedance state. Reset input is performed asynchronously. If low during operation, current state will be lost.

2.2.11 Power and Grounding Pins

Pin Name	Serial No.	Address No.	I/O	Function
V_{DD}			–	Power supply pins
GND			–	Ground pins

2.2.12 Others

Pin Name	Serial No.	Address No.	I/O Level	Function
IC			–	Internal circuit connection test pins.

2.2.13 Handling Unused Pins

TBD

2.2.14 Initial States of Each Pin

TBD

[MEMO]

[Caution]

The data bit string of the SONET/SDH frame is sequentially transmitted from the MSB when it is transmitted from the line interface (line side). In this document, the MSB is always shown on the left side in figures. Note that each bit in the overhead byte (OH byte) of the SONET/SDH frame is described in the following two ways:

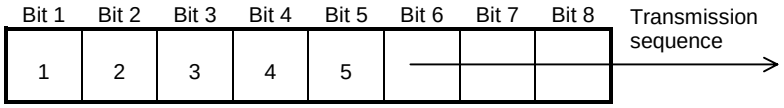
Description <1> bits 1 to 8

This description is mainly used to indicate the bit string of the overhead byte in the SONET/SDH frame in the order in which the bits are output from the line interface.

Description <2> D31 to D0 bits

This description is mainly used to indicate the bits in an internal register of the μPD98413. The bits correspond to the AD31 to AD0 pins of the external CPU interface.

<1> Indicating bits in overhead byte

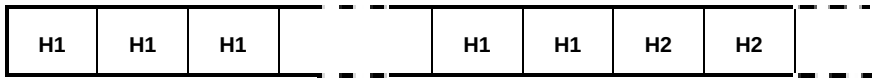


D31	D30	D29	D28	D27	D26	D25	D24
D23	D22	D21	D20	D19	D18	D17	D16
D15	D14	D13	D12	D11	D10	D9	D8
D7	D6	D5	D4	D3	D2	D1	D0

<2> Indicating bits in internal register

(D31 is input/output to/from data bus AD31 of CPU interface.)

In this document, the following two descriptions are also used to indicate the same overhead byte in the SDH/SONET frame.



Description <1>	1st H1	2nd H1	3rd H1	47th H1	48th H1	1st H1	2nd H1
Description <2>	H1#1	H1#2	H1#3	H1#47	H1#48	H1#1	H1#2

CHAPTER 3 FUNCTIONAL OUTLINE

The μPD98413 is a quad STS-12/STM-4 framer device. The major functions are to map the ATM cells/POS (PPP over SONET) packets received from the ATM/POS device into the SONET/SDH frame and output the ATM cells/POS packets to the line, or to receive the ATM cells/packets from a receive SONET/SDH frame and output the ATM cells/ packets to the ATM/POS device. The mode of the μPD98413 is set, commands are issued to the μPD98413, and its status registers are polled via the management interface.

Figure 3-1. μPD98413 and Peripheral Blocks

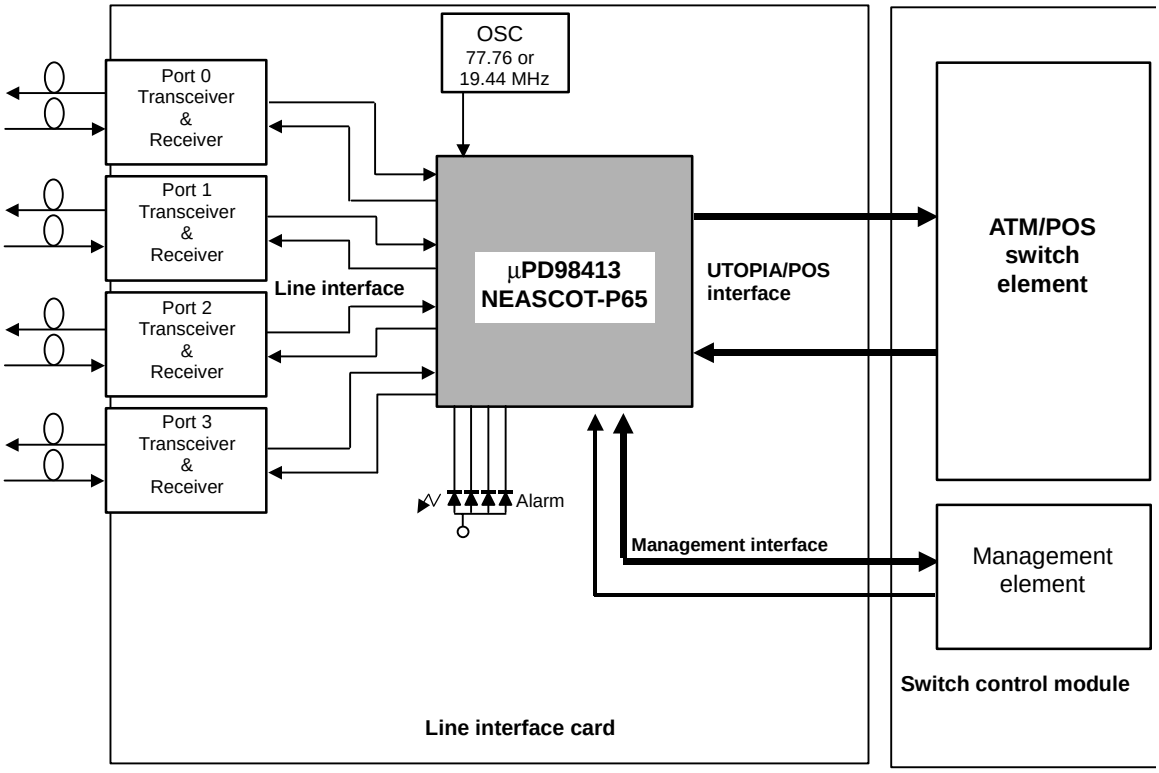


Figure 3-2. Transmit/Receive Data Flow of μPD98413

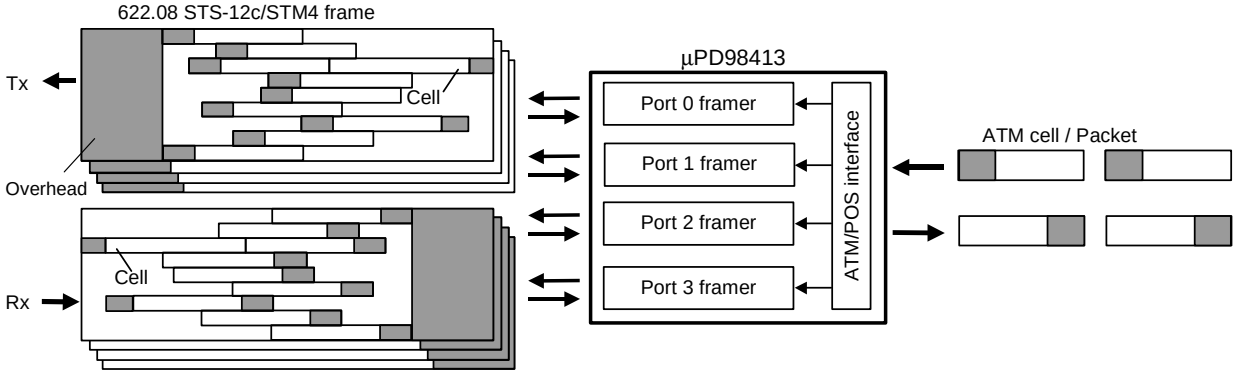
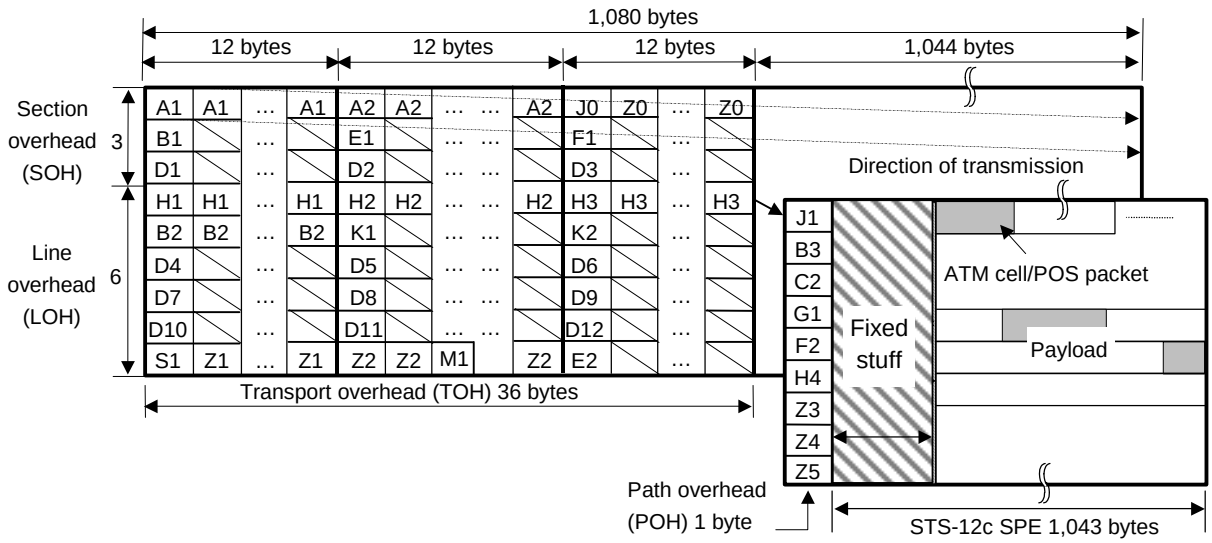
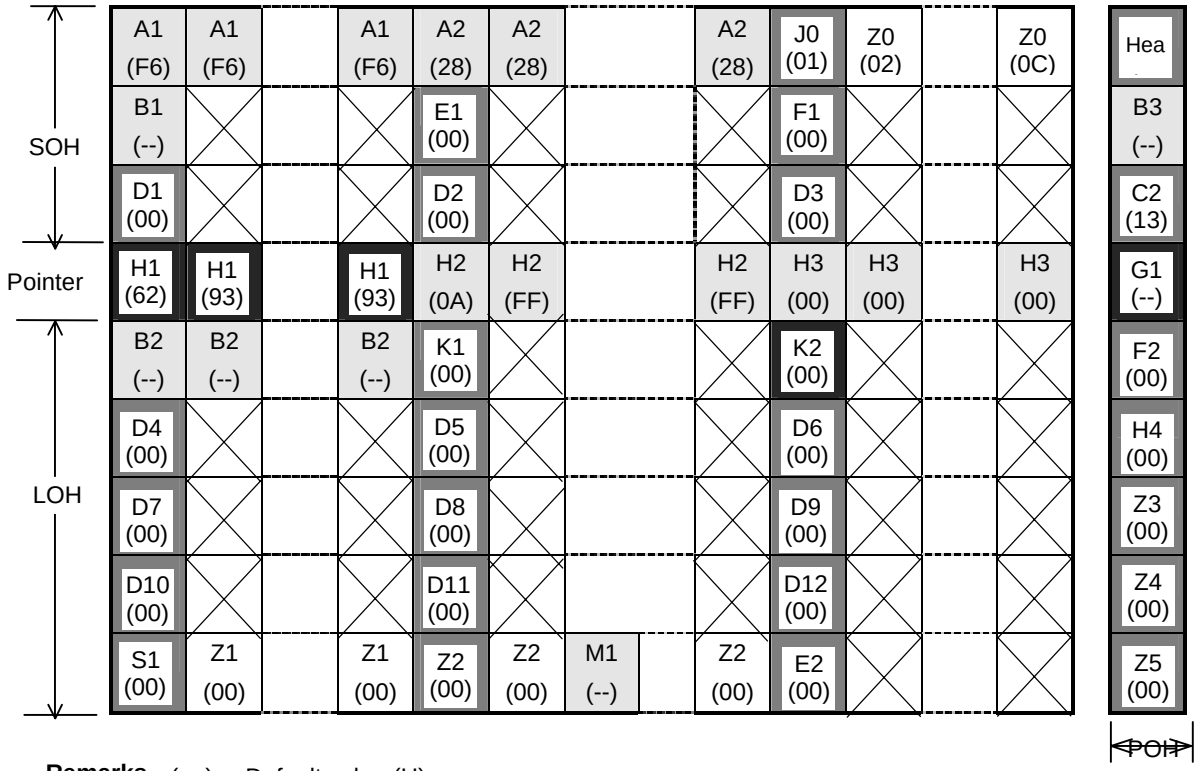


Figure 3-3 shows the format of the frame supported by the μPD98413.

Figure 3-3. Format of Transmit Frame



Overhead (OH) Field



Remarks ( ) : Default value (H)

: Byte area that cannot be rewritten by an external device (automatically set by μPD98413).

: Byte area that can be changed by writing a register.
(Can also be changed from the external insert interface of the OH byte.)

: Byte area in which some bits can be changed by writing a register.
(Only the SS bits of the H1 byte can be rewritten.)
(K2 and G1 can be set by a register or automatically set by the μPD98413.)

: Byte area that can be changed by the external insert interface of the OH byte.

: Unused byte area. Default value is 00H.
(Can be changed by the external insert interface of the OH byte.)

A1, A2 : Frame synchronization
J0 : Section trace
Z0 : Section growth
B1 : Section BIP-8
E1 : Order wire
F1 : Section user channel
D1-D3 : Section data communication channel
H1, H2 : Pointer
H3 : Pointer action byte
B2 : Line BIP-96
K1, K2 : APS channel
D4-D12 : Line data communication channel
S1 : Synchronization massaging
Z1 : Growth
Z2 : Growth
M1 : STS-N line REI
E2 : Order wire
J1 : STS path trace
B3 : Path BIP-8
C2 : STS path signal label
G1 : Path status
F2 : Path user channel
H4 : Multiframe indicator
Z3-Z5 : Growth

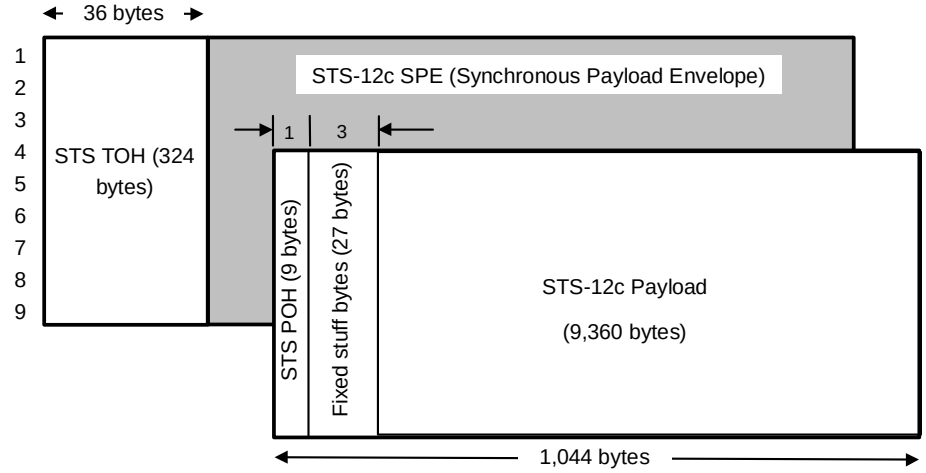
3.1 SONET Overhead Processing

3.1.1 Transmission Function

(1) Generation of SONET frame

The cell/packet stream is mapped onto the payload area of STS-12c SPE of SONET, and the μPD98413 creates a SONET STS-12c frame by adding the path overhead (POH) and transport overhead (TOH) information. For details of the format of the frame to be created, see **Figure 3-4**.

Figure 3-4. STS-12c SPE



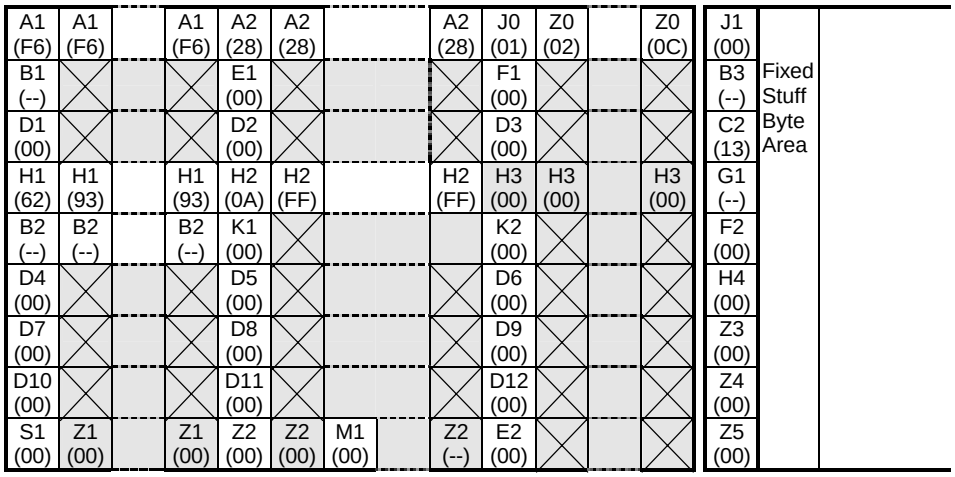
The overhead generated by the μPD98413 and the selection of a mode is described below.

(a) Selecting contents of unused OH byte

All 00H is inserted into the following areas of TOH (hatched area in Figure 3-5). The inserted value can be changed to FFH by using the UUBM bit of the MDSOHT and MDLOHT registers.

<1> Unused byte area (area marked ⊠ in Figure 3-5)
<2> H3 byte (Negative Stuff byte)
<3> Z1 and Z2 bytes (except the 1st Z2 byte)

Figure 3-5. Unused OH Byte



Remark Any value can be also inserted from the OH interface to the unused OH byte area. Inserting byte data from the OH interface takes precedence over the changing of this mode.

(b) Fixed Stuff byte

In the second through 4th columns of SPE are Fixed Stuff bytes. In the default mode, all FFH is inserted. This value can be changed to all 00H by using the FSBM bit of the MDPOHT register.

(c) Changing inserted value of 5th byte of Z0 and those that follow

In the default mode, 02H to 0CH are sequentially stored to the Z0 byte of 11. These values can be changed to AAH from the 4th byte to the 11th byte of the Z0 byte by using the Z0M bit of the MDSOHT register.

Figure 3-6. Inserted Value of Z0 Byte

	J0 0	Z0 1	Z0 2	Z0 3	Z0 4	Z0 5	Z0 6	Z0 7	Z0 8	Z0 9	Z0 10	Z0 11
Default	01	02	03	04	05	06	07	08	09	0A	0B	0C
AA mode	01	02	03	04	AA	AA	AA	AA	AA	AA	AA	AA

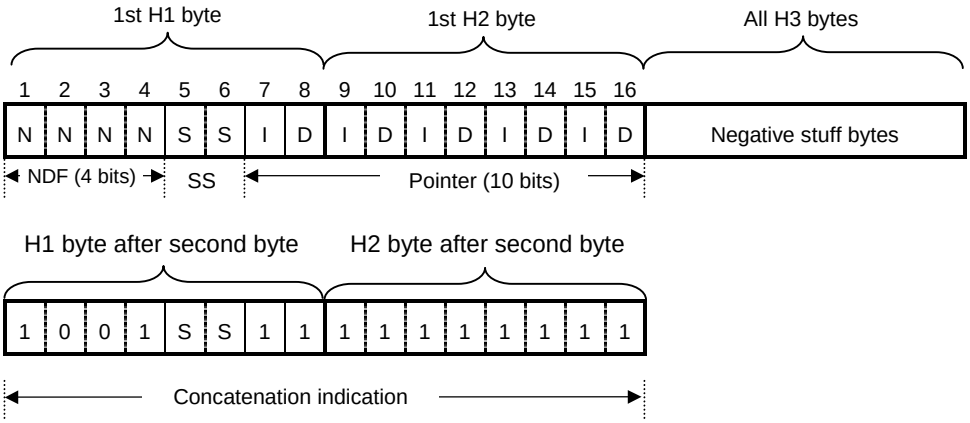
(d) Pointer generation

The pointer on the fourth line of TOH consists of three types of bytes, H1, H2, and H3, and it is used as an address to identify the first byte (J1 byte of POH) of SPE.

The transmit frame transmitted by the μPD98413 changes the position of neither POH (path overhead) nor the J1 byte. Therefore, the pointer value stored into the H1 and H2 bytes is always 20AH = "1000001010", and NDF is always fixed to "0110" and disabled. The SS bits that are the bit 5 and bit 6 of the H1 byte are "00" by default. Their values can be changed by setting the SS[1:0] bits of the MDPTRT register.

Because Frequency Justification (stuff operation) is not requested at the transmission side, payload data is not set in the H3 byte that is used as Negative Stuff byte. Instead, the H3 byte is set to all zeros and transmitted.

Figure 3-7. Format of Pointer (H1 through H3 Bytes)



Remark NDF: New Data Flag. Enable or disable command when the pointer value is to be changed. Because the μPD98413 does not change the pointer value, "0110," that disables the pointer value, is always transmitted.
(NDF Enable = 1001, NDF Disable = 0010, 0110, 0100, 0111, 1110)

SS bit: Indicates the type of SPE. The μPD98413 inserts the bit set into the SS[1:0] bits of the MDPTRT register. The default value is "00".

Pointer: Indicates the position of the first byte J1 of POH and requests Frequency Justification operation.
I (Increment bit): Requests Positive Justification operation.
D (Decrement bit): Requests Negative Justification operation.

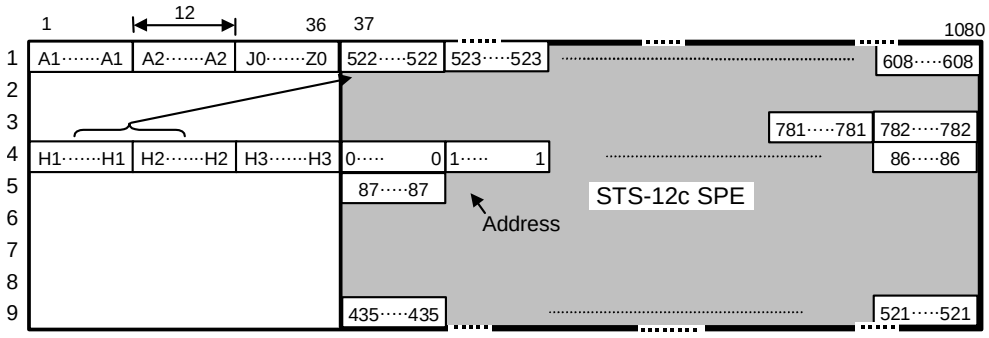
Concatenation indication: Indicates concatenation.

Contents of H1 through H3 Bytes Transmitted by μPD98413

	H1 Byte	H2 Byte	H3 Byte
1st byte	0110 SS10	0000 1010	0000 0000
2nd and onward	1001 SS11	1111 1111	0000 0000

Remark The pointer value is a binary number in the range of 0 to 782 and indicates the address of the first byte (J1) of SPE. The offset value increments by 12 bytes as shown in Figure 3-8. If the pointer value is 0, for example, it indicates that SPE starts from the byte position immediately after the H3 byte. If the pointer value is 522 (20AH), SPE starts from the position immediately after the 11th Z0.

Figure 3-8. Offset Value of Pointer



(e) BIP generation

The B1, B2, and B3 bytes of the overhead are used to monitor an error of a frame. The μPD98413 performs a BIP (Bit Interleaved Parity) operation on the transmit frame data and inserts the result of the operation into the positions equivalent to the B1, B2, and B3 bytes of the next overhead.

(f) REI transmission

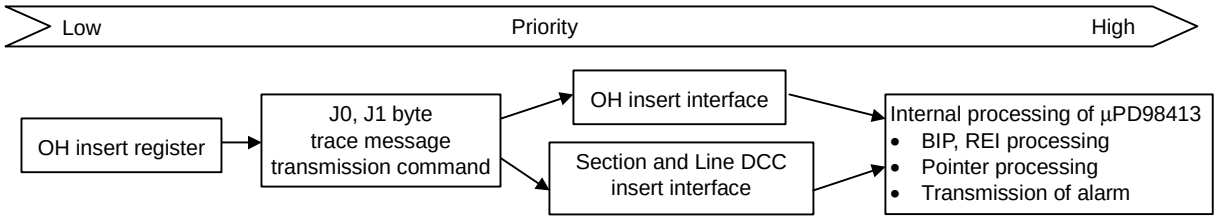
Whether a BIP error has occurred at the reception side is reported to the transmission destination device. If a B2 error is detected in a receive frame, the number of errors is stored into M1 byte of line overhead as Line REI (Remote Error Indication) for transmission. If a B3 error is detected, the number of errors is stored into G1 (bits 1 to 4) as Path REI for transmission.

(2) Insert function of transmit OH byte

The μPD98413 supplies the following four types of means to set the contents of the OH byte of a transmit frame.

- OH insert register
- OH insert interface
- Section and Line DCC insert interface
- Setting of J0/J1 byte trace message

If the same OH byte is set by two or more means, the priority is as follows:



(a) OH insert register setting

The μPD98413 has an insert register that sets an arbitrary value in the following byte areas of the overhead for transmission. By setting this insert register via the management interface, any value can be transmitted. Until a value is set in the register, the default value of the register is transmitted. For details of the OH insert register, see **Section 3.5**.

- OH byte having insert register
  TOH: K1, K2, E1, E2, F1, D1 through D3, D4 through D12, J0, S1, 1st Z2
  POH: J1, C2, F2, G1(bits 5 to 8), H4, Z3, Z4, Z5

Of these, the internal alarm processing of the μPD98413 takes precedence over K2 and G1 bytes if the μPD98413 must transmit an alarm.

(b) OH insert interface

The μPD98413 has an insert interface that is used to set the contents of the OH byte of the transmit TOH and POH from a peripheral device. These bytes can be input to all the OH bytes, except the following ten bytes.

- OH bytes that cannot be changed: A1, A2, B1, B2, B3, H1, H2, H3, G1 (bits 1 to 4), M1
  (These ten bytes can be input at some timing but, even if they are input, data cannot be changed to these bytes because the μPD98413 internally overwrites these bytes for output).

(c) Section and Line DCC insert interface

The μPD98413 has an input interface that is used to set the contents of the Section and Line DCC from a peripheral device. D1 through D3 bytes can be inserted from the Section DCC insert interface, and D4 through D12 bytes can be inserted from the Line DCC insert interface.

(d) Setting of J0 and J1 trace message

A trace message of 16 or 64 bytes can be set and transmitted to the J0 byte of SOH and J1 byte of POH.

J0: Section trace message
J1: Path trace message

The transmit message is set to an internal buffer of the μPD98413 via management interface. When a command is executed, the μPD98413 sets each byte of the message at the positions of the J0 and J1 bytes for transmission.

(3) Scramble of frame

The frame to be transmitted is scrambled by using the following polynomial expression. Scramble is performed for the bytes in the entire range, except a total 36 bytes of "A1, A2, J0 and Z0".

Polynomial $G(X) = 1 + X^6 + X^7$

The user can select a scramble stop mode for the purpose of testing. The scramble stop mode is selected by the FSCM bit of the MDSOHT register.

(4) Frame output to line interface

The generated frame data is output from the line interface to the line side as serial data in sync with the 622.08-MHz clock created by the internal synthesizer PLL.

(5) Transmission of alarm

By setting the CMALM register as necessary, alarm information, Line AIS, Path AIS, Line RDI, and Path RDI can be inserted into a specific overhead area of a transmit frame for transmission.

Line RDI and Path RDI are automatically transmitted depending on the status of the reception side. Automatic transmission can also be masked by setting the ALRDIM bit of the MDLOHT register (Line RDI) and the APRDIM bit of the MDPOHT register (Path RDI). For details of transmitting an alarm, see **Section 3.4.1**.

(6) Transmitting a pseudo frame generating error

A pseudo frame that causes the opposing receiver unit to detect an error is available for testing purposes. By setting the pseudo error register (PESOH, PELOH, PEPTR, PEPOH, PTATM register), the transmission of various pseudo frames is started. For details of the pseudo error frame transmission function, see **Section 3.7**.

- Types of pseudo frames generated

<1> LOS	**<2>** OOF/LOF	**<3>** LOP	**<4>** OCD/LCD
<5> B1 error	**<6>** B2 error	**<7>** B3 error	
<8> Line REI	**<9>** Path REI		

3.1.2 Reception Function

(1) Establishing frame synchronization

The synchronization pattern of the A1 and A2 bytes is detected in the bit string of the receive data to establish frame synchronization. When the μPD98413 detects four bytes (A1, A1, A2, and A2), two bytes each before and after the boundary of the A1 and A2 bytes that receive 12 bytes per frame, it checks the bit string at the A1 and A2 byte positions of the next frame. If this bit string coincides with the synchronization pattern again, the μPD98413 enters the frame synchronization (In frame) status.

Frame synchronization pattern: 4 bytes (A1 A1 A2 A2)

A1 = 11110110 (F6H), A2 = 00101000 (28H)

0	1	2	3	4	5	. . . . .	9	10	11	12	13	14	. . . . .	19	20	21	22	23	24	25
A1	A1	A1	A1	A1	A1	. . . . .	A1	A1	A1	A2	A2	A2	. . . . .	A2	A2	A2	A2	A2	J0	Z0

Even in the frame synchronization status, the μPD98413 always monitors the A1 and A2 byte positions (four bytes) of the receive frame. If four or more consecutive frame patterns other than the above synchronization pattern are detected, the μPD98413 enters the **frame non-synchronization (Out of Frame)** status.

The number of frames required by the μPD98413 to enter the In frame status (number of backward protection stages: δ) and the number of frames required by the μPD98413 to enter the Out of Frame status (number of forward protection stages: α) can be changed by using the MDSOHR register.

Table 3-1. Number of Forward and Backward Protection Stages of Frame Synchronization

Number of Forward Protection Stages α	MDSOHR Register OOFD[1:0]
3	00
4 (default)	01
5	10
6	11

Number of Backward Protection Stages δ	MDSOHR Register OOFT[1:0]
Reserved	00
2 (default)	01
3	10
4	11

If the OOF status lasts for 3 ms, the μPD98413 enters the Loss Of Frame (LOF) status. The LOF status is terminated if the μPD98413 does not stay in the OOF status for 3 ms. The 3 ms required to detect and terminate the LOF status can be changed to 0 ms by using LOFDT bit of the MDSOHR register to make the detection and clearing conditions of the OOF and LOF statuses the same.

If the levels of the signals input to RDIT, RDIC do not change for 25 μs, the μPD98413 enters the Loss Of Signal (LOS) status.

Table 3-2. OOF, LOF, and LOS Detection Conditions

	Detection Condition	Termination Condition
OOF	If a frame synchronization pattern cannot be detected in α forward protection stages in a row.	If a frame synchronization pattern is detected δ backward protection stages in a row
LOF	If the OOF status lasts for 3 ms. If the LOFDT bit of the MDSOHR register is 0, the LOF status is detected at the same time as OOF.	If the μPD98413 is not in the OOF status for 3 ms. If the LOFDT bit of the MDSOHR register is 0, the LOF status is terminated at the same time as OOF.
LOS	If the signals input to RDIT do not change in level for 25 μs (if the CDO bit of the MDSOHR register is 1, the LOS status is reported when the CD pin goes low.)	The μPD98413 is able to select the LOS termination condition, Bellcore mode or ANSI mode, by the LOST bit of the MDSOHR register. **Bellcore Mode:** If the incoming signal has two consecutive valid framing alignment patterns, and no pulse-free intervals for 25μ s consecutive time between that tow consecutive valid framing. **ANSI Mode:** If the incoming signal that have no pulse-free intervals of 25 μs for 125μs. *If the CD pin is High for above termination condition 25μ s consecutive time. (If include CD pins input for this termination condition (CDO bit of the MDSOHR register is 1),)

(2) Descramble of receive frame

After frame synchronization has been established, the received frame is descrambled with the polynomial shown below. The entire range of the STS-12c frame, except the 36 bytes from the beginning, "A1 (12), A2 (12), J0 (1), Z0 (11)" is descrambled.

Polynomial G (X) = $1 + X^6 + X^7$

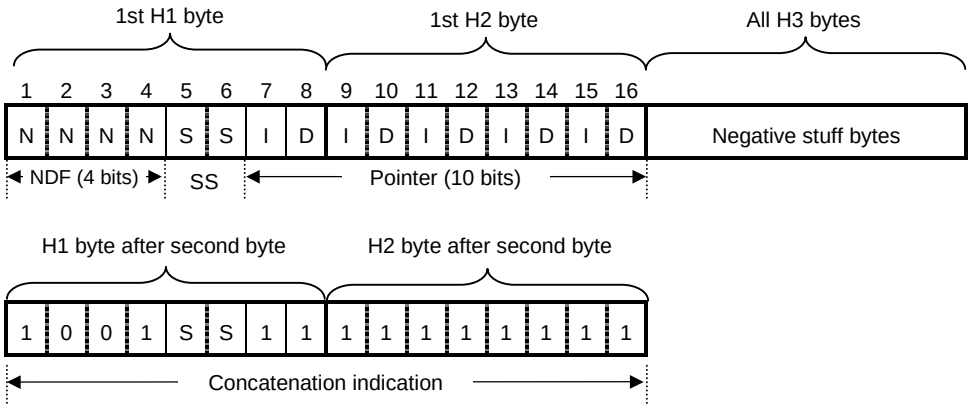
An option mode that disables descrambling of a frame is provided for testing purposes. This mode is set by using the FSCM Bit of the MDSOHR register.

(3) Pointer processing

The H1 and H2 bytes are extracted from the descrambled receive frame and the following processing is performed:

<1> Extraction of pointer value
<2> Frequency justification operation (Positive frequency justification, Negative frequency justification)
<3> Monitoring of pointer synchronization status

Figure 3-9. Format of Pointer



NDF: New Data Flags. These flags enable or disable changing of the pointer value.
- NDF Enable = Requests changing of the pointer value
  If three bits or more of the four bits coincide with 1001 (1001, 1000, 1011, 1101, 0001)
- NDF Disable = Does not request changing of the pointer value
  If three bits or more of the four bits coincide with 0110 (0010, 0110, 0100, 0111, 1110)

SS bit: Indicate the type of SPE.

Pointer: Indicates the position of first byte J1 of POH and requests Frequency Justification (stuff operation).
I (Increment bit): Requests Positive Justification operation.
D (Decrement bit): Requests Negative Justification operation.

Concatenation indication: Indicates concatenation.

(a) Status transition

The receive pointer may be in one of three statuses, NORM, LOP, or AIS, as shown in Figure 3-10, depending on the values of the extracted H1 and H2 bytes.

The overall status of the pointer changes depending on the status transition caused by the pointer processing of H1#1 and H2#1 and on the status transition of each pointer caused by the concatenation indication processing of H1#2 and H2#2 to H1#12 and H2#12.

The μPD98413 has two mode of status transition, Bellcere mode and ITU-T mode. In the Bellcore mode, H1#1 and H2#1, H1#2 and H2#2 to H1#12 and H2#12 is processed one sequencer and the overall status is decided this one sequencer. In the ITU-T mode, H1#1 and H2#1, H1#2 and H2#2 to H1#12 and H2#12 is processed each sequencer(total 12 sequencer) and the overall status is decided these sequencer.

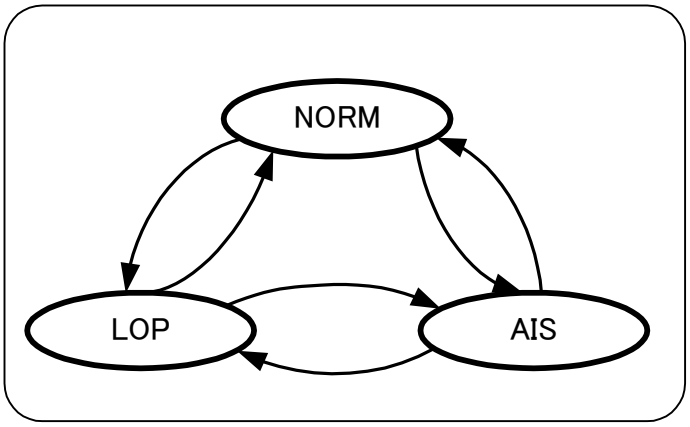
However, by setting the ITUM bit of the MDPTRR register, the status transition mode is changed.

NORM status: The receive pointer is normal and data can be received normally.

AIS status: An abnormality occurs in an upstream device or transmission path. Data cannot be received normally.

LOP status: The receive pointer value is not normal. Data cannot be received normally.

Figure 3-10. Pointer Status Transition



(b) Pointer processing of H1#1 and H2#1

The indication shown in Table 3-3 is interpreted depending on the NDF, SS bits, and pointer value extracted from the H1#1 and H2#1 bytes.

Table 3-3. Pointer Interpretation

	Indication	NDF	SS Bits	Pointer
1	norm_point	Disable	Don't Care<1> or coincidence with expected value	Range of 0 to 782
2	NDF_enable	Enable	Don't Care<1> or coincidence with expected value	Range of 0 to 782
3	AIS_ind	1111	11	All 1
4	incr_ind<2><3>	Disable	Don't care<1> or coincidence with expected value	Three or more I-bits are inverted and three or more D-bits are not inverted.
5	decr_ind<2><3>	Disable	Don't care<1> or coincidence with expected value	Three or more I bits are not inverted and three or more D bits are inverted.
6	inv_point	Cases other than above or norm_point with current pointer value not equal to receive pointer value.		

<1> Whether the SS bits are checked when a pointer is interpreted can be specified by using the SSM bit of the MDPTRR register, and the expected value to be verified can be set by using the SSR[1:0] bits of the MDPTRR register. In the default mode, the SS bit are not checked.

<2> In the default mode, the condition of incr_ind indication is Three or more I-bits are inverted and three or more D-bits are not inverted and decr_ind indication is Three or more I-bits are inverted and three or more D-bits are not inverted, but this condition can be changed to mach of 8 bits or more of the 10 bits I-bits and D-bits to either the increment and decrement indication. It can be changed by the FJM2 bits of the MDPTRR register.

<3> In the default mode, this operation is executed under the condition that incr_ind, decr_ind, and NDF_enable have not been received in the past three frames. If any of these indications has been received, the indication is Inv_point. This condition can be invalidated by using the FJM2 bit of the MDPTRR register.

<4> Conflict condition

- If the Frequency Justification operation is interpreted but the actual operation involves changing the pointer value to a new value, the pointer value is changed after the Frequency Justification operation.

Table 3-4. Pointer Interpretation History

Indication	Condition
3×norm_point	Three consecutive equal norm_point indication
3×AIS_ind	Three consecutive AIS_ind indication
N×inv_point	**N**<1> consecutive inv_point indication
N×NDF_enable	**N**<1> consecutive NDF_enable indication

<1> N: In the default status, the number of times of reception is nine, but this can be changed to eight or ten times by using the LOPN[1:0] bits of the MDPTRR register.

(c) Pointer processing of H1#2 and H2#2 to H1#12 and H2#12

The indication shown in Table 3-5 is interpreted depending on the NDF, SS bits, and pointer value extracted from the H1#2 and H2#2 to H1#12 and H2#12 bytes.

Table 3-5. Concatenation Interpretation

	Indication	NDF	SS Bits	Pointer
1	conc_ind	Enable	Don't Care	All 1
2	AIS_ind	1111	11	All 1
3	inv_point	Cases other than above		

Table 3-6. Concatenation Interpretation History

Indication	Condition
3×conc_ind	Three consecutive equal conc_ind indication
3×AIS_ind	Three consecutive AIS_ind indication
N×inv_point	**N**<1> consecutive inv_point indication

<1> N: In the default status, the number of times of reception is nine, but this can be changed to eight or ten times by using the LOPN[1:0] bits of the MDPTRR register.

(d) The status transition of in the Bellcere mode

In the Bellcore mode, H1#1 and H2#1 to H1#12 and H2#12 is processed one sequencer and the overall status is decided this one sequencer.

Table 3-7 shows the status transition condition of pointer processing of H1#1 and H2#1, H1#2 and H2#2 to H1#12 and H2#12. Figure 3-11 shows the status transition.

Figure 3-11. Status Transition of Processing (Bellcore MODE)

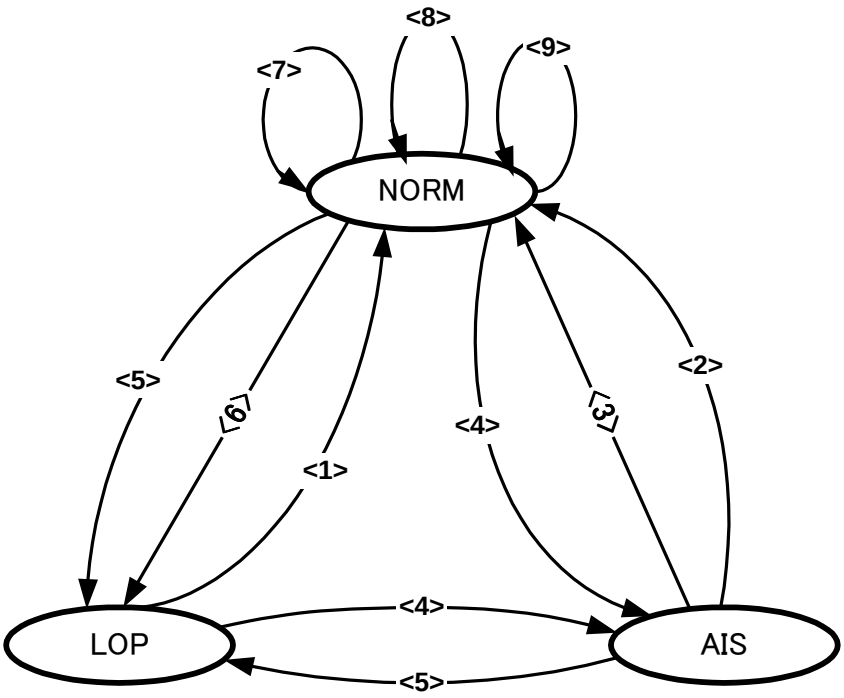


Table 3-7. Status Transition Condition of Pointer Processing of H1#1 and H2#1 to H1#12 and H2#12

Transition	Description	Condition
<1>	LOP → NORM	Reception of 3×norm_point of Pointer Interpretation and Reception of 3×conc_ind of all H1#2 and H2#2 to H1#12 and H2#12 Concatenation Interpretation
<2>	AIS → NORM	Reception of 3×norm_point of Pointer Interpretation and Reception of 3×conc_ind of all H1#2 and H2#2 to H1#12 and H2#12 Concatenation Interpretation
<3>	AIS → NORM	Reception of NDF_enable of Pointer Interpretation and Reception of conc_ind of all H1#2 and H2#2 to H1#12 and H2#12 Concatenation Interpretation
<4>	NORM → AIS LOP → AIS	Reception of 3×AIS_ind of Pointer Interpretation and Reception of AIS_ind of all H1#2 and H2#2 to H1#12 and H2#12 Concatenation Interpretation
<5>	NORM → LOP AIS → LOP	Not reception of 3×norm_point in the N frame of Pointer Interpretation
<6>	NORM → LOP	Reception of N×NDF_enable of Pointer Interpretation
<7>	NORM → NORM	Reception of NDF_enable
<8>	NORM → NORM	Reception of 3×norm_point
<9>	NORM → NORM	Reception of Incr_ind Reception of Decr_ind

<1> In the default mode, reception of 3×conc_ind of all H1#2 and H2#2 to H1#12 and H2#12 Concatenation Interpretation is included in the status transition, but can be excepted by the LOPT bit of the MDPTRR register setting.

<2> In the default mode, reception of 3×conc_ind of all H1#2 and H2#2 to H1#12 and H2#12 Concatenation Interpretation is included in the status transition, but can be excepted by the AIST1 bit of the MDPTRR register setting.

<3> In the default mode, reception of conc_ind of all H1#2 and H2#2 to H1#12 and H2#12 Concatenation Interpretation is included in the status transition, but can be excepted by the AIST2 bit of the MDPTRR register setting.

<4> In the default mode, reception of AIS_ind of all H1#2 and H2#2 to H1#12 and H2#12 Concatenation Interpretation is excepted in the status transition, but can included be by the AISD bit of the MDPTRR register setting.

<5> This transition condition can be changed by the LOPD[2:0] bits of the MDPTRR register. The transition condition is as follow.

LOPD[2:0] bits setting	Transition condition
000 (default)	Not detect 3×norm_point or 3×conc_ind of 1 or more H1#2 and H2#2 to H1#12 and H2#12 Concatenation Interpretation in N frame. (but transition<4> take precedence over transition <5>)
001	Not detect 3×norm_point and 3×conc_ind of all H1#2 and H2#2 to H1#12 and H2#12 Concatenation Interpretation in N frame. (but transition<4> take precedence over transition <5>)
010	Not detect 3×norm_point in N frame. (but transition<4> take precedence over transition <5>)
011	Detect N×Inv_point of H1#1 and H2#1 or N×Inv_point of 1 or more H1#2 and H2#2 to H1#12 and H2#12 Concatenation Interpretation. (but transition<8> take precedence over transition <5>)
100	Detect N×Inv_point of H1#1 and H2#1. (but transition<8> take precedence over transition <5>)

<7><8><9> The transition from NORM to NORM do not represent changes of state but imply offset change.

(e) The status transition of in the ITU-T mode

In the ITU-T mode, the overall status of the pointer changes depending on the status transition caused by the pointer processing of H1#1 and H2#1 and on the status transition of each pointer caused by the concatenation indication processing of H1#2 and H2#2 to H1#12 and H2#12.

Table 3-8 shows the status transition condition of pointer processing of H1#1 and H2#1, H1#2 and H2#2 to H1#12 and H2#12. Figure 3-12 shows the pointer status transition(H1#1 and H2#1). Figure 3-13 shows the concatenation status transition (H1#2 and H2#2 to H1#12 and H2#12). And Figure 3-13 shows the overall status transition.

•Pointer indication processing

H1#1 and H2#1 are independently checked in a pair of H1#1 and H2#1.

The Pointer indication processing is same as the Bellcore mode.

Note: In the ITU-T mode, some option mode must be configured by the MDPTRR register. The configuration is as follow.

Bit	Setting
LOPT	Set to 1
AIST1	Set to 1
AIST2	Set to 1
AISTD	Set to 1
LOPD[2:0]	Set to 100

•Concatenation indication processing

H1#2 and H2#2 to H1#12 and H2#12 are independently checked in a pair of H1#m and H2#m. The NDF, SS bits, and pointer values extracted from each pair of bytes are classified into the following indication and interpreted.

Figure 3-12. Status Transition of Concatenation Indication

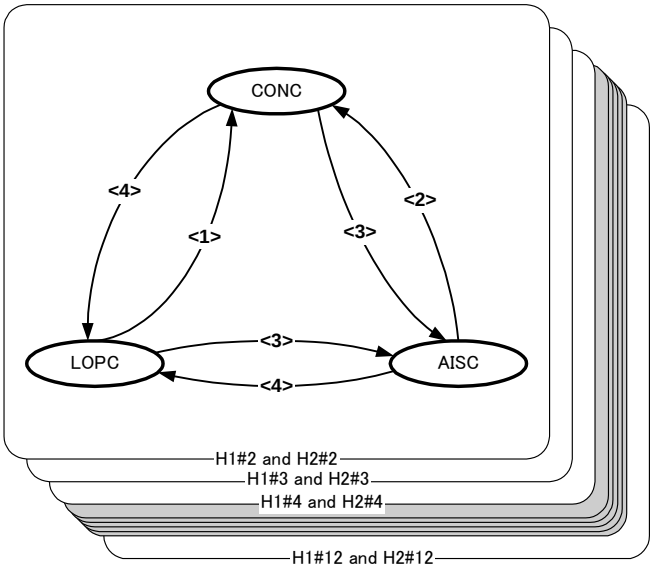


Table 3-8. Status Transition of Concatenation Indication

Transition	Description	Condition
<1>	LOPC → CONC	Reception of 3×conc_ind
<2>	AISC → CONC	Reception of 3×conc_ind or Reception of NDF_enable of pointer indication and reception of conc_ind of all other H1#m and H2#m process
<3>	CONC → AISC	Reception of 3×AIS_ind
	LOPC → AISC	
<4>	CONC → LOPC	Reception of N×inv_point
	AISC → LOPC	

<2> In the default mode, NDF_ind indication status of the H1#1 and H2#1 process and conc_ind indication status of the other H1#2 and H2#2 to H1#12 and H2#12 process is not included for status transition, but can be included by the AISCT bit of the MDPTRR register.

•Overall indication processing

The overall status of the pointer changes depending on the status transition caused by the pointer processing of H1#1 and H2#1 and on the status transition of each pointer caused by the concatenation indication processing of H1#2 and H2#2 to H1#12 and H2#12.

Figure 3-13. Overall Pointer Status Transition

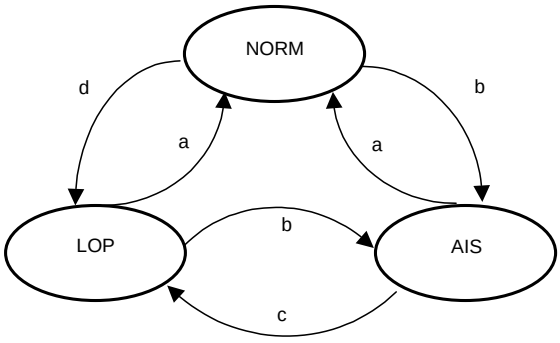


Table 3-9. Overall Pointer Status Transition Condition

Transition	Description	Condition
<a>	LOP → NORM	NORM and CONC in all H1#1 and H2#1 to H1#12 and H2#12
	AIS → NORM	
<b>	NORM → AIS	AIS and AISC in all H1#1 and H2#1 to H1#12 and H2#12
	LOP → AIS	
<c>	AIS → LOP	LOP or LOPC or NORM or CONC in any of H1#1 and H2#1 to H1#12 and H2#12. However, the transition <a> takes precedence.
<d>	NORM → LOP	LOP or LOPC or AIS or AISC in any of H1#1 and H2#1 to H1#12 and H2#12. However, the transition <b> takes precedence.

(f) Pointer action

	condition	Process
New pointer value	Detect 3×norm_point	Change the current value
NDF enable	Detect NDF_enable	Change the current value
Positive frequency justification	Detect incr_ind	Increment the current value
Negative frequency justification	Detect decr_ind	Decrement the current value

For the format of the pointer, see **Figures 3-9**.

(g) Frequency Justification operation

When indication incr_ind(4 in Table 3-3) or decr_ind(5) has been received, the Frequency Justification operation that identifies inversion of the I and D bits by majority is executed.

Note, however, that this operation is executed under the condition that incr_ind, decr_ind, and NDF_enable have not been received in the past three frames. If any of these indications has been received, the indication is Inv_point. This condition can be invalidated by using the FJM1 bit of the MDPTRR register.

- incr_ind: Positive Justification

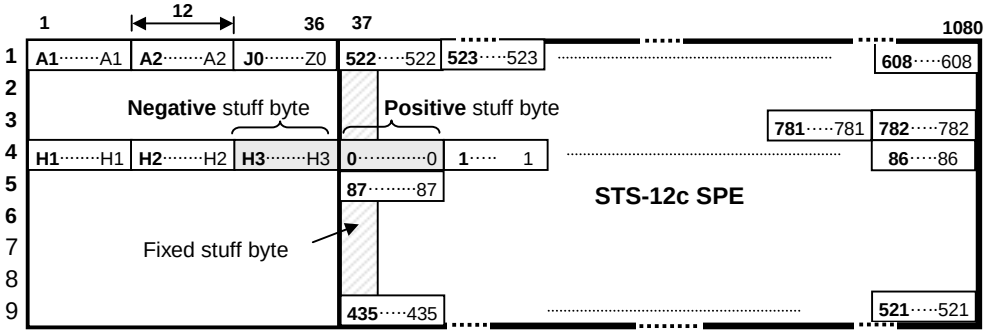
  If it is detected that three or more I bits and up to two D bits of a new pointer are inverted with NDF = Disable, the byte at pointer address 0 is not received as payload data.

- decr_ind: Negative Justification

  If it is detected that up to two I bits and three or more D bits of a new pointer are inverted with NDF = Disable, the H3 byte area is received as payload data.

Note: The indication condition of incr_ind and decr_ind can be changed to mach of 8 bits or more of the 10 bits I-bits and D-bits to either the increment and decrement indication by the FJM2 bit of the MDPTRR register.

- The pointer value is changed to the specified new value after the Frequency Justification operation.



(4) Drop function of received OH byte

The μPD98413 offers the following four means of obtaining the contents of the OH byte in a received frame.

- Drop register
- OH extract interface
- Section and Line DCC extract interface
- Reception of J0/J1 byte trace message

These means are used on the assumption that frame synchronization is established and that reception can be performed normally.

(a) OH drop register

The μPD98413 has drop registers that store the received contents of the following byte areas of the received overhead. The CPU can check the received contents by reading each of these registers via the management interface. For details of the drop registers, see **Section 3.5**.

- OH bytes having drop register
  TOH: K1, K2, E1, E2, F1, D1 through D3, D4 through D12, J0, S1, 1st Z2
  POH: J1, C2, F2, G1, H4, Z3, Z4, Z5

(b) OH extract interface

The μPD98413 has an OH output interface through which a peripheral device can obtain the contents of the OH byte of the received TOH and POH as signals. For details, see **Section 4.4**.

(c) Section and Line DCC extract interface

The μPD98413 has an output interface through which a peripheral device can obtain the contents of the Section and Line DCC as signals. D1 through D3 bytes can be extracted via the Section DCC extract interface, and D4 through D12 bytes can be extracted via the Line DCC extract interface, see **Section 4.4.**

(d) Reception of J0 and J1 trace messages

The μPD98413 stores a 16- or 64-byte trace message in the J0 byte of the SOH or J1 byte of POH, to a dedicated buffer and then reports it to the CPU. If the μPD98413 is instructed to receive a message after the message size and synchronization pattern (start or end pattern of the message) have been specified, it stores a new message when it has detected it from the J0 (J1) byte string of a received OH, and reports this message to the CPU by issuing an interrupt.

For details of the trace message reception function, see **Section 3.6.2**.

(5) Detection of line failure

A function for reporting the events that monitor and detect receive data, such as line failures, alarms, and the degradation of line quality, to the host via registers as OAM (Operation, Administration and Maintenance) information is provided.

- Detection of failure and alarm
- Detection of cause of line quality degradation
- Performance monitoring counter
- Monitoring bit error rate

For details, see **Section 3.4**.

3.2 ATM Function

The μPD98413 can map ATM cells into a SONET/SDH payload. The mapping of ATM cells into a SONET payload is shown below.

Figure 3-14. Mapping of ATM cell

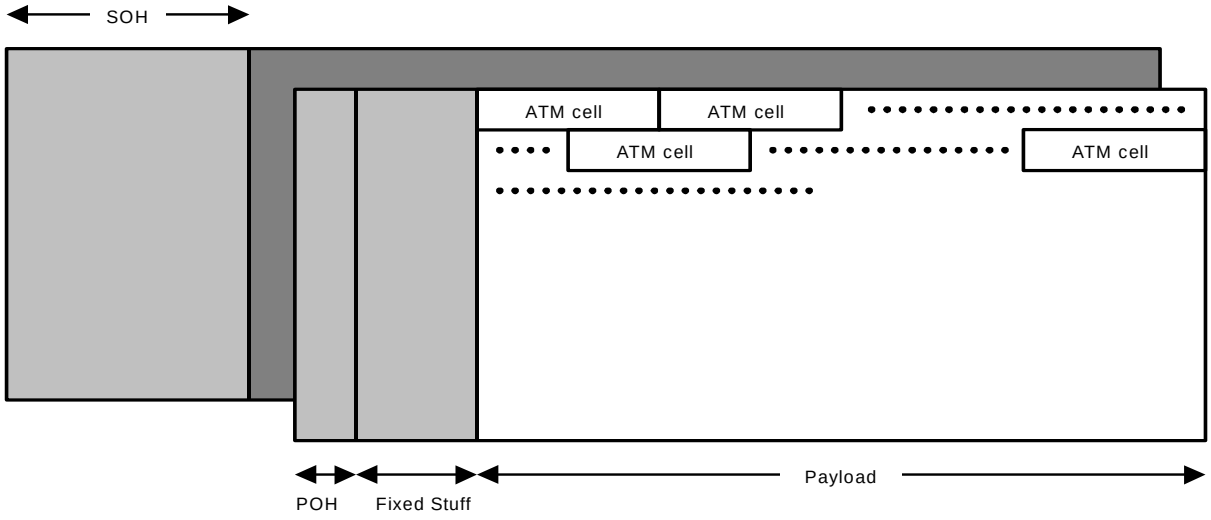
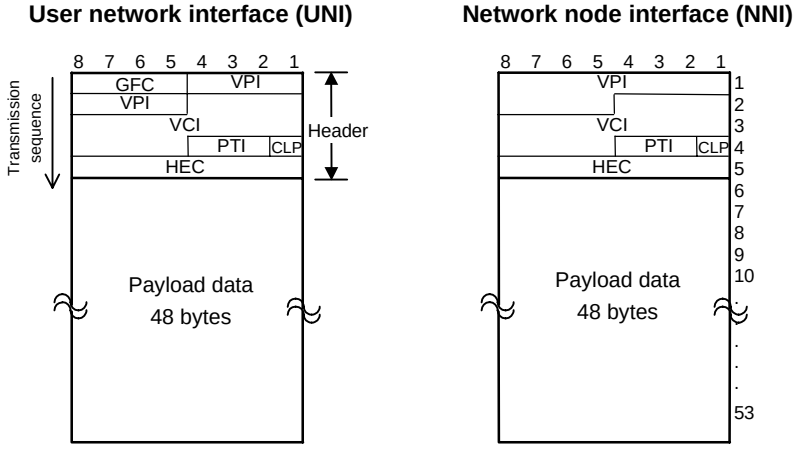


Figure 3-15 shows the format of the ATM cell (user network interface). An ATM cell consists of a 5-byte header and 48-byte payload data. In the case of the user network interface (UNI), the header contains a GFC field (4 bits). In the case of the network node interface (NNI), however, the corresponding field is defined as a VPI field that is 12 bits long.

Figure 3-15. Structure of ATM Cell



GFC: Generic flow control
VPI: Virtual path identifier
VCI: Virtual channel identifier
PTI: Payload type identifier
CLP: Cell loss priority
HEC: Header error control

3.2.1 Transmit ATM function

(a) Cell data reception from ATM device

A cell is received from the high-end ATM device via the ATM interface of 32 bits × 104 MHz MAX and stored to the transmit FIFO, having a capacity of 1K bytes for each port.

Items, below, are related to the mode setting and function of the transmit ATM interface. For details of the ATM interface, see **Section 4.2.**

Selecting format of transmit cell

As the format of the transmit cell that is to be input to TXDATA[31:0], a 52-byte mode that does not include one word of an HEC field, a 56-byte mode that includes one word of an HEC field, and formats in which a TAG field is, or is not, inserted are supported. Before starting the insertion of a cell, the cell format must be matched with the setting of the MDAPIT registers. For details of cell format, See **Section 4.2.2.**

Setting condition to deassert TXCLAV signal that indicates that cell reception is ready

If the transmit FIFO has a vacancy, the TXCLAV signal is asserted to inform the ATM device that the μPD98413 is ready to receive the next cell. If the transmit FIFO is full and the μPD98413 cannot receive the next cell, the TXCLAV signal is deasserted. The number of words (32bit) in the transmit FIFO at which the TXCLAV signal is deasserted can be selected by using the APHIGH[7:0] bits of the FTHT1 register. This setting is useful for connecting an ATM device that cannot immediately stop cell transfer after recognizing that TXCLAV has been deasserted.

Detection of transmit FIFO overflow error

When a transmit FIFO is full and μPD98413 receives next cell, μPD98413 indicates the detection of a transmit FIFO overflow error. The received cell data is ignored and not stored to the transmit FIFO after transmit FIFO overflow occurs. If the transmit FIFO has a vacancy, the detection of the overflow is cleared.

Parity check

At the transmission side of the ATM interface, parity check is performed based on the cell data input to TXDATA[31:0] and parity bit input to TXPRTY. The range of this check is up to when TXENB_B is asserted. The parity is not checked when no cell is input. If a parity error is detected, the PARE bit of the APIET register is set. In the default mode, odd parity calculation is performed, but an even parity can also be used as an option by using the PARM bit of the MDAPIT register.

In addition, the μPD98413 also checks the parity of the data that passes through the transmit FIFO as a self check of its operation. If an error is detected, the PnPEB or PnPEA (n: port No.) bit of the APIPET register is set.

(b) Generation/insertion of HEC

CRC operation is performed on the high-order four bytes of the five bytes of the header of an ATM cell. The value resulting from the operation plus "55H" is inserted to the fifth byte position of the ATM header to carry out HEC (Header Error Control). This HEC Generation can be disabled by the HECO bit of the MDATMT register. If HEC generation is disabled and not inset HEC from ATM device, the HEC Field of ATM Cell is inserted “00h”.

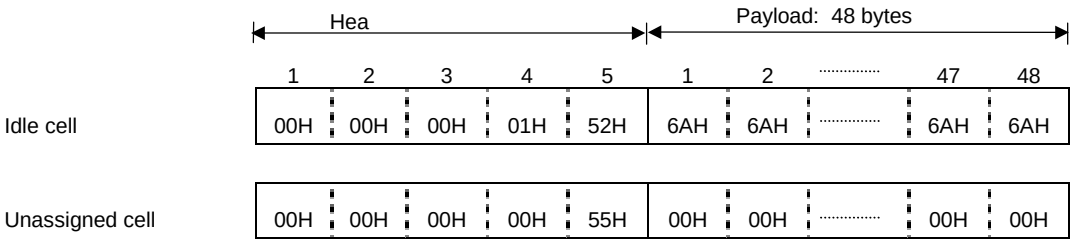
And if HEC generation is disabled and HEC is inserted from ATM device, the HEC field of ATM Cell is inserted the original value that inserted from ATM device.

Polynomial G (X) = $X^8 + X^2 + X + 1$

(c) Inserting an idle cell

If the ATM device does not transmit cell data to the μPD98413 and one cell of data is missing from the transmit FIFO, a vacant (idle) cell is generated and inserted between data cells. The format of the inserted cell can be changed to the unassigned cell format by using the IVCM bit of the MDATMT register. Figure3-16 shows the formats of the idle cell and unassigned cell generated by the μPD98413.

Figure 3-16. Format of Vacant Cell Inserted by *μ*PD98413



(d) Scramble of ATM cell

The data of an ATM cell is scrambled by using the following polynomial. The range of scramble is limited to the 48-byte payload of the ATM cell.

Polynomial G (X) = $X^{43} + 1$

The user can select a scramble stop mode for the purpose of testing. The scramble stop mode is set by the CSCM bit of MDATMT register.

3.2.2 Receive ATM function

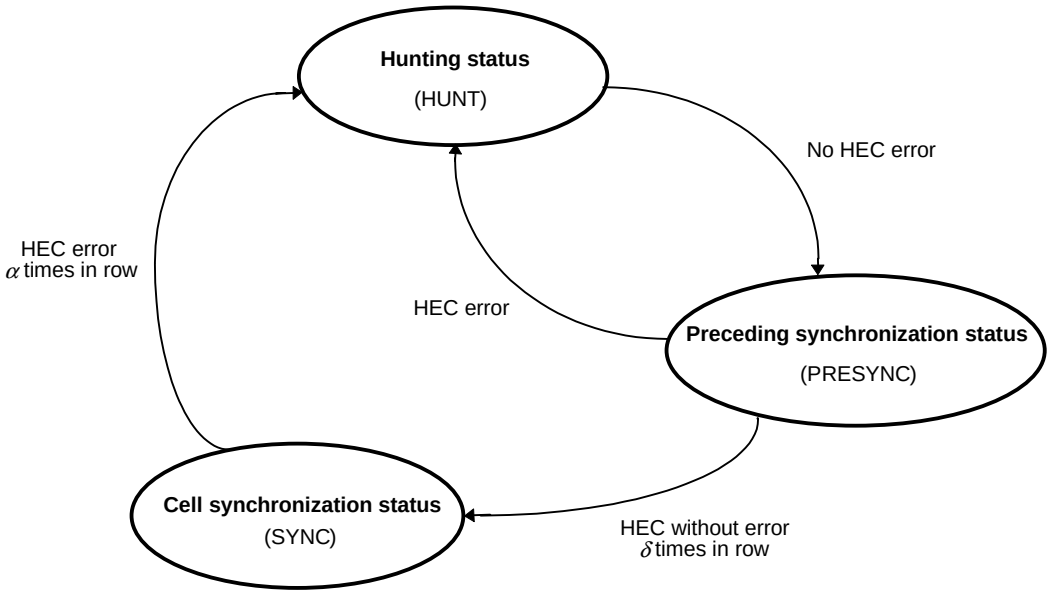
(a) Cell synchronization

Cell synchronization is used to identify a cell boundary and extract an ATM cell from the bit string accommodated in the SPE payload area. The cell boundary is identified by using the header error control (HEC) area for a cell header. The position of a cell is identified by checking CRC calculation of a bit string accommodated in the SPE payload area, shifting the bit string one byte at a time, to check the point at which the syndrome becomes 0. The following polynomial expression is used for this purpose.

$G(X) = X^8 + X^2 + X + 1$

Figure shows the status transition of cell synchronization by means of header error control.

Figure 3-17. Cell Synchronization Status Transition



- The hunting status is that status in which synchronization is not established and a cell boundary is searched. A check of whether an HEC error has occurred is made (CRC (Cyclic Redundancy Check) is conducted with 1 bit each shifted to check whether the remainder is 0.) If HEC coincides and an HEC with no errors is detected, the status changes to the preceding synchronization status.

- In the preceding synchronization (PRESYNC) status, the candidate of a cell boundary is found in the hunting (HUNT) status, and whether this candidate is correct is checked. The μPD98413 enters the cell synchronization status when it has received HEC without an error δ times in a row. It returns to the hunting status if detects an HEC error. The δ th cell that is free from an error is dropped, and the cells are stored to the receive FIFO, starting from the next cell.

- The cell synchronization status (SYNC) is the normal status in which cell synchronization is established. If an HEC error is detected α times in a row, it is considered that cell synchronization is no longer established and the μPD98413 enters the hunting status.

- The number of forward protection stages (α) and the number of backward protection stages (δ) are α = 7 and δ = 6 in the default mode. However, α can be changed by setting the OCDD[1:0] bits of the MDATMR register and δ can be changed by setting the OCDT[1:0] bits.

Table 3-9. Number of Forward/Backward Protection Stages of Cell Synchronization

Number of Forward Protection Stages α	MDATMR Register OCDD[1:0]
6	00
7 (default)	01
8	10
9	11

Number of Backward Protection Stages δ	MDATMR Register OCDT[1:0]
5	00
6 (default)	01
7	10
8	11

- The status in which cell synchronization is not established is reported as the Out Of Cell Delineation (OCD) status. If this status lasts for 4 ms, the μPD98413 enters the Loss Of Cell Delineation (LCD) status. The LCD status is cleared if the cell synchronization status lasts for 4 ms. The 4 ms required to detect and clear the LCD status can be changed to 0 ms by using the LCDDT bit of the MDATMR register to make the condition of detecting and terminating OCD and LCD the same.

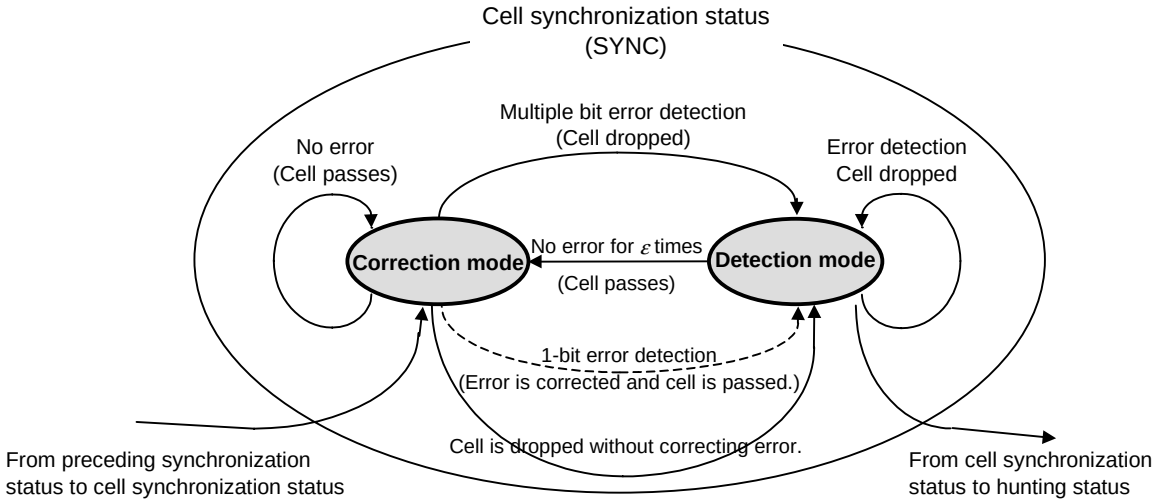
Table 3-10. OCD and LCD Detection Conditions

	Detection Condition	Termination Condition
OCD	If normal HEC cannot be detected in α forward protection stages in a row.	If normal HEC is detected in δ backward protection stages + 1 in a row.
LCD	If OCD lasts for 4 ms. If the LCDDT bit of the MDATMR register is 0, the LCD status is detected at the same time as OCD.	If cell synchronization status lasts for 4 ms. If the LCDDT bit of the MDATMR register is 0, the LCD status is cleared at the same time as OCD.

(b) HEC error control

While cell synchronization is established, a one-bit error of a cell header is corrected and errors of multiple bits are detected by means of header error control (HEC). As a result of the header error control processing, only the valid cell that includes error correction and which does not offer error correction in the header is stored into the receive FIFO and transferred to the ATM interface. Figure 3-18 shows the status transition of header error control.

Figure 3-18. HEC Check Status Transition in Cell Synchronization Status



- An error of only one bit is corrected in the correction mode and then the detection mode is set.
- HEC errors are continuously monitored in the correction mode. If errors are detected α times in a row, the status is changed from the cell synchronization status to the hunting status.
- Whether a 1-bit error is corrected when it has been detected, and the condition in which the mode is changed from detection mode to correction mode can be specified by using the MDATMR register.

Table 3-11. HEC Error Control Mode

Execution of 1-bit error correction of header	MDATMR Register HECCM Bit
None	1
Correction executed (default)	0

Number of stages (ε) for changing mode from detection to correction	MDATMR Register HECDC[1:0] Bits
1 (default)	00
2	01
4	10

(c) Descramble of ATM cell

In the cell synchronization status, the data of the cell is descrambled by the following polynomial. The range of descramble is limited to the payload of the cell.

Polynomial G (X) = $X^{43} + 1$

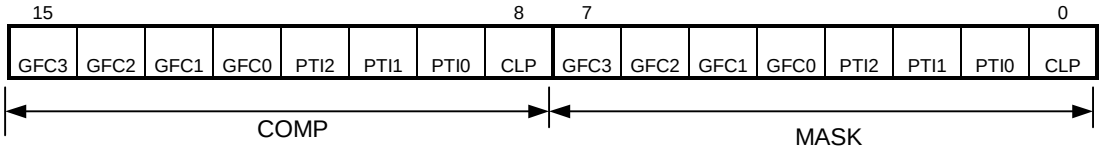
An option mode in which the descrambling of cells can be disabled for testing purposes is supported. To set this mode, use the CSCM bit of the MDATMR register.

(d) Dropping idle and unassigned cells

If an idle cell is detected as a result of monitoring the high-order four bytes of the header of the cell stream extracted from a frame, the cell is not stored into the receive FIFO but is dropped. Patterns other than the VPI/VCI field of the header to be monitored can be changed by using the DCHP register, so that an unassigned cell can be dropped or passed along with the idle cell.

In the default, only CLP bit of the COMP field is set to “1”, therefore only idol cell is dropped. (Unassigned cell is not dropped.)

Figure 3-19. DCHP Register



DCHP Register Setting Examples

COMP Field CLP Bit	MASK Field CLP Bit	Cells to Be Dropped
×	1	Idle and unassigned cells
1	0	Idle cells only (default)
0	0	Unassigned cells only

(e) Output of cell from ATM interface

If cell synchronization is established, a cell that does not fit in the pattern specified by the DCHP register is stored to the receive FIFO as a valid cell. The stored cell is transferred to the ATM device via the ATM interface. If a cell is received when the receive FIFO is full, a receive FIFO overflow error occurs and that cell is dropped. The occurrence of the receive FIFO overflow error can be used as an interrupt cause.

3.3 POS FUNCTIONS

The μPD98413 can map POS packets into a SONET/SDH payload. POS packet processing is performed according to HDLC frame processing. The following is an overview of POS packet processing.

On the sending end, the μPD98413 performs HDLC processing on the packet data entered from the POS interface and maps it as POS packets into a SONET payload, inserting a flag sequence (7Eh) between packets.

On the receiving end, the μPD98413 extracts POS packets from the SONET frame payload entered from the line interface, based on the flag sequence (7Eh). It then performs HDLC processing on the POS packets and sends them to the POS interface.

The mapping of POS packets into a SONET payload and the POS packet format are shown below.

Figure 3-20. Mapping of POS Packets

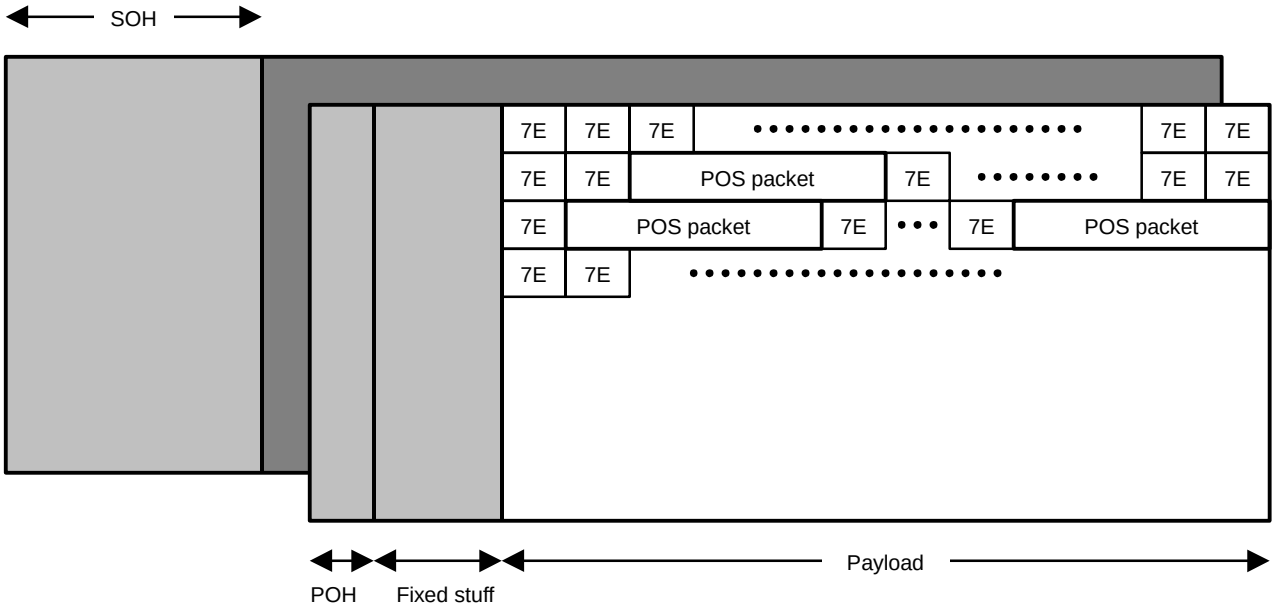
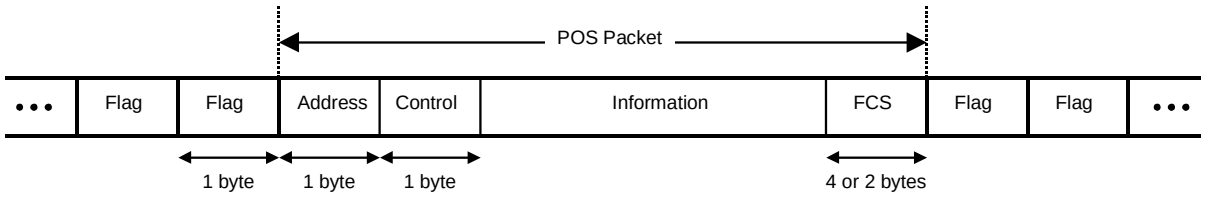


Figure 3-21. POS Packet Format



3.3.1 Transmission POS functions

The transmission POS processor of the μPD98413 performs HDLC processing on the packet data entered from the POS interface and maps it into a SONET payload. If there are no POS packets to be mapped, a flag sequence (7Eh) is inserted. The functions, which are executed in the following order, are described in detail below.

Address and control byte generation → FCS generation → Byte stuffing → Data scrambling

(a) Address and control byte generation

The μPD98413 adds an address byte and a control byte at the beginning of packet data. The address and control bytes added by the μPD98413 are fixed to the following values:

Address byte = FFh, control byte = 03h

The address and control byte generation function is optional and it may be disabled by the ADRM bit of the MDPOST register.

(b) FCS generation

The μPD98413 executes an FCS operation (CRC-32 or CRC-CCIT operation) on the entire packet data and adds an FCS field to the end of the POS packet. The user can select between a 32-bit FCS and a 16-bit FCS for the FCS field to be added by the μPD98413. And user can selects the FCS calculation order whether it is calculated from the LSB or MSB of the transmit packet.

The polynomials used to generate them are as follows:

32-bit FCS (CRC-32):

$g(x) = 1 + x + x^2 + x^4 + x^5 + x^7 + x^8 + x^{10} + x^{11} + x^{12} + x^{16} + x^{22} + x^{23} + x^{26} + x^{32}$

16-bit FCS (CRC-CCIT):

$g(x) = 1 + x^5 + x^{12} + x^{16}$

If the address and control byte generation function is enabled, FCS operation is executed on the entire packet data, including the address and control bytes.

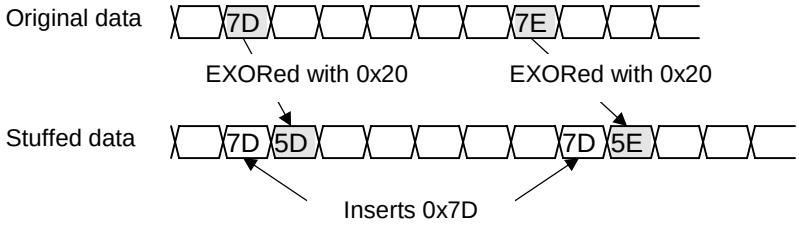
The FCS generation function is optional and it may be disabled by the FCSM bit of the MDPOST register.

(c) Byte stuffing

The μPD98413 supports a byte stuffing function. Upon detecting a 7Dh or 7Eh byte in a POS pocket, the byte stuffing of the μPD98413 inserts 7Dh (control escape) before that byte, and EXORs the detected 7Dh or 7Eh byte with 20h. The data resulting from byte stuffing is as shown below.

Original data	Stuffed data
7D	7D-5D
7E	7D-5E

Figure 3-22. Byte Stuffing



(d) Data scrambling

The μPD98413 scrambles the entire SONET payload including the POS packets and flag sequences (excepted POH and Fixed stuff). The polynomial used for scrambling is as follows:

$g(x) = 1 + x^{43}$

The scrambling function is optional and it may be disabled by the PSCM bit of the MDPOST register.

(e) SONET overhead byte for POS

In PPP over SONET, the values of the C2 and H4 bytes of the SONET overhead bytes are defined. Set the transmission C2 and H4 byte registers to the following values:

C2 byte: 16h when scrambling is used
CFh when scrambling is not used

H4 byte: 00h (Default value of register)

(f) Error processing and transmission of an abort packet

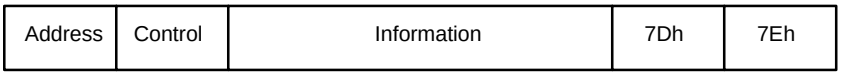
This section shows the processing of μPD98413 when the following errors occur in the transmit side.

- Transmission FIFO overflow
- Transmission FIFO underflow
- The next start-of-packet notification is received before an end-of-packet notification
- The TERR signal is asserted

Upon detecting any of the following errors, the μPD98413 sends a POS packet as an abort packet. 7Dh and 7Eh are inserted at the end of the packet as the abort packet.

- Transmission FIFO underflow
- The TERR signal is asserted

Figure 3-23. Abort Packet



Transmission FIFO overflow

If a transmission FIFO overflow occurs during packet transmission (the transmission FIFO overflows before TEOP is asserted), the μPD98413 sends all the data that remains in the transmission FIFO at that point. The μPD98413 also indicates the error and interrupt when a transmission FIFO overflow occurs.

If, after a transmission FIFO overflow occurs, the remaining data for that packet is entered (the data is entered without TSOP being asserted), the μPD98413 discards that data.

Transmission FIFO underflow

If a transmission FIFO underflow occurs during packet transmission (the transmission FIFO becomes empty before TEOP is asserted), the μPD98413 inserts 7Dh and 7Eh after the data sent before the underflow occurs, and sends the data as an abort packet. The μPD98413 also indicates the error and interrupt when a transmission FIFO underflow occurs.

If, after a transmission FIFO underflow occurs, the remaining data for that packet is entered (the data is entered without TSOP being asserted), the μPD98413 discards that data.

The next start-of-packet notification is received before an end-of-packet notification (EOP error)

If the next start-of-packet notification is received before an end-of-packet notification during packet transmission (the TSOP of the next packet is asserted before TEOP is asserted), the μPD98413 indicates the error and interrupt.

TERR signal is asserted

If the TERR signal is asserted during packet transmission, the μPD98413 inserts 7Dh and 7Eh and sends the data as an abort packet.

(g) Performance monitors

The μPD98413 supports the following performance counters. All the counters are 32-bit counters.

- Transmit valid packet counter
- Transmit abort packet counter
- Transmit FIFO underflow packet counter

Transmit valid packet counter

Upon sending a valid packet (packet other than abort packets), the μPD98413 increments the transmit valid packet counter. This counter is selectable in units of packets or bytes by the VPCTM bit of the MDCNTT register.

Transmit abort packet counter

Upon sending an abort packet, the μPD98413 increments the send abort packet counter. This counter includes the counts of the abort packet due to a transmit FIFO underflow and TERR is asserted. See the description above for details of the transmission of an abort packet.

Transmit FIFO underflow packet counter

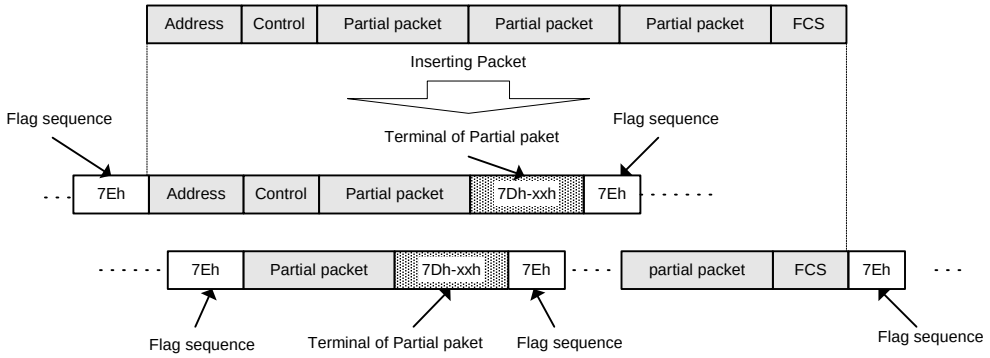
The μPD98413 increments the transmit FIFO underflow packet counter when a transmit FIFO underflow occurs during packet transmission.

(h) Packet Inserting SONET Payload on HALT mode

The μPD98413 supports the HALT mode, which enables to transmit the fragmentary packet.

The data “7Dh-xxh” is terminal flag for the partial packet. If this flag is asserted, the packet insert is paused. And insert data “7Eh” continually. Then if the μPD98413 can be mapping the POS data for SONET payload, that data is insert as the next partial packet. In default, this mode is disabled. It is enabled by the HALTM bit of the MOPOST register.

Figure 3-24 Packet insert on HALT mode (Transmit)



Name	Value
Flag sequence	7Eh
Terminal of Partial paket	7Dh-xxh (xx is the value, which set by the STPN[7:0] bits of the HPTNT register.)

3.3.2 Reception POS functions

The reception POS processor of the μPD98413 extracts POS packets from the SONET frame payload entered from the line interface, based on the flag sequence (7Eh). The μPD98413 recognizes a packet boundary by detecting a flag sequence (7Eh). It then performs HDLC processing on the POS packets and sends them to the POS interface. The functions, which are executed in the following order, are described in detail below.

Data descrambling → Byte destuffing → Address and control check → Packet size check → FCS check

(a) Data descrambling

The μPD98413 descrambles the entire SONET payload containing the POS packets and flag sequences. The polynomial used for descrambling is as follows:

$g(x) = 1 + x^{43}$

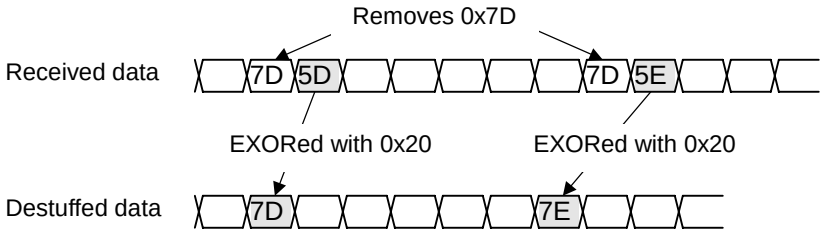
The descrambling function is optional and it may be disabled by the PSCM bit of the MDPOSR register.

(b) Byte destuffing

The μPD98413 supports the byte destuffing function. Upon detecting a 7Dh (control escape) byte in a POS packet, the byte destuffing of the μPD98413 deletes that byte, and EXORs the next byte with 20h. The data resulting from byte destuffing is as shown below.

Stuffed data	Destuffed data (Original)
7D-5D	7D
7D-5E	7E

Figure 3-25. Byte Destuffing



Remark If 7D-7Eh bytes are detected in a POS packet, the μPD98413 does not perform byte destuffing. That packet is processed as an abort packet.

The μPD98413 also performs byte destuffing if the byte following the control escape (7Dh) is not 5Dh, 5Eh, or 7Eh.

(c) Address and control bytes check

Upon receiving a packet, the μPD98413 detects the Address and control fields in the packet (first byte of the POS packet) and checks it. If the value in the Address field of the packet is not FFh or the control field is not 03h, the packet is handled as an address error packet, and the address error counter is incremented. The address error packet is discarded internally, without being sent to the POS interface. If the address error does not occur, μPD98413 sends the packet stripped the address and control bytes or not stripped, which is the setting by the ADRPAS bit of the MDPOSR register, to the POS interface.

The address and control error detection function is optional and it may be disabled by the ADRM bit of the MDPOSR register.

(d) Packet size check

The μPD98413 monitors the packets for both minimum and maximum size errors. The domain checked is only an Information domain except address byte, control byte, and FCS. Each error is indicated by the interrupt and the error counter. The packet size check function is optional and it may be disabled by the MDPOSR register.

Short size packet error

The μPD98413 allows you to set the minimum receive packet size in the PRENR1 register. If receiving a packet whose size is below the minimum, the μPD98413 increments the short size packet counter and indicates it by the interrupt. If receiving such a short size packet, the μPD98413 outputs it as an error packet from the POS interface. At the end of the packet, the RERR pin is asserted for notification. The Short packet size check function, it may be disabled by the SPM bit of the MDPOSR register.

Long size packet error

The μPD98413 allows you to set the maximum receive packet size in the PLENR2 register. Upon receiving a packet whose size exceeds the maximum, the μPD98413 increments the long size packet counter and indicates it by the interrupt. Upon receiving such a long size packet, the μPD98413 outputs it as an error packet from the POS interface. At the end of the packet, the RERR pin is asserted for notification. The remaining data for the packet exceeding the maximum is discarded internally. The Long packet size check function, it may be disabled by the LPM bit of the MDPOSR register.

(e) Detection of abort packet

Upon receiving an abort packet (which ends with abort sequence 7D-7E), the μPD98413 increments the receive abort packet counter and indicates it by the interrupt. The received abort packet, which is stripped an abort sequence (7D-7E), is output from the POS interface. At the end of the packet, the RERR pin is asserted for notification.

(f) FCS check

The μPD98413 executes an FCS operation (CRC-32 or CRC-CCIT operation) on the entire packet data and then performs an FCS check. The user can select between a 32-bit FCS and a 16-bit FCS for the FCS check. The polynomial for each is as follows:

32-bit FCS (CRC-32):

$g(x) = 1 + x + x^2 + x^4 + x^5 + x^7 + x^8 + x^{10} + x^{11} + x^{12} + x^{16} + x^{22} + x^{23} + x^{26} + x^{32}$

16-bit FCS (CRC-CCIT):

$g(x) = 1 + x^5 + x^{12} + x^{16}$

After performing the FCS check, the μPD98413 sends the packet stripped the FCS or not stripped, which is the setting by the FCSPAS bit of the MDPOSR register, to the POS interface. When the FCS is not stripped, the μPD98413 places the results of the FCS operation in the FCS field. If no FCS error occurs, the value in the FCS field is zero.

If an FCS error occurs, this is reported by asserting the RERR pin at the end of the packet. The μPD98413 also increments the FCS error counter and indicates it by the interrupt.

The FCS check function is optional and it may be disabled by the FCSM bit of the MDPOSR register.

(g) Performance monitors

The μPD98413 supports the following receive error handling and performance counters. Each counter is described below. All the counters are 32-bit counters.

- Receive valid packet counter
- Receive abort packet counter
- Receive Address error counter
- Receive FCS error counter
- Receive FIFO overflow counter
- Receive short size packet counter
- Receive long size packet counter

Receive valid packet counter

Upon receiving a packet without an error, the μPD98413 increments the receive packet counter. This counter is selectable in units of packets or bytes, and it may be selected by the VPCRM bit of the MDCNTR register.

Receive abort packet counter

Upon receiving an abort packet (which ends with abort sequence 7D-7E), the μPD98413 increments the receive abort packet counter.

Receive Address error counter

Upon receiving a packet, the μPD98413 detects the Address and control fields in the packet (first byte of the POS packet) and checks it. If the value in the Address field of the packet is not FFh or the control field is not 03h, the packet is handled as an address error packet, and the address error counter is incremented.

Receive FCS error counter

Upon detecting an FCS error, the μPD98413 increments the FCS error counter.

Receive FIFO overflow counter

If a receive FIFO overflow occurs, the μPD98413 increments the reception FIFO overflow counter. If a reception FIFO overflow occurs while a packet is being received, the μPD98413 outputs it from the POS interface as an error packet. At the end of the packet, the RERR pin is asserted for notification. The remaining data for the packet that is entered after the reception FIFO overflow occurs is discarded internally.

After a reception FIFO overflow occurs, the μPD98413 does not resume reception until a certain amount of free area (settable in an appropriate register, programmable) is reserved in the reception FIFO. Any new packet that otherwise would be received during the suspended reception is discarded internally (as in the case where a reception FIFO overflow occurs at the beginning of a packet). In this case too, the reception FIFO overflow counter is incremented.

Short size packet counter

The μPD98413 allows you to set the minimum receive packet size (settable in an appropriate register, programmable). If receiving a packet whose size is below the minimum, the μPD98413 increments the short size packet counter.

Long size packet counter

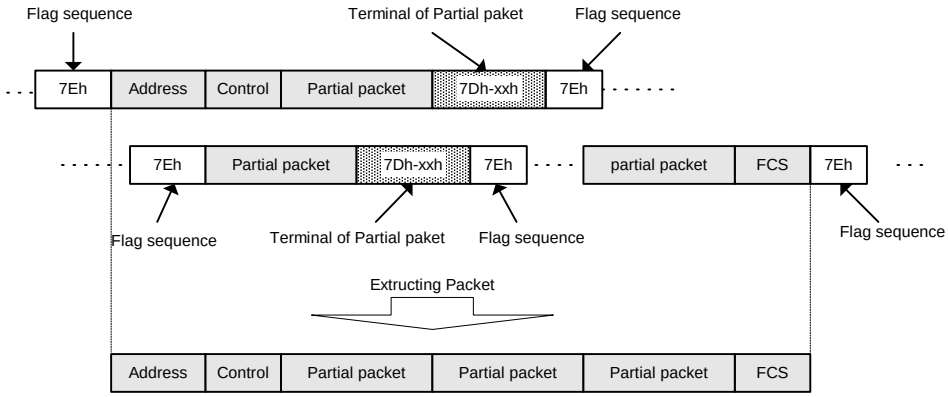
The μPD98413 allows you to set the maximum receive packet size (settable in an appropriate register, programmable). Upon receiving a packet whose size exceeds the maximum, the μPD98413 increments the long size packet counter.

(h) Packet Extracting from SONET payload on HALT mode

The μPD98413 supports the HALT mode, which enables to receive the fragmentary packet.

In default, this mode is disabled. It can be enable by the HALTM bit of the MOPOSR register. The data “7Dh-xxh” is terminal flag for the partial packet. If this flag is asserted, the packet extract is paused. Then if expect data except “7E”, that data is recognized as the next partial packet.

Figure 3-26. Packet Extracting on HALT mode



Name	Value
Flag sequence	7Eh
Terminal of Partial paket	7Dh-xxh (xx is the value, which set by the STPN[7:0] bits of the HPTNR register.)

3.4 OAM Function

The μPD98413 has an OAM (Operation, Administration, Maintenance) function to maintain and monitor the network. This section explains the OAM functions supported by the μPD98413.

3.4.1 Transmitting Alarm

Alarm information is set in a specific overhead area of a transmit frame and sent. The alarm information can be transmitted by using a register, by inputting a signal to the alarm transmission command pin, or automatically depending on the line status at the reception side.

Table 3-12. Transmitting an Alarm

Alarm		Transmitting/Terminating Method	Transmit Frame
(1)	APS	**<1>** Set the K12T register. **<2>** Set the K1 and K2 bytes from the OH insert interface.	The contents of the K12T register are loaded to the positions of the K1 and K2 bytes and transmitted each time a frame is sent.
(2)	Line AIS	**<1>** Set the LAIS bits of the CMALM register. **<2>** Input a signal to the TALM pins.	All the bits other than those in the SOH area (LOH + POH + SPE areas) are set to "1".
(3)	Path AIS	**<1>** Set the PAIS bits of the CMALM register. **<2>** Input a signal to the TALM pins.	All the H1, H2, and H3 bytes and all the bits in the SPE area before frame scramble are set to "1".
(4)	Line RDI	**<1>** Sets the LRDI bits of the CMALM register. **<2>** Input a signal to the TALM pins. **<3>** Automatic transmission due to occurrence of an internal cause.	Bits 6 to 8 of the K2 byte of the OH byte are "110".
(5)	Path RDI	**<1>** Sets the PRDI bits of the CMALM register. **<2>** Input a signal to the TALM pins. **<3>** Automatic transmission due to occurrence of an internal cause.	One-bit RDI: Bit 5 of the G1 byte of the OH byte is "1". Enhanced RDI: Bit 5-7 of the G1 byte of the OH byte is the corresponding alarm.

If an attempt is made to transmit two or more alarms at the same time, or if an attempt is made to transmit another alarm while Line RDI or Path RDI is automatically returned and transmitted, the priority is as follows:

Table 3-13. Priority of Alarm Transmission

	Line AIS	Path AIS	Line RDI	Path RDI	APS
Line AIS		Line AIS	Line AIS	Line AIS	Line AIS
Path AIS	Line AIS		Can be set simultaneously.	Path AIS	Can be set simultaneously.
Line RDI	Line AIS	Can be set simultaneously.		Can be set simultaneously.	Line RDI
Path RDI	Line AIS	Path AIS	Can be set simultaneously.		Can be set simultaneously.
APS	Line AIS	Can be set simultaneously.	Line RDI	Can be set simultaneously.	

(1) Transmitting the APS (Automatic Protection Switching) code

The APS function is provided to switch a signal into an auxiliary signal in case a line fails. The switching operation is requested, confirmed, or acknowledged by using the K1 and K2 bytes in OH in a line-multiplexed zone and by using the commands and protocols defined by ANSI T1.105.01 or ITU-T G.783. Transmission method is as follows:

- **Transmitting/Terminating method**

  Set the APS signal to be transferred to the K12T register of the OH insert register. The μPD98413 loads the contents of the K12T register to the positions of the K1 and K2 bytes and transmits them each time it has transmitted a frame. To change or clear the contents of the APS signal, change the contents of the K12T register. The contents of the K1 and K2 bytes can also be input from the OH insert interface.

  Bits 6 to 8 of the K2 byte are also used to transmit alarm Line RDI or Line AIS. If the transmission of alarm Line RDI or Line AIS is specified, the setting of K2T[2:0], the portion of the K12T register equivalent to these bits, is ignored and alarm transmission takes precedence.

  Bits 6 to 8 of the K2 byte are also ignored even when they are input from the OH insert interface.

(2) Transmitting Line AIS (Line Alarm Indication Signal)

Line AIS is a line alarm indication signal that detects a failure in the upstream and sends an alarm to the downstream during relaying.

- **Transmitting / Terminating method**

  The Line AIS frame can be transmitted in the following two ways. The frame is transmitted or terminated by observing the boundary of the frame.

  <1> Set the LAIS bit of the CMALM register to 1. While this bit is set to 1, the Line AIS frame is transmitted.

  <2> Drive the TALM pins to the Line AIS code. While these pins are set to the Line AIS code, the Line AIS frame is transmitted. **See section 4.7**

- **Line AIS frame**

  This frame has "1" in all the bits of all the areas (LOH + POH + SPE) of a transmit frame, except the SOH area.

(3) Transmitting Path AIS (Path Alarm Indication Signal)

Path AIS is a Path Alarm Indication Signal that is reported to the downstream when a failure is detected in the upstream and alarm is issued during relaying.

- **Transmitting/Terminating method**

  The Path AIS frame can be transmitted in the following two ways. The frame is transmitted or cleared by observing the boundary of the frame.

  <1> Set the PAIS bit of the CMALM register to 1. While this bit is set to 1, the Path AIS frame is transmitted.

  <2> Drive the TALM pins to the Path AIS code. While these pins are set to the Path AIS code, the Path AIS frame is transmitted.

- **Path AIS frame**

  This frame has "1" in all the H1, H2, and H3 bytes of the AU pointer of the OH byte of a transmit frame, and all the bits in the SPE area (POH and payload) before frame scramble.

(4) Transmitting Line RDI (Line Remote Defect Indication)

Line RDI is a signal that reports detection of a line receive failure (LOS, LOF, or Line AIS) to a unit in the upstream.

- **Transmitting/Terminating method**

  The Line RDI frame can be transmitted in the following three ways. The frame is transmitted or cleared by observing the boundary of the frame.

  <1> Automatic return transmission

  The Line RDI frame is automatically transmitted if any of the events of LOS, LOF, and Line AIS is detected at the reception side. When the μPD98413 has recovered from the event, it resumes transmitting the ordinary frame, but μPD98413 guarantees to generate the Line RDI frame for at least 20 frames. This function is enabled in the default mode, but can be disabled by using the ALRDIM bit of the MDLOHT register.

  <2> Set the LRDI bit of the CMALM register to 1. While this bit is set to 1, the Line RDI frame is transmitted.

  <3> Drive the TALM pins to the Line RDI code. While these pins are set to the Line RDI code, the Line RDI frame is transmitted.

- **Line RDI frame**

  This frame has "110" in bits 6 to 8 of the K2 byte of the OH byte.

(5) Transmitting Path RDI (Path Remote defect Indication)

Path RDI is a signal that reports detection of a path receive failure to a unit in the upstream. μPD98413 supports two modes of One-bit RDI and Enhanced RDI. This mode can be selected by the PRDIM bit of the MDPOHT register.

One-bit Path RDI

- **Transmitting/Terminating method**

  The One-bit Path RDI frame can be transmitted in the following three ways. The frame is transmitted or cleared by observing the boundary of the frame.

  <1> Automatic return transmission

  The One-bit Path RDI frame is automatically transmitted if any of the events of LOS, LOF, Line AIS, LOP, Path AIS, and (LCD) is detected at the reception side.

  When the μPD98413 has recovered from the event, it resumes transmission have the ordinary frame (Bit5 of G1 byte is “0”), but μPD98413 guarantees to generate the One-bit Path RDI frame for at least 20 frames. This function is enabled in the default mode, but can be disabled by using the APRDIM bit of the MDPOHT register. LCD is not included in the condition of automatic transmission of the One-bit Path RDI in the default mode, but can be included in the condition by using the LCDO bit of the MDPOHT register.

  <2> Set the PRDI field of the CMALM register to 001. While this field is set to 001, the One-bit Path RDI frame is transmitted.

  <3> Drive the TALM pins to the One-bit Path RDI code. While these pins are set to the One-bit Path RDI code, the One-bit Path RDI frame is transmitted.

- **One-bit Path RDI frame**

  This frame has "1" in bit 5 of the G1 byte of the OH byte.

Enhanced Path RDI

- **Transmitting/clearing method**

The Enhanced Path RDI frame can be transmitted in the following three ways. The frame is transmitted or cleared by observing the boundary of the frame.

<1> Automatic return transmission

The corresponding Enhanced Path RDI frame is automatically transmitted if the following events are detected at the reception side.

G1 bit5-7	Priority	Trigger	Interpretation
001	4	No defects	No RDI-P defect
010	3	Path PLM, (LCD option)	ERDI-P Payload defect
101	1	LOS, LOF, Line AIS, Path AIS, LOP	ERDI-P Server defect
110	2	Path UNEQ, (Path TIM, Path TIU option)	ERDI-P Connectivity defect

When the μPD98413 has recovered from the event, it resumes transmission of the ordinary frame (Bit5-7 of G1 byte are “001”), but μPD98413 guarantees to generate the Enhanced Path RDI frame for at least 20 frames. When a higher priority incoming defect is detected before the Enhanced Path RDI code for a lower priority has been sent for 20 frames, μPD98413 changes the Enhanced Path RDI code to a higher priority code from a lower priority code, and not guarantee a lower priority code for 20 frames. This function is enabled in the default mode, but can be disabled by using the APRDIM bit of the MDPOHT register.

● LCD is not included in the condition of automatic transmission of ERDI-P Payload defect in the default mode, but can be included in the condition by using the LCDO bit of the MDPOHT register. LCD also is invalid in the POS mode.

● Path TIM is not included in the condition of automatic transmission of ERDI-P Connectivity defect in the default mode, but can be included in the condition by using the PTIMO bit of the MDPOHT register.

● Path TIU is not included in the condition of automatic transmission of ERDI-P Connectivity defect in the default mode, but can be included in the condition by using the PTIUO bit of the MDPOHT register.

<2> Set the PRDIC field of the CMALM register to the following value. While this field is set to the following value, the following Enhanced Path RDI frame is transmitted.

PRDI field	G1 bit5-7	Interpretation
000, 100, 101, 110, 111	001	No RDI-P defect
100	010	ERDI-P Payload defect
101	101	ERDI-P Server defect
110	110	ERDI-P Connectivity defect

<3> Drive the TALM pins to the following code. While these pins are set to the following code, the following Enhanced Path RDI frame is transmitted.

TALMCx-TALMAx pins	G1 bit5-7	Interpretation
000	001	No RDI-P defect
100	101	ERDI-P Server defect
101	110	ERDI-P Connectivity defect
110	010	ERDI-P Payload defect

- **Enhanced Path RDI frame**

This frame has the above value in bit 5-7 of the G1 byte of the OH byte.

3.4.2 Detection of Alarm and Failure

Table 3-14 lists the failures and alarms monitored by the μPD98413. If any of these events has been detected, the following actions are taken.

<1> The corresponding bit of the interrupt cause register is set.
The CPU identifies the event that has occurred by reading the register.

<2> An interrupt signal is asserted active to report the host.
Whether an interrupt signal corresponding to each event is asserted active (mask, unmask) can be selected.

<3> The corresponding pin is asserted active.
If an event occurs, the corresponding alarm output pin (RALM pins) goes high to report the external peripheral device.

Table 3-14. Alarms and Failures (1/4)

LOS (Loss Of Signal)
Receive signal lost status Detection: See section 3.1.2 (Table 3-2) Termination: See section 3.1.2 (Table 3-2)
OOF (Out Of Frame)
Frame non-synchronization Detection: If a frame synchronization pattern cannot be detected α times in a row at the positions of the A1 and A2 bytes. Termination: If a frame synchronization pattern is detected δ times in a row. * α = 3, 4, 5, or 6, δ = 2, 3, or 4. These values can be selected by using the OOFD[1:0] and OOFT[1:0] bits of the MDSOHR register. In the default mode, α = 4 and δ = 2.
LOF (Loss Of Frame)
Frame lost status Detection: If OOF status lasts for T ms Termination: If not OOF status lasts for T ms * T = 3 ms or 0 ms. This can be selected by using the LOFDT bit of the MDSOHR register. In the default mode, T = 3 ms. When T = 0 ms, the detection/clearing condition is the same as that of OOF.

Table 3-14. Alarms and Failures (2/4)

Section TIM (Section Trace Identifier Mismatch)
Section trace identifier mismatch. Detection: See **Section 3.6**. Termination: See **Section 3.6**.
Section TIU (Section Trace Identifier Unstable)
Section trace identifier unstable. Detection: See **Section 3.6**. Termination: See **Section 3.6**.
Line AIS (Line Alarm Indication Signal)
Line alarm indication signal. Detects occurrence of Line AIS in unit of transmission source (upstream). Detection: If frames with K2 byte (bits 6 to 8) being "111" are received n times continuously Termination: If frames with K2 byte (bits 6 to 8) not being "111" are received n times continuously * n = 3 or 5. This can be selected by using the LAISDT bit of the MDLOHR register. In the default mode, n = 5.
Line RDI (Line Remote Defect Indication)
Line remote reception failure information. Indicates detection of line reception failure (LOS, LOF, or Line AIS) in unit of transmission destination (downstream). Detection: If frames with K2 byte (bits 6 to 8) being "110" are received n times continuously Termination: If frames with K2 byte (bits 6 to 8) being other than "110" are received n times continuously * n = 3 or 5. This can be selected by using the LRDIDT bit of the MDLOHR register. In the default mode, n = 5.
PSBF (Protection Switching Byte Failure)
Protection switching byte failure. Detection: See **Section 3.4.4**. Termination: See **Section 3.4.4**.
SD (Signal Degrade)
Signal degrade. Detection: **Section 3.4.5**. Termination: **Section 3.4.5**.
SF (Signal Failure)
Signal failure. Detection: **Section 3.4.5**. Termination: **Section 3.4.5**.
LOP (Loss Of Pointer)
Pointer error detection. Detection: See **(3)** in **Section 3.1.2**. Termination: See **(3)** in **Section 3.1.2**.
Path AIS (Path Alarm Indication Signal)
Path alarm indication signal. Detects occurrence of Path AIS in unit of transmission source (upstream). Detection: See **(3)** in **Section 3.1.2**. Termination: See **(3)** in **Section 3.1.2**.

Table 3-14. Alarms and Failures (3/4)

Path RDI (Path Remote Defect Indication)
Path remote reception failure information. Indicates detection of path reception failure in unit of transmission destination (downstream). μPD98413 supports two modes of One-bit RDI and Enhanced RDI. This mode can be selected by the PRDIM bit of the MDPOHR register. **One-bit Path RDI** Detection: If frames with bit 5 of G1 byte being "1" are received n times continuously Termination: If frames with bit 5 of G1 byte being "0" are received n times continuously * n = 3, 5, or 10. This can be selected by using the PRDIDT[1:0] bits of the MDPOHR register. In the default mode, n=10. **Enhanced Path RDI** Detection: If frames with bit 5 to 7 of G1 byte being the following values are received n times continuously "010" : ERDI-P Payload defect "101", "100" and "111" : ERDI-P Server defect "110" : ERDI-P Connectivity defect Termination: If frames with bit 5 to 7 of G1 byte being the following values are received n times continuously ERDI-P Payload termination : The values other than "010" ERDI-P Server termination : The values other than "101", "100" and "111" ERDI-P Connectivity termination : The values other than "110" * n = 3, 5, or 10. This can be selected by using the PRDIDT[1:0] bits of the MDPOHR register. In the default mode, n=10.
Path PLM (Path Payload Label Mismatch)
Path payload label mismatch. Detection: See **Section 3.4.4**. Termination: See **Section 3.4.4**.
Path UNEQ (Path Unequipped)
Path unequipped. Detection: See **Section 3.4.4**. Termination: See **Section 3.4.4**.
Path PLU (Path Payload Label Unstable)
Path payload label unstable. Detection: See **Section 3.4.4**. Termination: See **Section 3.4.4**.
Path TIM (Path Trace Identifier Mismatch)
Path trace identifier mismatch. Detection: See **Section 3.6**. Termination: See **Section 3.6**.
Path TIU (Path Trace Identifier Unstable)
Path trace identifier unstable. Detection: See **Section 3.6**. Termination: See **Section 3.6**.

Table 3-14. Alarms and Failures (4/4)

OCD (Out of Cell Delineation)
Cell non-synchronization. Detection: If a cell in which an error is found as a result of HEC test has been received α times in a row. Termination: If a cell in which no error is found as a result of HEC test has been received δ times + 1 in a row. * α = 6, 7, 8, or 9, δ = 5, 6, 7, or 8. These values can be selected by using the OCDD[1:0] and OCDT[1:0] bits of the MDATMR register. In the default mode, α = 7 and δ = 6.
LCD (Loss of Cell Delineation)
Status in which frame is lost. Detection: If the OCD status lasts for T ms. Termination: If a non-OCD status lasts for T ms. * T = 4 ms or 0 ms. This can be selected by using the LCDDT bit of the MDATMR register. In the default mode, T = 4 ms. When T = 0 ms, the detection/termination condition is the same as that of OCD.
CD (CD Pin State Change)
Indicates that the CD pin input goes low. Detection: If the CD pin input level goes low. Termination: If the input level goes high again. The changes in the input level of the CD pin can be included in the LOS detection condition by setting the CDO bit of the MDSOHR register. CD pin = Low: LOS status High: Normal status (Notice that the pin input level is opposite to the logic of the bit of the register.)

3.4.3 Alarm management

(1) Alarm detection

When the μPD98413 detect the specific alarm, the corresponding alarm is detected automatically and notified by the corresponding register bits. The detection alarm is as follow.

Detection alarm	Detect condition
OOF	When LOS is detected.
LOF	
Line AIS	When LOS or LOF is detected.
Path AIS	When LOS, LOF or Line AIS is detected.
OCD	When LOS, LOF, Line AIS, LOP or Path AIS is detected.
LCD	

(2) Protection of the alarm detection

When the μPD98413 detect the specific alarm, the mPD98413 is protected the alarm detection and not detect corresponding alarm. And if the corresponding alarm is in detecting condition, that alarm is terminated automatically. The protection and termination alarm is as follow.

Termination alarm	Terminate condition
Section TIM	When LOS and OOF is detected.
Section TIU	
Line RDI	When LOS and LOF is detected
PSBF	
LOP	When LOS, LOF or Line AIS is detected.
Path RDI	When LOS, LOF, Line AIS, LOP or Path AIS is detected.
Path PLM	
Path UNEQ	
Path TIM	
Path TIU	

(3) Transmit alarm

When the μPD98413 detect the specific alarm, the μPD98413 automatically transmit corresponding alarm. The transmit alarm is as follow.

Transmit alarm	Transmit condition
Line RDI	When LOS, LOF or Line AIS is detected.
One-bit Path RDI or Enhanced Path RDI Server defect	When LOS, LOF, Line AIS or Path AIS is detected.
Enhanced Path RDI Payload defect	When Path PLM is detected.
Enhanced Path RDI Connectivity defect	When Path UNEQ or Path TIM is detected.
Line REI	When B2 error is detected.
Path REI	When B3 error is detected

(4) Counter stop

When the μPD98413 detect the specific alarm, the corresponding alarm counter is stopped automatically. The stop alarm counter is as follow.

Stop counter	Counter stop condition
B1 error counter	When LOS or OOF is detected.
B2 error counter	When LOS, LOF or Line AIS is detected.
Line REI counter	When LOS, LOF, Line AIS or Line RDI is detected.
B3 error counter	When LOS, LOF, Line AIS, LOP or Path AIS is detected.
Path REI counter	When LOS, LOF, Line AIS, LOP, Path AIS or Path RDI is detected.
Receive valid cell counter	When LOS, LOF, Line AIS, LOP, Path AIS or LCD is detected.
Receive idol cell counter	
Receive HEC error correct cell counter	
Receive HEC error drop cell counter	
Receive valid packet counter	When LOS, LOF, Line AIS, LOP or Path AIS is detected.
Receive abort packet counter	
Receive address error packet counter	

3.4.4 APS (Automatic Protection Switching)

(1) Transmit APS signal

The μPD98413 can transmit APS signal by using K12T register. The mPD98413 always transmit the K1 and K2 byte by setting the K12T register. If occur the transmission Line AIS or Line RDI, those alarm transmission is take precedence the setting K12T register.

(2) Receive APS signal

The μPD98413 has a function for monitoring the K1 and K2 bytes and reporting the arrival of the APS signal when frame synchronization is established. Each time a frame has been received, the APS signal are recorded and compared with the next APS signal. If an APS signal different from that received previously is detected, and if that APS signal is the same in three frames in a row, the APS bit of the DSLER register is set to report the CPU. The APS bit is not set as long as the same APS signals are received. When the CPU detects that the APS bit has been set, it reads the K12R register of the OH drop register to obtain the APS signal. The K12R register is updated only if the same value has been received in three frames in succession. It is not updated if random values are received in three frames in a row, or if frame synchronization is not established.

(3) Protection Switching Byte Failure (PSBF)

The μPD98413 checks the K1 byte to monitor whether a stable K1 byte has been received. If a frame having the same K1 byte is missing three times in a row in 12 continuous frames, the μPD98413 indicates this status as the PSBF. The PSBF status is terminated if a frame having the same K1 byte has been received three times in a row.

If μPD98413 detecting Line AIS, status of PSBF is not change.

(4) 1+1 APS support

The μPD98413 Support 1+1 APS architecture, which can transmit the same cell or packet for working port and protection port, and can switch the receive port from working port to protection port.

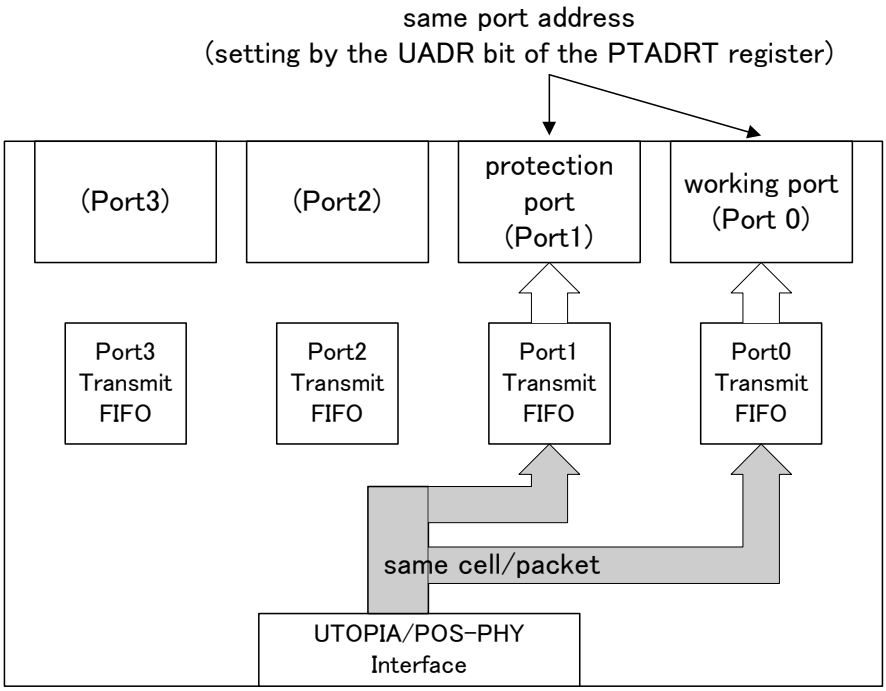
(a) Transmit

The μPD98413 can transmit the same cell or packet for working port and protection port. The method is as follows.

1. Set the same transmit port address to the UADR bit of working Port and protection port of the PTADRT register. (In the POS mode, set the same in-band address to the IADR bit of working port and protection port of the PTADRT register.)

2. Transmit cell/packet for port, which is set by UADR bit the PTADRT register.

Note: Take care of the transmit cell available signal. When transmit cell/packet to the port, the uplink device must be conform the cell available signal of each port that is transmitted the same cell/packet. (In the status polling mode, the result of polling is ORed working port and protection port which is set the same port address.)



(b) Receive

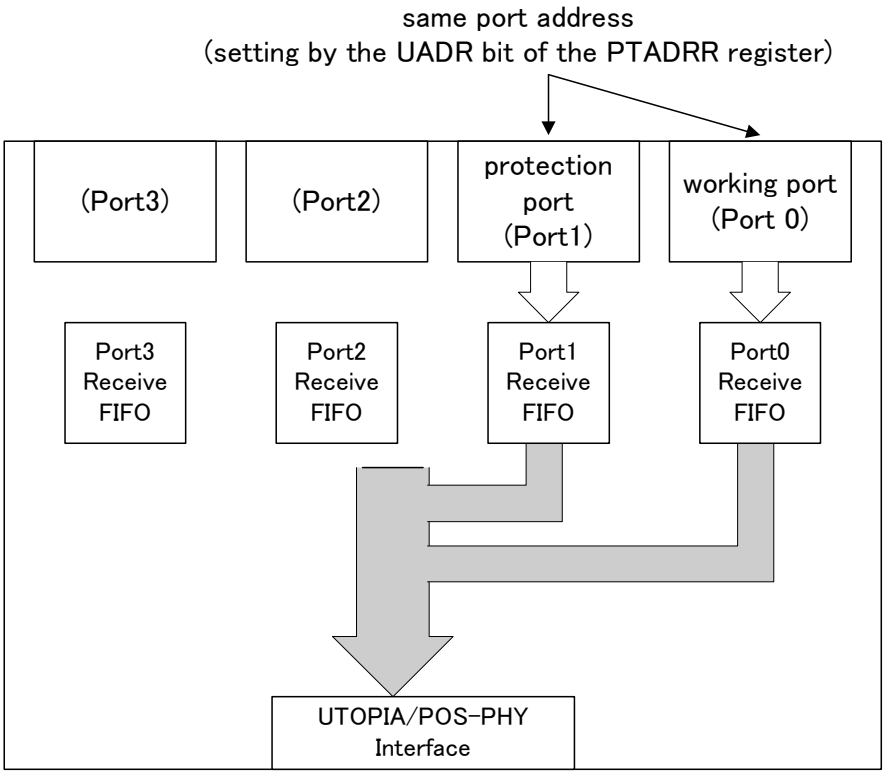
The μPD98413 can switch the receive port from working port to protection port. The method is as follows.

1. Set the same receive port address to the UADR bit of working port and protection port of the PTADRR register. (In the POS mode, set the same in-band address to the IADR bit of Port0 and Port1 of the PTADRR register.)

2. Stop the receive FIFO of the protection port by the PnFCLS bit of the MDAPIR register. And enable the protection port by setting the PnER bit of the PENB register.

3. Disable the working Port by setting the PnER bit of the PENB register.

4. After confirm that the working port FIFO is not busy by the PnBSY bit of the DGE and TGE register, start the receive FIFO of the protection port by the PnFCLS bit of the MDAPIR register.



3.4.5 Monitoring Signal Label Byte

(1) Path Payload Label Unstable (Path PLU)

The μPD98413 checks whether Signal Label, stored in the C2 byte, is received stably. Each time a frame has been received, the value of the C2 byte is checked to see if it is the same as the value of the previous frame. If the value of the C2 byte differs, an internal counter is incremented. When counter has been incremented up to five, the μPD98413 indicates this status as the Path PLU. The internal counter is reset to zero if a frame having the same C2 byte is received three or five times (set to the MDPOHR register) continuously. Then the Path PLU status also is terminated.

For example, if a C2 byte with one byte lost is received while C2 bytes having the expected value have been received in succession, the counter is incremented by one when the lost byte is received and is again incremented by one when the normal byte is next received. As a result, the counter is incremented by two.

The C2R register of the OH drop register stores the value of a C2 byte if the μPD98413 has received the C2 byte of the same value three or five times (set to the MDPOHR register) continuously.

(2) Signal Label Mismatch

The μPD98413 has a function for checking the received C2 byte and detects the Path Unequipped (Path UNEQ) and the Path Payload Label Mismatch (Path PLM).

Path UNEQ

Each time a frame has been received, a value of the C2 byte is compared with 00h. If the C2 byte is 00h, the Path UNEQ is detected. The detection and clearing conditions are as follows.

Detection: If frames with the C2 byte being 00h are received n times continuously

Clearing: If frames with the C2 byte being the value other than 00h are received n times continuously

* n = 3 or 5. This can be selected by using the PPLMM bit of the MDPOHR register. In the default mode, n=5.

When the Path UNEQ is detected, the μPD98413 indicates this error by the interrupt.

If the μPD98413 is detecting LOS, LOF, LOP, L-AIS or P-AIS, the Path UNEQ is not detected.

Path PLM

Each time a frame has been received, a value of the C2 byte is compared with the expected value. If the values do not coincide, the Path PLM is detected.

- The μPD98413 can be set the expected value by the C2EX[7:0] bits of the MDPOHR register (Default value is 13H) , and it can be select to include in the expected value by the PPLM02 bit of the MDPOHR register.
- Note that the value of 01H is includes in the expected value, but it can be except by setting of the PPLM01 bit of the MDPOHR register.

The detection and termination conditions are as follows.

Detection: If frames with the C2 byte Not being the expected value are received five times continuously.

Termination: If frames with the C2 byte being the expected value are received five times continuously.

* n = 3 or 5. This can be selected by using the PPLMDT bit of the MDPOHR register. In the default mode, n=5.

The default value of the C2EX field is 13H.

When the Path PLM is detected, the μPD98413 indicates this error by the interrupt.

If the μPD98413 is detecting LOS, LOF, LOP, L-AIS or P-AIS, the Path PLM is not detected.

The following table is the Signal Label Mismatch detects conditions.

Expected value (C2EX field)	Received C2 byte	Detect	Detect (If not include 01H as expect value)
00h	00h	Path UNEQ	Path UNEQ
00h	01h	None (Matched)	Path PLM
00h	XXh	Path PLM	Path PLM
01h	00h	Path UNEQ, Path PLM	Path UNEQ, Path PLM
01h	01h	None (Matched)	None (Matched)
01h	XXh	Path PLM	Path PLM
XXh	00h	Path UNEQ, Path PLM	Path UNEQ, Path PLM
XXh	01h	None (Matched)	Path PLM
XXh	XXh	None (Matched)	None(Matched)
XXh	Yyh	Path PLM	Path PLM

Note: XXh = anything except 00h or 01h

YYh = anything except 00h or 01h, and not equal XXh.

3.4.6 Monitoring Line Quality (Performance Monitoring)

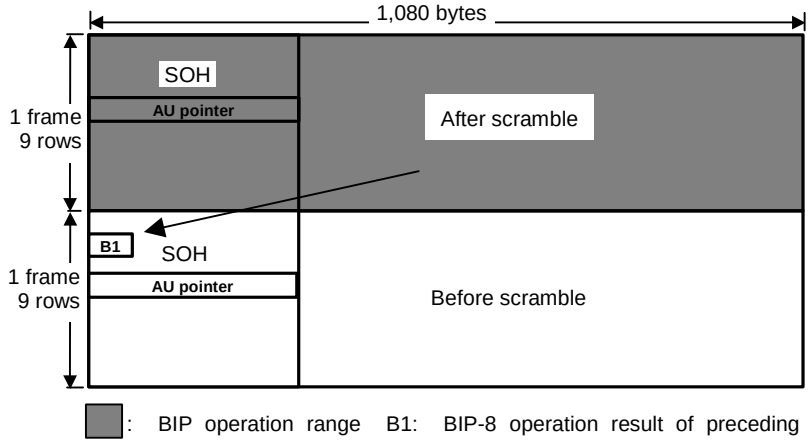
(1) Transmission performance monitoring-related functions

To monitor a sign error to maintain the line quality at the transmission side, a Bit Interleaved Parity (BIP) operation is performed on a specific area and the result is inserted as an OH byte. In addition, the number of Interleaved Bit Blocks in which an error has been detected at the reception side is inserted in the OH byte at the transmission side and transmitted to the upstream side.

(a) Bit Interleaved Parity (BIP)

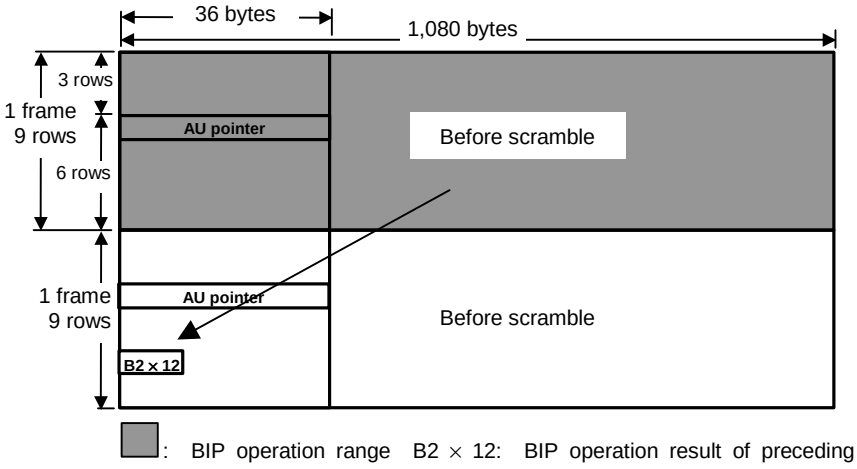
(i) B1 byte (Section BIP-8)

BIP-8 operation is performed on all the bits in frames after frame descramble, and the result of this operation is inserted in the B1 byte before frame scramble of the next frame, then transmitted.



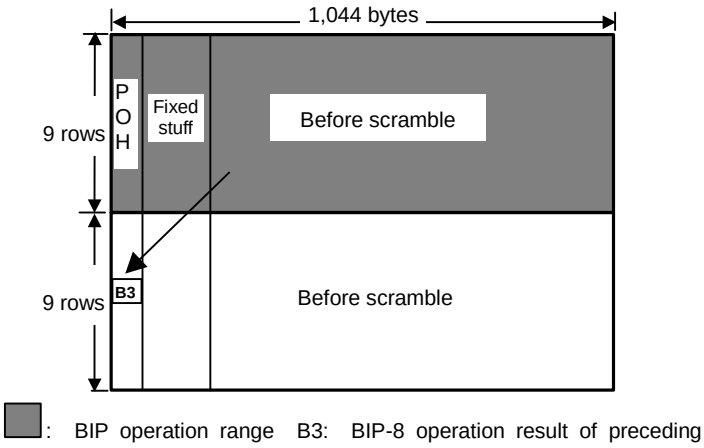
(ii) B2 byte (Line BIP-96)

BIP-96 operation is performed on all the bits of the frames before frame scramble, except the bits on the first through third lines of SOH, and the result of this operation is inserted in the B2 byte before frame scramble of the next frame, and transmitted.



(iii) B3 byte (Path BIP-8)

BIP-8 operation is performed on the STS-12c SPE area before frame scramble, and the result of the operation is inserted in the B3 byte of POH before frame scramble of the next transmit frame, and is transmitted.



(b) Transmitting Line REI (Line Remote Error Indication)

Whether Line BIP-96 error has occurred is reported to a unit in the upstream. If a B2 error is detected in the receive frame, the number of erroneous interleaved bit blocks is automatically stored to the M1 byte.

(c) Transmitting Path REI (Path Remote Error Indication)

Whether Path BIP-8 error occurs is reported to a unit in the upstream. When the μPD98413 detects a B3 error in the receive frame, it automatically stores the erroneous interleaved bit blocks to the G1 byte (bits 1 to 4) of the transmit frame.

(2) Receive performance monitoring function

The events in Table 3-15 are detected when the quality of the reception line is monitored. If an event is detected, the detection is reported to the host by an interrupt signal. The host can identify the type of the event that has occurred by reading the corresponding register. The interrupt can be masked or unmasked for each event.

Table 3-15. Causes of Degradation in Line Quality

B1 error detection
Detects section layer BIP-8 error in receive data. BIP-8 operation is performed on all the frame bits one frame before (data before frame descramble), and the result of the operation is verified with the value of the B1 byte of the current frame.
B2 error detection
Detects line layer BIP-96 error in receive data. BIP-96 operation is performed on all the bits except the first, second, and third lines of SOH one frame before (data after frame descramble), and the result of the operation is verified with the value of the B2 byte of the current frame.
B3 error detection
Path layer BIP-8 of the receive data is checked. BIP-8 operation is performed on the STS-12c SPE area one frame before (data after frame descramble), and the result of the operation is verified against the value of the B3 byte of the current frame.
Line REI detection (Line Remote Error Indication)
Line remote block error information. Line REI is detected when a frame having the M1 byte set to the value of 1 through 96 is received. 0 and 97 through 255 values are no error. μPD98413 also has an optional mode which is ignored the bit 1(MSB) of the M1 byte. This mode is set to the M1M bit of MDLOHR register, and 0 and 97 through 127 values are no error in this mode. The value stored to the M1 byte is the number of interleaved blocks in which an error has been detected as a result of line layer BIP-8 at the transmission destination (downstream).
Path REI detection (Path Remote Error Indication)
Path remote block error information. Path REI is detected when a frame having bits 1 to 4 of the G1 byte set to the value of 1 through 8 is received. 0 and 9 through 15 values are no error. The value stored to this area is the number of interleaved bit blocks in which an error has been detected as a result of path layer BIP-8 operation at the transmission destination (downstream).

(3) Performance monitoring counter

The 32-bit performance monitoring counters that totalize the number of times each event for a cell reception has occurred are provided to each port as shown in Table 3-16. The host can recognize these counts by reading data from the register.

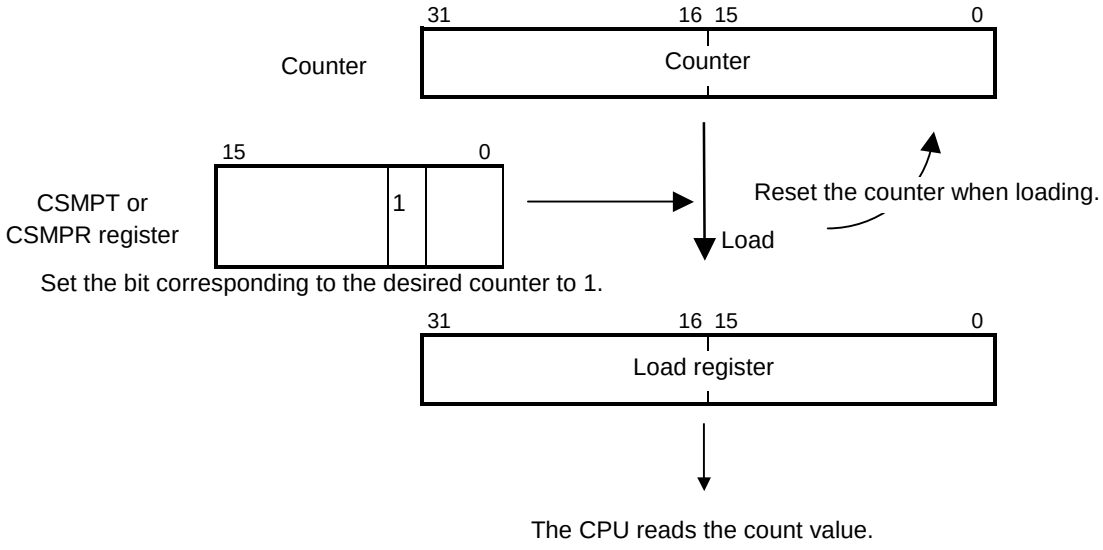
Table 3-16. Performance Monitoring Counters

Counter Type	Counter Name	Count Item
Line monitor counters	B1 error counter	Number of bits or frames detected B1 errors
	B2 error counter	Number of bits or frames detected B2 errors
	B3 error counter	Number of bits or frames detected B3 errors
	Line REI counter	Number of bits or frames detected Line REI errors
	Path REI counter	Number of bits or frames detected Path REI errors
Cell counters	Transmit valid cell counter	Number of cells transmitted from the transmit FIFO to the line.
	Receive valid cell counter	Number of received cells transferred from the receive FIFO to the ATM interface
	Receive idle cell counter	Number of received invalid cells dropped internally
	HEC error drop cell counter	Number of cells discarded due to the HEC verification Note
	HEC correct cell counter	Number of cells modified due to the HEC verification Note
	Receive FIFO full drop cell counter	Number of dropped cells due to receive FIFO overflow
Packet counters	Transmit valid packet counter	Number of packets or bytes transmitted from the transmit FIFO to the line
	Transmit abort packet counter	Number of abort packets transmitted from the transmit FIFO to the line
	Transmit FIFO underflow packet counter	Number of abort packets transmitted due to transmit FIFO underflow
	Receive valid packet counter	Number of received packets or bytes transferred from the receive FIFO to the POS interface
	Receive abort packet counter	Number of received abort packets transferred from the receive FIFO to the POS interface
	Receive address error packet counter	Number of address error packets dropped internally
	Receive FCS error packet counter	Number of FCS error packets transferred from the receive FIFO to the POS interface
	Receive FIFO overflow packet counter	Number of packets which the receive FIFO overflow occurs while a packet is being received
	Receive long packet counter	Number of long packets due to long size packet error
	Receive short packet counter	Number of short packets due to short size packet error

Note: The HEC drop cell counter and HEC Correct counter operate differently depending on the mode setting of HEC error control by the MDATMR registers.

The following figure shows the functions related to the counters and the registers that implement them.

Figure 3-28. Performance Counter Related Register



(a) Monitoring a counter

All the counters are 32 bits wide. After power-on, each counter starts counting the number of events associated with it. A counter unit consists of a counter that actually counts the number of events and a load register in which the counter value is stored temporarily.

1. The CPU sets the bits in the CSMPT and CSMPR register corresponding to the counter whose value is to be obtained to 1.
2. The μPD98413 loads the count value at the time of the counter that has been set to 1 to the load register, and clears the counter to 0. It also clears the bits of the CSMPT and CSMPR register to 0.
3. The CPU reads the count value from the load register. The count value that has been stored to the load register is retained until a new value is loaded by the CAMPR register.
4. If the counter will be overflow, the counter start counting from 0 again, and the corresponding bit of the registers is set to 1 to report the overflow to the CPU.

(4) Bit error rate monitoring

This is a function for monitoring the bit error rates for B2 errors. It reports the signal failure (SF) and signal degrade (SD) when the error rate, which is set in advance, is reached. An interrupt (DSLER, TSLER, SSLER register) or the relevant alarm output pin is used to notify the CPU and peripheral devices of the degradation.

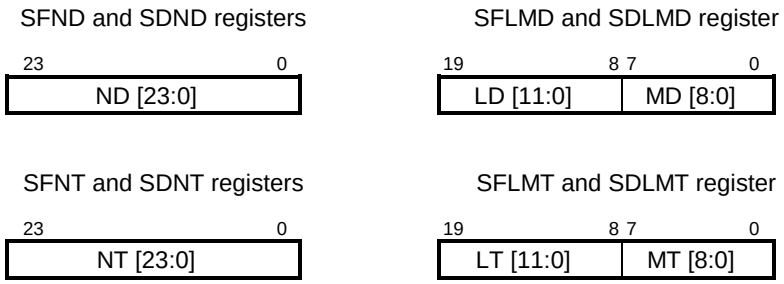
The user can be select the source of the bit error rate monitoring which are B1, B2 and B3 errors. It is set to the MDBER register and the default is B2 error.

Table 3-17. Conditions to Detect Error Rate Degradation Alarms

SF (Signal Failure)
Signal failure alarm. Detection: A specific number of frames are defined as one frame to be monitored, called the ND frame. This alarm is detected when an ND frame (one) in which LD or more bit errors are detected is received MD consecutive times. Termination: A specific number of frames are defined as one frame to be monitored, called the NT frame. This alarm is cleared when an NT frame (one) in which less than LT bit errors are detected is received MT consecutive times.
SD (Signal Degrade)
Signal degrade alarm. Detection: A specific number of frames are defined as one frame to be monitored, called the ND frame. This alarm is detected when an ND frame (one) in which LD or more bit errors are detected is received MD consecutive times. Termination: A specific number of frames are defined as one frame to be monitored, called the NT frame. This alarm is cleared when an NT frame (one) in which less than LT bit errors are detected is received MT consecutive times.

The bit error monitor function starts monitoring in accordance with the default value after power application. To change the parameters, disable the monitor function by using the SFM [1:0] and SDM [1:0] bits of the MDBER register.

Figure 3-29. Registers and Default Values of Bit Error Rate Parameters



Default Values of the Parameters

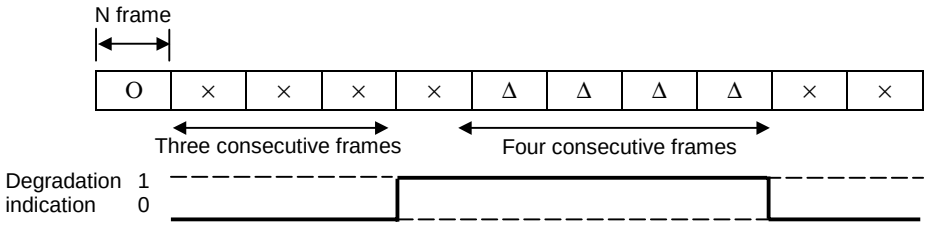
Parameter			SF	SD
ND	NT	Number of frames (24 bits)	000 H	000 H
LD	LT	Number of errors detected (12 bits)	000 H	000 H
MD	MT	Number of consecutive frames (8 bits)	00 H	00 H

(Example) When MD = 3 and MT = 4

O: Less than LD errors are detected in the ND frame.

×: LD or more errors are detected in the ND frame.

Δ: Less than LT errors are detected in the NT frame.



3.5 Overhead Insert/Drop Function

The OH bytes shown in Table 3-18 can set any value to the transmit frame and transmit it by using the insert/drop register, or read the value stored to the receive frame.

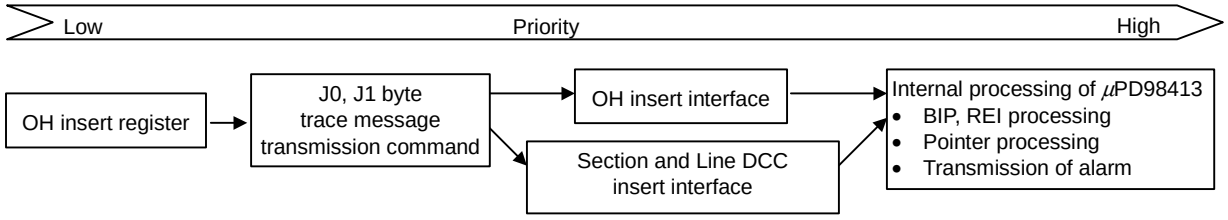
Table 3-18. Insert/Drop Registers

OH Byte		Insert		Drop
		Register	Default	Register
SOH	J0	J0T	01(H)	J0R
	E1	E1F1T	00(H)	E1F1R
	F1	E1F1T	00(H)	E1F1R
	D1	SDCCT	00(H)	SDCCR
	D2	SDCCT	00(H)	SDCCR
	D3	SDCCT	00(H)	SDCCR
LOH	K1	K12T	00(H)	K12R
	K2	K12T	00(H)	K12R
	D4	LDCCT1	00(H)	LDCCR1
	D5	LDCCT1	00(H)	LDCCR1
	D6	LDCCT1	00(H)	LDCCR1
	D7	LDCCT2	00(H)	LDCCR2
	D8	LDCCT2	00(H)	LDCCR2
	D9	LDCCT2	00(H)	LDCCR2
	D10	LDCCT3	00(H)	LDCCR3
	D11	LDCCT3	00(H)	LDCCR3
	D12	LDCCT3	00(H)	LDCCR3
	S1	S1Z2E2T	00(H)	S1Z2E2R
	1st Z2	S1Z2E2T	00(H)	S1Z2E2R
	E2	S1Z2E2T	00(H)	S1Z2E2R
	1st Z2 bit6-7	--	--	Z2FDR
	1st Z2 bit7-8	--	--	Z2FMR
PTR	1st H1 SS bit	MDLOHT	00(b)	--
POH	J1	J1C2T	16(H)	J1R
	C2	J1C2T	00(H)	C2R
	G1	G1F2H4T	00(H)	G1F2H4R
	F2	G1F2H4T	00(H)	G1F2H4R
	H4	G1F2H4T	00(H)	G1F2H4R
	Z3	Z345T	00(H)	Z345R
	Z4	Z345T	00(H)	Z345R
	Z5	Z345T	00(H)	Z345R

3.5.1 Insert Register

A value set to the insert register is stored to a specific position in the transmit OH byte and transmitted. Unless the value of the register is changed, the default value of the insert register is stored and transmitted.

The OH insert register function is lower priority than the transmission of the J0 and J1 trace message, the OH insert interface, the Section and Line DCC insert interface and the internal processing of the μPD98413. If such processing works, the value set to the insert register is overwritten.



3.5.2 Drop Register

The drop registers store the contents of the OH byte of the receive frame. The CPU can obtain the received contents by reading these registers. The contents of the drop registers, except the K12R, C2R, Z2FDR and Z2FMR registers, are updated each time a frame is received. The K12R, C2R, Z2FDR and Z2FMR registers are updated in the following conditions.

K12R

This register is updated if the values of the K1 and K2 are the same in three frames received continuously after the different value from that received previously is detected. When this register is updated, the μPD98413 indicates it to the APS bit of the DSLER register and interrupt.

C2R

This register is updated if the same value is received in three or five, which is set to the MDPOHR register, frames continuously.

Z2FDR

This register is updated if the values of the bit6-7 of 1st Z2 are the same in six frames received continuously after the different value from that received previously is detected. When this register is updated, the μPD98413 indicates it to the Z2D bit of the DSLER register and interrupt.

Z2FMR

This register is updated if the values of the bit7-8 of 1st Z2 are the same in 12 frames received continuously after the different value from that received previously is detected. When this register is updated, the μPD98413 indicates it to the Z2M bit of the DSLER register and interrupt.

3.6 Transmission/Reception of J0/J1 Trace Message

The J0 byte of SOH and J1 byte of POH are used to transfer 16-byte or 64-byte trace messages. µPD98413 has a function for transmitting or receiving these trace messages.

J0: Section trace message
J1: Path trace message

3.6.1 Transmitting Trace Message

The µPD98413 has a message buffers for each of J0 and J1 to set trace messages. A new message is set to Expected buffer; a trace message is transmitted from buffer.

Table 3-19 Register and bits related trace message transmit

Classification	Register and Bit of Section trace message		R/W	Outline
	Section (J0)	Path (J1)		
Mode	MDSOHT register J0SZ bit	MDPOHT register J1SZ bit	R/W	Selection of 16- or 64-byte length
Buffer select TMBT register	BSEL bit	BSEL bit	R/W	Selection of J0 buffer or J1 buffer
	BADR bits	BADR bits	R/W	Set the offset address of the trace message buffer
Buffer Access register TMDT register	BDAT bit	BDAT bit	R/W	Access to Accepted buffer,
Transmit command CMTMT register	J0STAT bit	J1STAT bit	R/W	Start to transmit new trace massage.

(1) Transition of trace message

1. Specify whether a trace message is 16 or 64 bytes long by using the J0SZ bit of the MDSOHT register (Section trace message), and using the J1SZ bit of the MDPOHT register (Path trace message). In the default mode, both the J0 message size and the J1 message size are 64 bytes.

2. Set a message to a buffer memory. As an example, buffer of J0 is used to transmit a trace message. First, select the section message buffer by the BSEL bit of the TMBT register. Next, write 00H to offset register (BADR bits of the TMBT register). Next, write data, one word (32 bits) at a time, to the access register (TMDT). The write pointer of J0 buffer is automatically incremented by one word each time data is written to it. Therefore, set the pointer value to (00H) in the first instance only. Subsequently, 64-byte or 16-byte data can be set simply by repeatedly writing to the access register.

Note: If TMDT register is accessed by 16-bit access, the lower word (16-bit) is not use. See Figure 3-31.

3. Upon the completion of writing to the highest address of the pointer, incremented each time a write access occurs, the pointer is automatically returned to 0. The highest address varies with the setting of the message length.

4. The pointer register (BADR bit of the TMBT register) indicates the pointer value for the word to be written next. By directly specifying the pointer to be set next in the pointer register, a message can be partly updated.

5. Enable the receive line interface by setting the PENB register, and enable to the section trace message by setting the CMTMT register.

6. If the transmission command is enabled (by setting the J0STAT bit of the CMTMT register to 1) after data has been set, the μPD98413 inserts a trace message to the position of the J0 byte in a transmit frame, one byte at a time, starting from the high-order eight bits of the first word of J0 buffer.

7. If transmit next new trace message, overwrite setting buffer and then enable the transmission command.

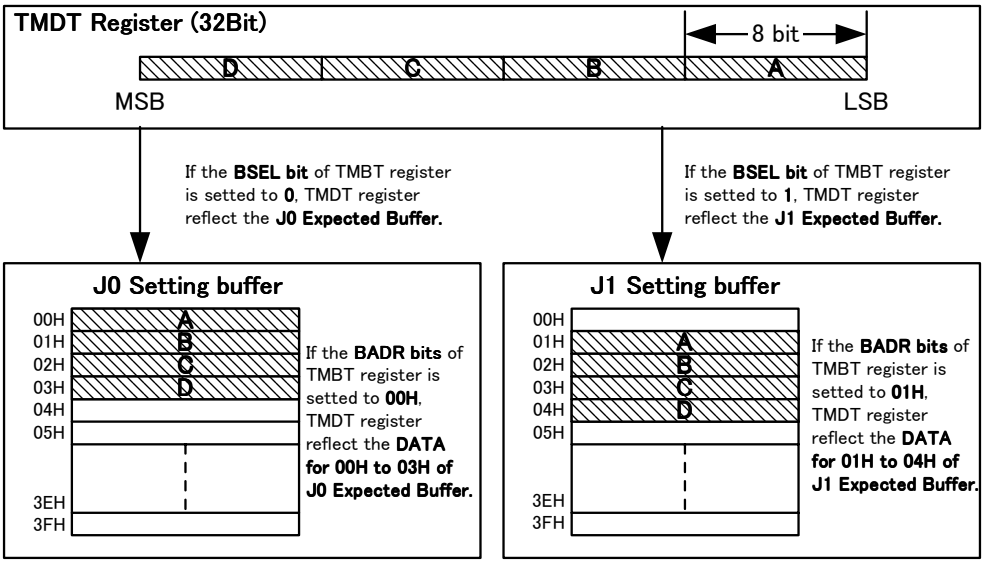
Note: after enable the transmission command, the transmission command register is not return to 0. Therefore, if transmit next trace message, write 0 to the register, and then write 1 to the register.

(2) Transmit trace message Buffer access Method

(a) 32 bit access

32 bit access method is as follows.

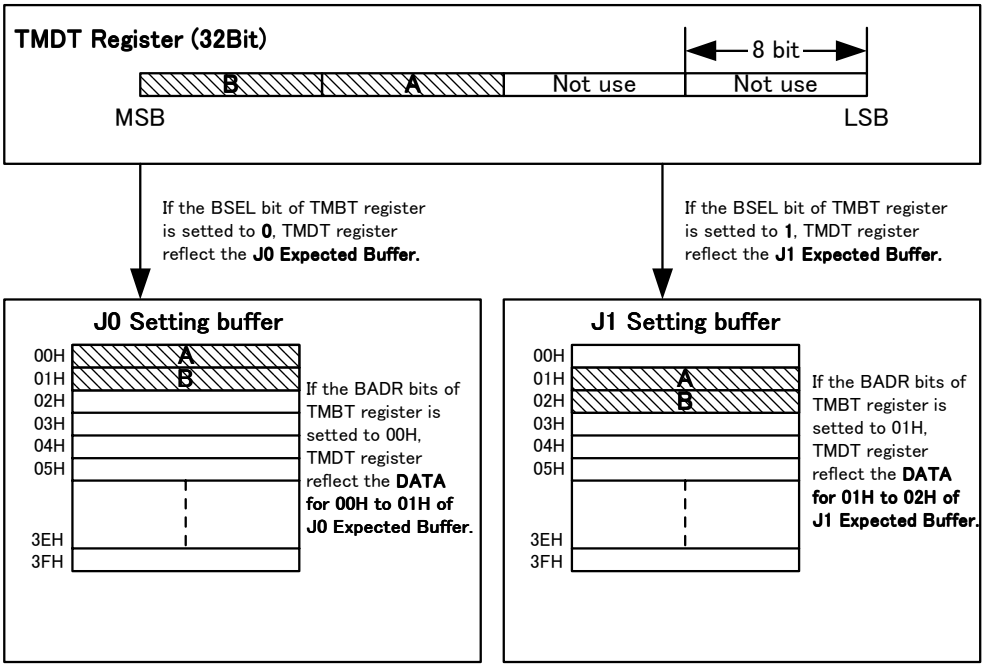
Figure 3-30 The method of Access to transmit trace message buffer



(b) 16 bit access

16 bit access method is as follows.

Figure 3-31 The way to Access to transmit trace message buffer



3.6.2 Receiving Trace Message

The μPD98413 has two 64-byte buffers (Accepted and Captured buffer) for each of J0 and J1 that store received trace messages. Accepted buffer is able to access by the Management Interface, but Captured buffer is not. When μPD98413 is received a new message, it is stored in Captured buffer, and then if Accepted buffer is not locked, the received message is stored in Accepted buffer. Accepted buffer is able to lock, because if a message that is stored in the Accepted buffer is not finished to read by the CPU, the read massage value is differ from received message value. While the message stored to Accepted buffer, a new message is stored to the Captured buffer. The μPD98413 also has one 64-byte buffer storing expected trace message for each of J0 and J1.

Table 3-20 Register and bits related trace message receive

Classification	Register and Bit of Section trace message		R/W	Outline
	Section (J0)	Path (J1)		
Mode	MDSOHR register J0SZ bit	MDPOHR register J1SZ bit	R/W	Selection of 16- or 64-byte length
	MDSOHR register J0SYNC bit	MDPOHR register J1SYNC bit	R/W	Specifies whether set synchronization pattern is at the beginning or end of message
Buffer select TMBR register	BSEL bit	BSEL bit	R/W	Selection of J0 buffer or J1 buffer
	BTYP bit	BTYP bit	R/W	Selection of Accepted buffer or Expected buffer
	BADR bit	BADR bit	R/W	Set the offset address of the trace message buffer
Buffer lock CMTMR register	J0LOCK bit	J1LOCK bit	R/W	Indicated and sets to lock the Accepted buffer of the trace message.
Buffer Access register TMDR register	BDAT bit	BDAT bit	R/W	Access to Expected Buffer or Accepted buffer, Which to Access is setting by buffer select register (TMBT).
TIM detecting pattern setting J0PTN J1PTN register	J0PTN bit	J1PTN bit	R/W	Set the synchronous pattern of J0/J1 massage
	J0M bit	J1M bit	R/W	Set the mask value of the synchronous pattern.

(1) Reception of trace message

1. Specify whether the trace message is 16 or 64 bytes by using the J0SZ bit of the MDSOHR register (Section trace message). In the default mode, both the J0 message size is 64 bytes.

2. Set a 2-byte synchronization pattern that indicates the beginning or end of the message to the J0PTN[15:0] bits and J0M[15:0] bits of the J0PTN registers(Section trace message). Set a pattern to be detected to the J0PTN[15:0] bits, and specify the bits of the bit string of the J0M[15:0] bits that are treated as Don't Care bits, to the J0PTN[15:0] bits.

3. Specify whether the set synchronization pattern is the beginning or end of the message to the J0SYNC bit of the MDSOHR register. By default, the pattern is assumed to be an end pattern.

For example, to have one byte with the MSB set to 1 (1xxxb) be recognized as the end pattern of the message, the setting is as follows, and the J0SYNC bit of MDSOHR register is set to 0.

J0PTN	1000 0000 0000 0000
J0M	0111 1111 1111 1111
Pattern to be detect	1xxx xxxx xxxx xxxx

J0SYNC bit	Detected Pattern Position
0	Specifies end of the message
1	Specifies head of the message

4. The μPD98413 stores the data at the J0 byte position of the receive frame, in order, into Captured buffer, checking the contents of the data string each time it is updated. When the data string stored in Captured buffer satisfies the three conditions listed below, the data is stored in the Expected Buffer, and the JLOCK bit of the CMTMR register is set to 0 and, at the same time, the J0M bit of the DPPER register is set to post notification of the arrival of a new message to the CPU. The setting of the J0M bit can be used to trigger an interrupt. If the J0LOCK bit of the CMTMR register status is 1, the trace message that is stored to Expected buffer is kept and not overwrite, and then if μPD98413 detect new message, that is aborted internally.

Detecting Trace message condition is as follows.
Condition 1. The synchronization pattern is contained in receive message.
Condition 2. The same message is received three or more time in a row.
Condition 3. The received message is different from message that is contained Captured buffer.

5. When the CPU has been informed of reception of a new message, to receive the next message, it sets to 0 the J0LOCK bit of the CMTMR register (if the data of Expected buffer has already been read by the CPU and can be overwritten by the new message).

6. The data of the message stored in the Accepted buffer has been automatically rearranged by the μPD98413. If a synchronization pattern is specified at the beginning of a message, the data has been rearranged so that the synchronization pattern is at the beginning of the buffer (pointer = 00H). If the synchronization pattern is specified as the end byte of the message, the data is rearranged so that the synchronization pattern is at the end of the message.

7. The CPU read-accesses the access register (TMDR) of Accepted buffer to read the message it contains.

Note: If TMDR register is accessed by 16-bit access, the lower word (16-bit) is not use. See Figure 3-33.

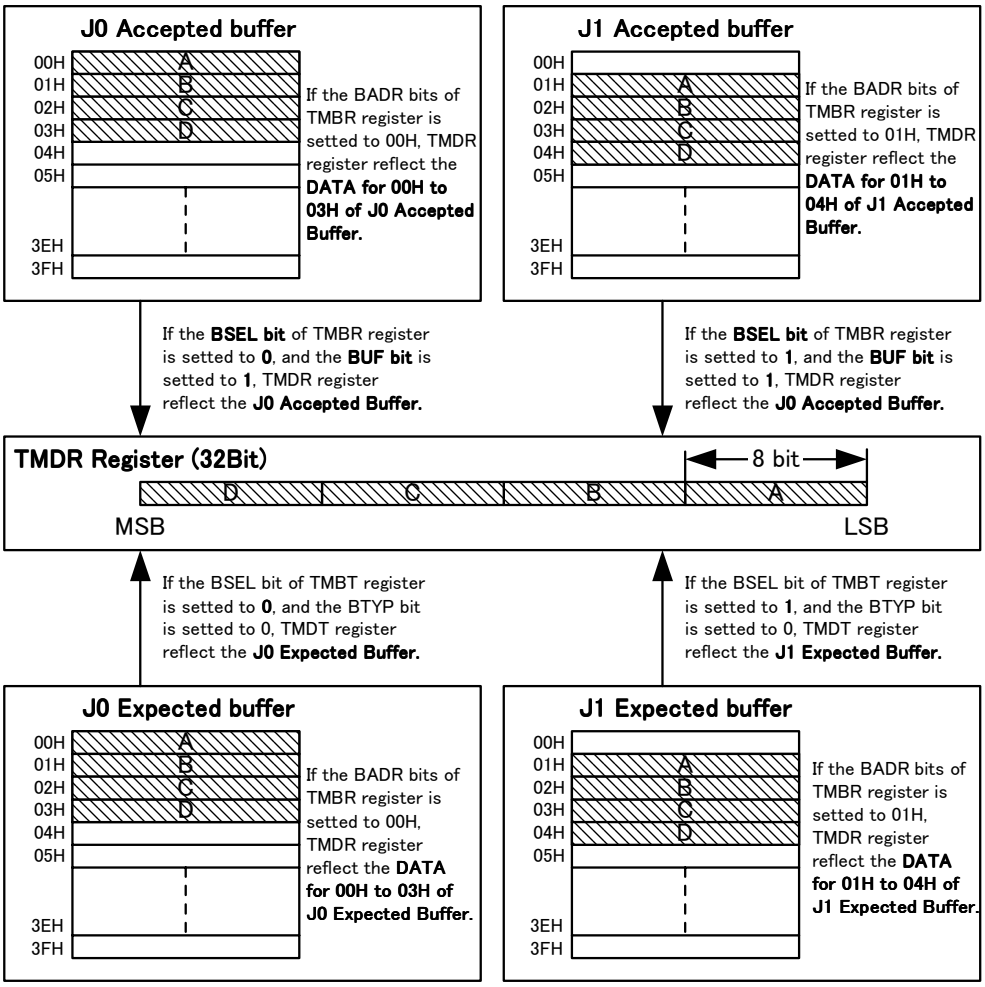
8. Each time the CPU has accessed the access register, the μPD98413 automatically increments the pointer of the buffer. Upon the completion of reading from the highest address of the pointer, incremented each time a read is performed, the pointer is automatically returned to 0.

(2) Receive trace message Buffer access Method

(a) 32 bit access

32 bit access method is as follows.

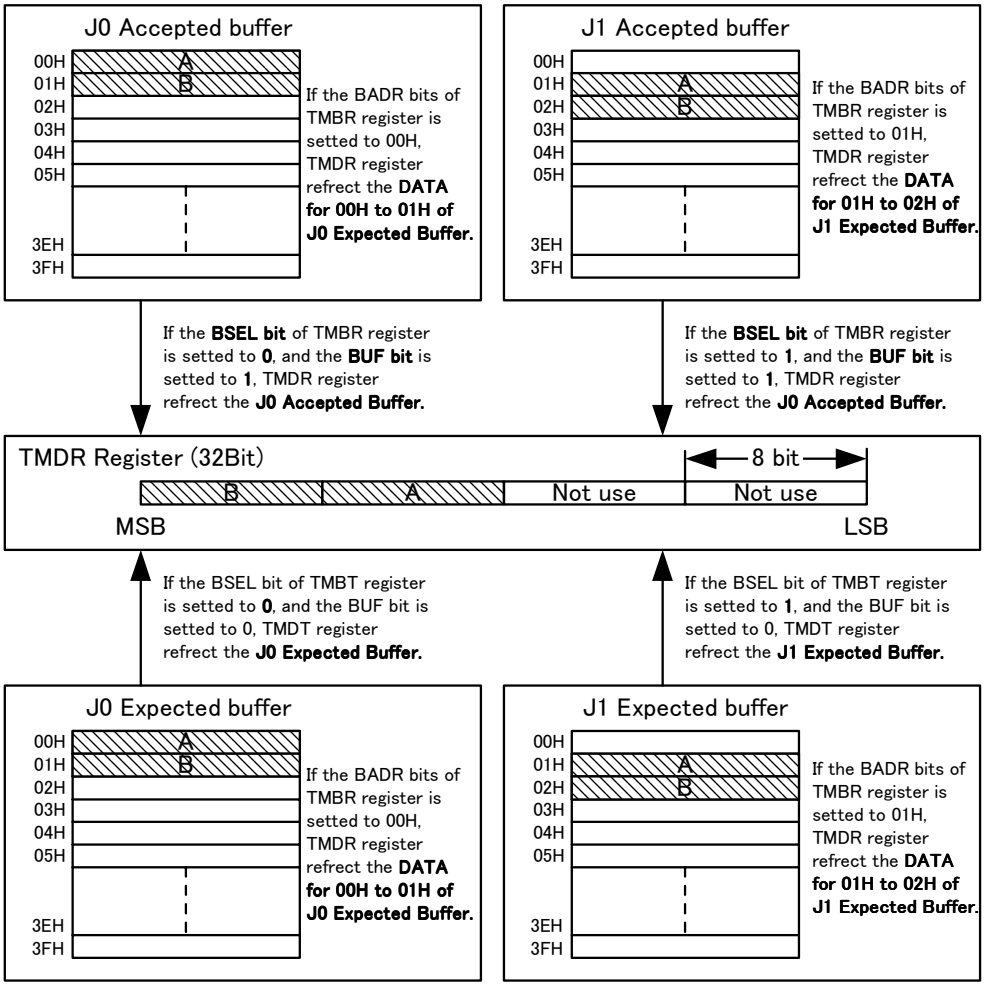
Figure 3-32 Access to receive trace message buffer



(b) 16 bit access

16 bit access method is as follows.

Figure 3-33 Access to receive trace message buffer



(2) Monitoring receive trace message

(a) Detecting J0 Section Trace Identifier Unstable (Section TIU)

Whether the 16- or 64-byte section trace message stored in the J0 byte is received stably is checked. If the receive message differs from the previous message, the internal counter is incremented (+1). When the value of the counter reaches eight or five (set to the STIUD bit of the MDSOHR register), the status is indicated as Section TIU. This status is cleared if three or five (set to the STIUT bit of the MDSOHR register) messages of the same contents have been received in succession. At the same time, the internal counter is also reset.

(b) Detecting J0 Section Trace Identifier Mismatch (Section TIM)

Whether the 16- or 64-byte section trace message stored in the J0 byte is the expected message is checked. If the message stored to the J0 message buffer differs from the expected message (set the expected massage to Expected buffer), the μPD98413 detects the Path TIM. The detection and termination conditions are as follows.

Detection: If the mPD98413 received same J0 massage three or five times (set to the STIMDT bit of the MDSOHR register) continuously, and that message is differ from expected massage..

Termination: If the mPD98413 received same J0 massage three or five times (set to the STIMDT bit of the MDSOHR register) continuously, and that message equal to expected massage.

When the μPD98413 detects the Section TIM, the status is indicated as the Section TIM in the DSLER register.

(c) Detecting J1 Path Trace Identifier Unstable (Path TIU)

Whether the 16- or 64-byte section trace message stored in the J1 byte is received stably is checked. If the message stored to the J1 message buffer differs from the previous message, the internal counter is incremented (+1). When the value of the counter reaches five or eight (set to the PTIUD bit of the MDPOHR register), the status is indicated as Path TIU. This status is cleared if three or five (set to the PTIUT bit of the MDPOHR register) messages having the same contents are received in succession. At the same time, the internal counter is also reset.

(d) Detecting J1 Path Trace Identifier Mismatch (Path TIM)

Whether the 16- or 64-byte section trace message stored in the J1 byte is the expected message is checked. If the message stored to the J1 message buffer differs from the expected message, the μPD98413 detects the Path TIM. The detection and termination conditions are as follows.

Detection: If the mPD98413 received same J1 massage three or five times (set to the PTIMDT bit of the MDPOHR register) continuously, and that message is differ from expected massage..

Termination: If the mPD98413 received same J1 massage three or five times (set to the PTIMDT bit of the MDPOHR register) continuously, and that message equal to expected massage.

When the μPD98413 detects the Path TIM, the status is indicated as J1 Path TIM in the DPPER register.

3.7 Transmitting Pseudo Frame for Testing

The μPD98413 can internally generate and transmit a pseudo frame that causes the errors listed in Table 3-21 in the opposing device. This function is useful for testing the system, and can be executed by using the pseudo error register.

Table 3-21. Pseudo Error Frame

Target Error	Pseudo Frame Name	Register for transmit Pseudo frame	Description of Transmit Frame
LOS	PLOS frame	PESOH register	Fixes transmit data to 00H.
OOF/LOF	POOF frame	PESOH register	Fixes A1 and A2 bytes to 00H.
LOP	PLOP frame	PEPTR register	Fixes H1, H2, and H3 bytes to FF, FE, and FFH.
OCD, LCD	POCD frame	PEATM register	Maps cell with LSB in HEC field inverted.
B1 error	PB1 frame	PESOH register	Inverts any bits of B1 byte. Inverted bits are set in the PESOH register. μPD98413 inverts the corresponding bits of B1 byte by the PB1[7:0] bits of the PESOH register. If set to “01H” in the PB1[7:0] field, the LSB bit of the B1 byte is inverted.
B2 error	PB2 frame	PELOH register	Inverts any bits of 12^{th} B2 byte. Inverted bits are set in the PELOH register. μPD98413 inverts the corresponding bits of 1^{st} B2 throw 12th B2 byte by the PB2[7:0] bits of the PELOH register. If set to “01H” in the PB2[7:0] field, the LSB bit of the B2 byte is inverted.
B3 error	PB3 frame	PEPOH register	Inverts any bits of B3 byte. Inverted bits are set in the PEPOH register. μPD98413 inverts the corresponding bits of B3 byte by PB3[7:0] bits of the PEPOH register, If set to “01H” in the PB3[7:0] field, the LSB bit of the B3 byte is inverted.
Line REI	PLREI frame	PELOH register	Sets M1 byte to the value set in the PM1[7:0] bits of the PELOH register for transmission.
Path REI	PPREI frame	PEPOH register	Sets bits 1 to 4 of G1 byte to the value set in the PG1[3:0] bits of the PEPOH register for transmission.

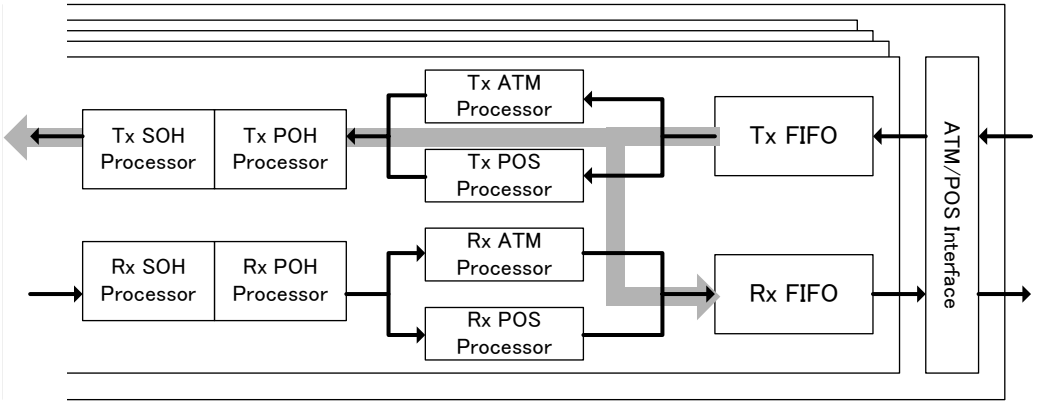
3.8 Loopback Function

The two types of loopback modes are supported. These modes can be selected by using the MDPGEN register.

(1) Equipment Loopback

The data input to the transmission side of the ATM/POS interface is looped back at the μPD98413 internal, and is output from the reception side of the ATM/POS interface. When loopback is set, the loop data is not output to the transmission line side. Instead, a frame that is mapped Line AIS frame is transmitted. If the ELPOM bit of the MDPGEN register is set, the loop data can also be sent to the transmission line.

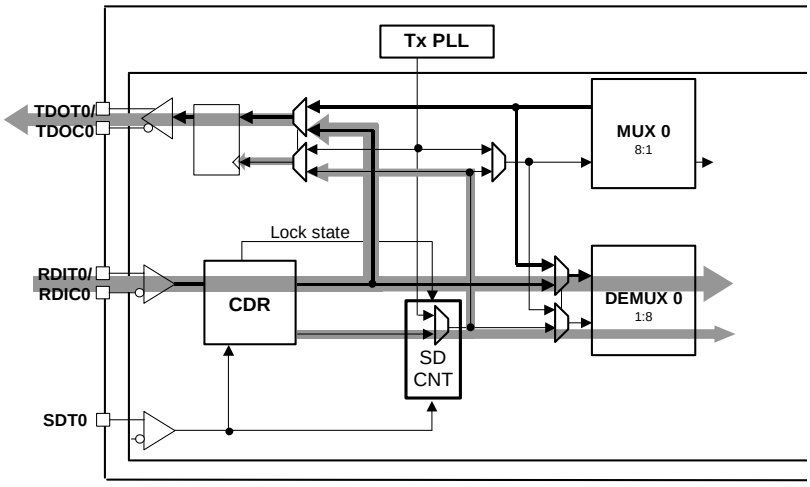
Figure 3-34. Equipment Loopback



(2) Line Loopback

In this mode, the data input from the reception side of the line interface is returned at the μPD98413 internal and output from the transmission side of the line interface.

Figure 3-35. Line Loopback



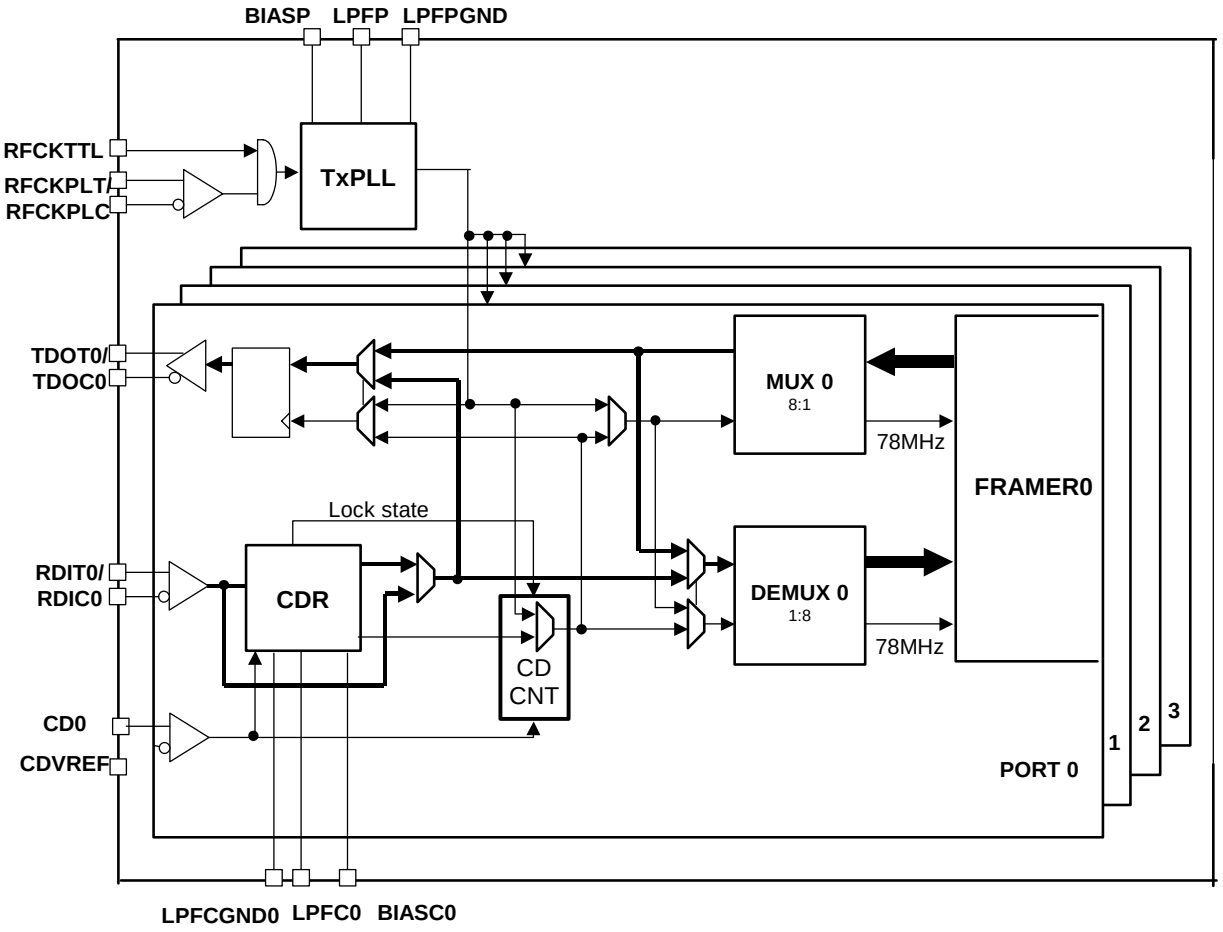
CHAPTER 4 INTERFACES

4.1 Line Interface

The line interface is used to connect an optical transceiver or receiver on the line side.

The following figure is an outline block diagram of the line interface of the μPD98413. The transmit/receive clock paths can be changed by setting pins and registers. This block consists of parallel-to-serial (MUX), serial-to-parallel (DEMUX), TxPLL, and clock and data recovery unit (CDR).

Figure 4-1. Overview of μPD98413 line interface block



(1) Synthesizer PLL

The internal synthesizer PLL generates the 622.08-MHz clock based on the 77.76MHz clock. All the ports use this clock as there transmit clock. The internal synthesizer PLL starts creating a clock as soon as power is applied. However, about **T.B.D** ms must elapse before appropriate 622.08MHz clock is supplied to each port.

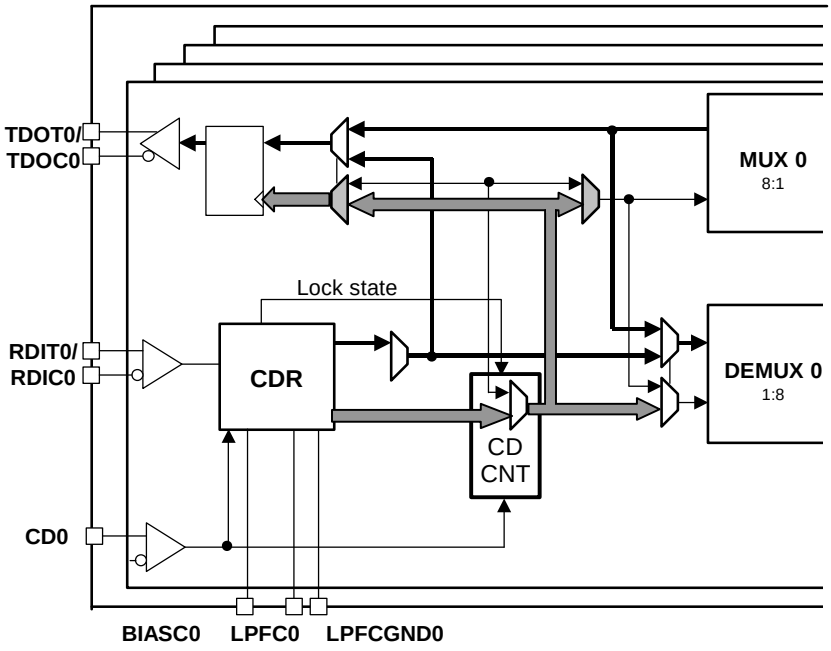
(2) Reference Clocks

µPD98413 provides two types reference clock input, a differential PECL reference clock input and a LVTTL reference clock input. Both reference clock are internally ANDed to generate the reference for TxPLL and CDR. If the LVTTL reference clock is used, the positive side of the differential PECL (RFCKPLT) must be connected to a logic one and the negative side (RFCKPLC) to a logic zero. If a differential PECL reference clock is used, LVTTL reference clock input (RFCKTTL) must be tied high.

(3) Loop timing mode

When the LPTIM bit of the MDPGEN register are set to 1, the corresponding port uses the clock extracted by the CDR from the receive data as the transmit clock. This setting is made for each port and does not affect the transmit clock setting of the other ports.

Figure 4-2. Loop timing mode



(4) Clock Data Recovery

The receive clock is extracted by the clock recovery unit (CDR) from the receive data string input by each port to RDIT/RDIC. After power is applied, the CDR of each port starts following up with the reference clock. When the frequency of the recovered clock is within 500 ppm of the reference clock, the CDR switch the following up to the receive data. If the correct receive data is input, a synchronization clock can be obtained about **T.B.D.** ms after reset.

(5) Lock Detect

Each port CDR has unlock detection circuit that monitors whether the CDR follows up with a receive data string and that the expected clock is extracted. This circuit monitors the frequency difference between the clock extracted by the CDR and the reference clock. If the difference between the two clock frequencies exceeds **500 ppm**, the lock detection circuit judges that the CDR is in out of locked state (OOL status). This status is reflected on the bits of the status register and can be used as an interrupt cause. If CDR enters the OOL status, to prevent the receiver circuit from operating with an unstable clock, the clock that provided to the receiver circuit (after DEMUX) be automatically changed to the TxPLL.

If the difference is within **500 ppm**, the OOL status is cleared. When the OOL status is cleared, the recovery clock is used as the receive clock again.

(6) CD (Carrier Detect)

Each port has Carrier Detect (CD) pin. When CD is low, μPD98413 assumes that the port is in loss of signal status and the serial data on RDIT/RDIC will be internally forced to constant zero. And the clock that provided to the receiver circuit be forcibly switched to the TxPLL. When a port is in loop-timing mode, it is use the clock extracted by the CDR from the receive data as the transmit clock. In that case, if CDR enter OOL status, the transmit clock is forcibly switched to the clock generated by TxPLL. The low level of CD signal can be used as a condition for LOS detection.

(7) Connection example

TBD

4.2 ATM Interface

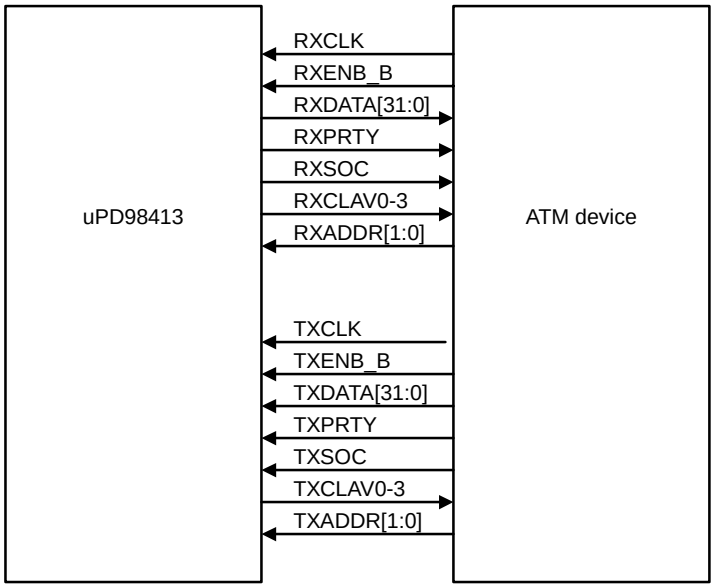
The ATM interface transfers transmit and receive cell data to the ATM device. The features of this interface are as follows:

- Compliant with ATM Forum “UTOPIA 3 Physical Layer Interface (af-phy-0136.00)”.
- 32-bit, 104 MHz LVTTL FIFO interface.
- Supports 52-byte and 56-byte cell format.
- Supports direct status indication and status poling.
- Executes a parity check on transmit data, generates and outputs a parity bit of receive data.
- Detects transmit/receive FIFO overflows.
- Selectable FIFO threshold condition for TXCLAV signal indicating an available area of transmit FIFO for each port.
- 1K bytes transmit and receive FIFOs for each port.
- Supports an optional TAG field with transmit and receive cells.

4.2.1 Signals

An example of connecting the ATM interface is shown below.

Figure 4-3. Example of Connecting the ATM Interface



(1) Transmit interface

The transmit interface uses the signals defined below.

TXCLK (input): Transmit clock.
TXCLK is used to clock the transmit control signals and data. TXCLK cycles at a rate up to 104MHz.

TXDATA[31:0] (input): Transmit data.
TXDATA[31:0] is 32-bit data bus for the transmit data, from the ATM device to the µPD98413. TXDATA31 is the MSB, TXDATA0 is the LSB.

TXSOC (input): Transmit start of cell.
TXSOC is an active high signal asserted by the ATM device to indicate the start of cell position. TXSOC is only asserted during the first clock cycle of the data transfer.

TXENB_B (input): Transmit enable.
TXENB_B is an active low signal and the assertion is coincident with the start of the cell transfer. TXENB_B is used for address selection during the last clock cycle before it is asserted.

TXPRTY (input): Transmit data path parity.
TXPRTY is served as the odd or even parity over TXDATA[31:0].

TXCLAV0-3 (output): Transmit cell buffer available.
TXCLAV is used to indicate that space for at least one cell is available in the µPD98413 transmit FIFO. TXCLAV0 is used in the status-polling mode. TXCLAV0-3 are used in the direct status indication mode. Then TXCLAV0 corresponds to the port0, TXCLAV3 corresponds to the port3.

TXADDR[1:0] (input): Transmit address.
TXADDR[1:0] is used to select the port for which the transmit data is to be destined. The address is used in both the direct status indication mode and the status-polling mode. The following addresses show the corresponding ports.
0: port0, 1: port1, 2: port2, 3: port3

(2) Receive interface

The receive interface uses the signals defined below.

RXCLK (input): Receive clock.
RXCLK is used to clock the receive control signals and data. RXCLK cycles at a rate up to 104MHz.

RXDATA[31:0] (output): Receive data.
RXDATA[31:0] is 32-bit data bus for the receive data, from the μPD98413 to the ATM device. RXDATA31 is the MSB, RXDATA0 is the LSB.

RXSOC (output): Receive start of cell.
RXSOC is an active high signal asserted by the μPD98413 to indicate the start of cell position. RXSOC is only asserted during the first clock cycle of the data transfer.

RXENB_B (input): Receive enable.
RXENB_B is an active low signal asserted by the ATM device to initiate a cell transfer. RXENB_B is used for address selection during the last clock cycle before it is asserted.

RXPRTY (output): Receive data path parity.
RXPRTY serves as the odd or even parity over RXDATA.

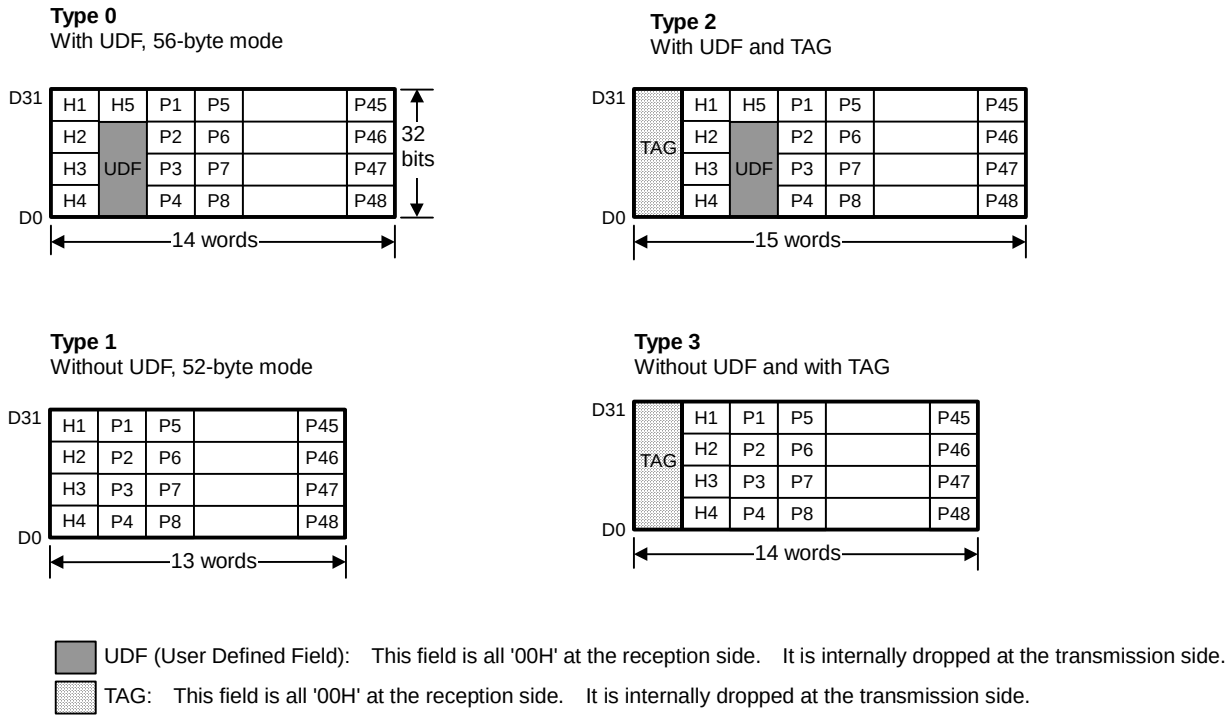
RXCLAV0-3 (input): Receive cell available.
RXCLAV is used to indicate that at least one cell is available in the μPD98413 receive FIFO. RXCLAV0 is used in the status-polling mode. RXCLAV0-3 are used in the direct status indication mode. Then RXCLAV0 corresponds to the port0, RXCLAV3 corresponds to the port3.

RXADDR[1:0] (input): Receive address.
RXADDR is used to select the port from which the receive data is to be read. The address is used in both the direct status indication mode and the status polling mode. The following addresses show the corresponding ports.
0: port0, 1: port1, 2: port2, 3: port3

4.2.2 Cell Formats

The format of the cell transferred via the ATM interface can be selected from the four types shown in the following figure.

Figure 4-4. Cell Formats



(1) UDF

The μPD98413 supports a 52-byte cell format that does not include the H5 byte that is the HEC field of a cell overhead, and a 56-byte format that includes. If H5 is included, dummy data 'UDF' is also inserted. In this manual, the 56-byte cell format is referred to as "mode with UDF" and the 52-byte format as "mode without UDF." The UDF mode is set to the MDAPIT and MDAPIR registers.

Table 4-1. Mode of UDF

	Mode with UDF	Mode without UDF (Default)
Transmission	Cell is input as 56-byte (14-word) data. The internally calculated HEC value is overwritten to the H5 byte, and UDF is internally dropped.	Cell is input as 52-byte (13-word) data. The μPD98413 inserts an HEC value between H4 and P1.
Reception	Received HEC value and UDF (all '00H') are combined and inserted into the second word position of a cell and the cell is output as 56-byte (14-word) data.	Received HEC is dropped within the μPD98413 and a cell is output as 52-byte (13-word) data.

(2) TAG

The μPD98413 supports modes in which a one-word space is inserted in the first word of a cell as a function to assist the ATM device to append TAG (label) to each cell. In this manual, these modes are referred to as modes with and without TAG. The TAG mode is set to the MDAPIT and MDAPIR registers.

Table 4-2. Mode of TAG

	Mode without TAG (Default)	Mode with TAG
Transmission	The word indicated by the high level of TXSOC is input as the first word of a cell.	The word in the cycle next to that in which a word indicated by the high level of TXSOC is input as the first word of a cell. The μPD98413 ignores the first word (TAG).
Reception	RXSOC is driven high when the first word of a cell is output.	One word of TAG space is inserted before the first word of a cell, and RXSOC is driven high when the TAG space is output.

The user can set any TAG value added to the receive cell in the IADRR register. The μPD98413 sends the receive cell to ATM interface with the TAG value set to the IADRR register.

4.2.3 Transmit operation

The μPD98413 supports both the direct status indication mode and the status polling mode (Multi-PHY operation with 1 TXCLAV).

(1) Direct status indication

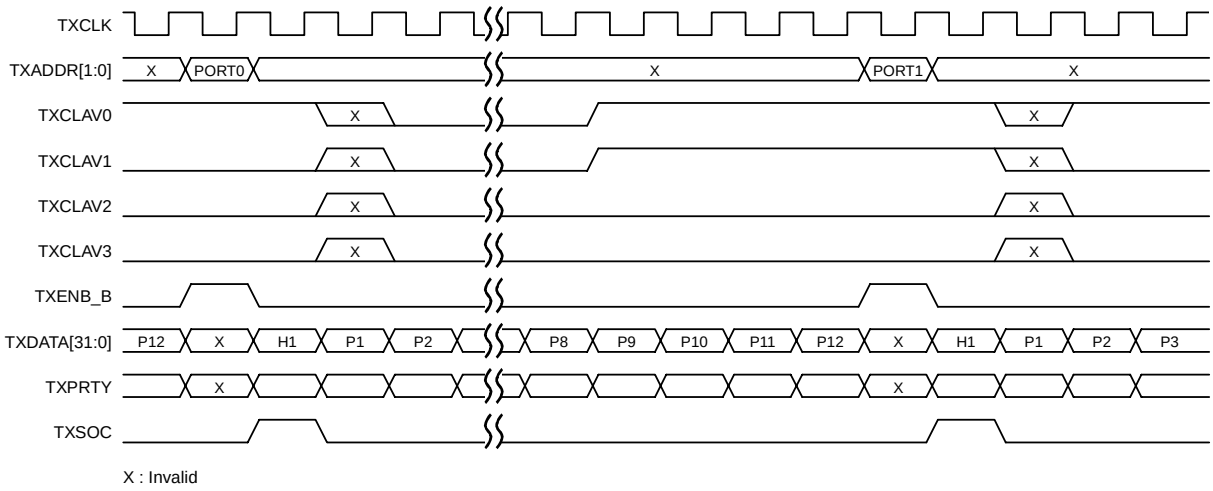
The μPD98413 implements a dedicated TXCLAV signal for each of the ports. TXCLAV0 corresponds to the port0, while TXCLAV3 corresponds to the port3.

The ATM device can send a cell to the μPD98413 only when the port has indicated to the ATM device that it is ready to receive at least one complete cell. The μPD98413 indicates transmit cell buffer available information to the ATM device. The TXCLAV0-3 are not applicable on the first cycle after TXSOC is asserted, on this cycle, the μPD98413 keeps the status before the transfer is started. The μPD98413 will deassert TXCLAV unless it can accept at least one cell (after the currently transferred cell) from the ATM device. Once the TXCLAV0-3 has been asserted, it will have to stay asserted until the clock edge after assertion of the next TXSOC on that particular port. The FIFO availability information indicated by TXCLAV is programmable by the FTHT register.

The port to which the next cell will be sent will be selected by TXADDR[1:0] during the clock cycle before TXENB_B is asserted. This signal will be decoded by the μPD98413 and the specified port will be ready to receive cell data from the ATM device as soon as the TXENB_B is asserted.

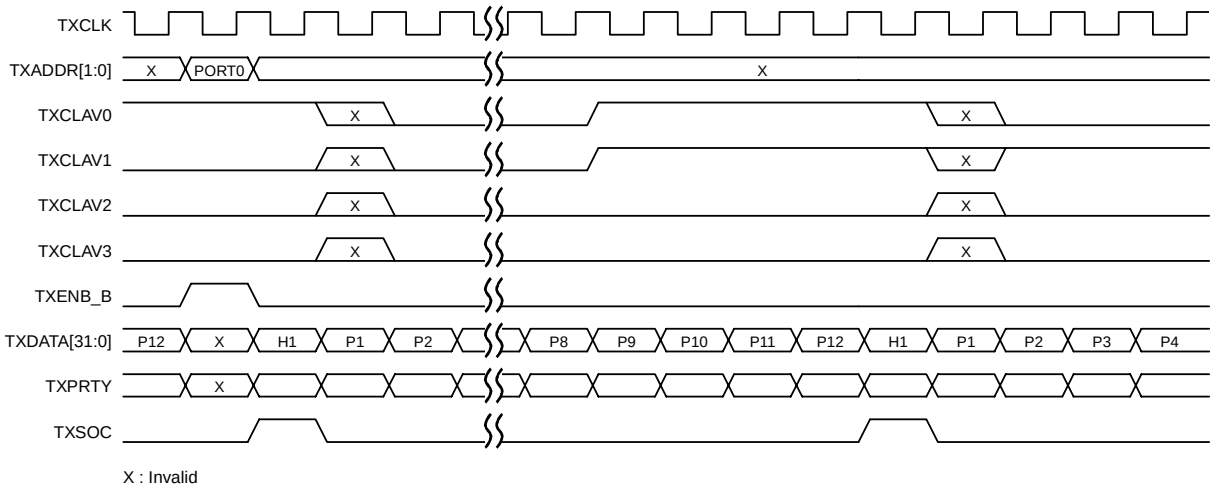
The following figure shows an example of the transmit timing in the direct status indication.

Figure 4-5. Transmit Timing (Direct Status Indication)



Back-to-back transfer of cells is possible when two cells have to be sent the same port and this port indicates that it can receive the second cell. In the case of back-to-back transfer the ATM device does not explicitly select the µPD98413 port and TXENB_B will not be deasserted. The second cell is transferred immediately after the previous one and the TXSOC is asserted to indicate the start of cell. This example is illustrated below.

Figure 4-6. Back-to-back Cell Transmission (Direct Status Indication)



(2) Status polling (Multi-PHY operation with 1 TXCLAV)

In the status-polling mode, the ATM device can receive the μPD98413 port FIFO status information through the polling mechanism. In this mode, only TXCLAV0 is used. TXCLAV1-3 are not used, and these signals are fixed to low.

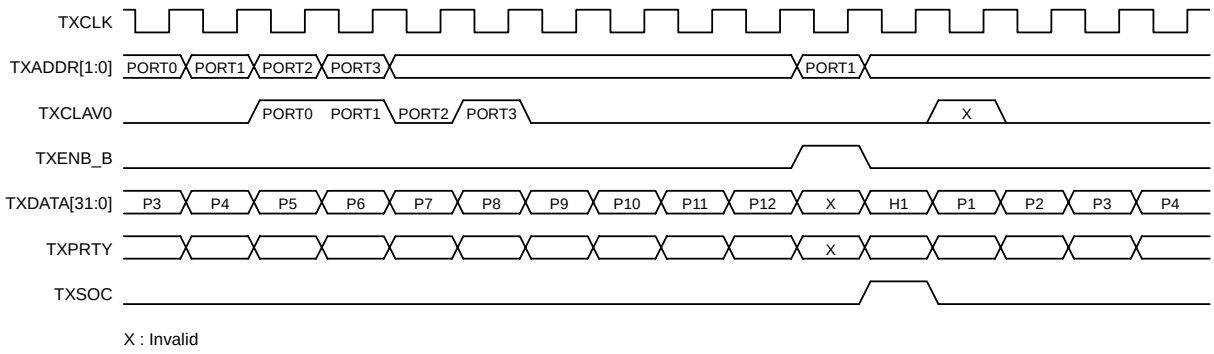
The ATM device can send a cell to the μPD98413 only when the port has indicated to the ATM device that it is ready to receive at least one complete cell. The μPD98413 sends transmit cell buffer available information for that port to the ATM device when that port is polled, using the TXCLAV0. Once the TXCLAV0 response for a particular port indicates buffer availability, responses to subsequent polls of that port continues to indicate buffer availability until after the second cycle of the transfer of a cell to that port. The FIFO availability information indicated by TXCLAV0 is programmable by the FTHT register.

The ATM device polls by presenting the port address on TXADDR[1:0]. The μPD98413 responds two clock cycles later by driving TXCLAV0 high if the port can accept one or more complete ATM cells; TXCLAV0 is driven low otherwise. The TXCLAV0 is not applicable on the first cycle after TXSOC is asserted, on this cycle, the μPD98413 keeps the status before the transfer is started.

TXADDR[1:0] during the clock cycle before asserting the TXENB_B signal will select the port which will receive the next cell. The μPD98413 will decode this signal and the specified port will be ready to receive cell data from the ATM device at the next clock cycle.

The following figure shows an example of the transmit timing in the status polling.

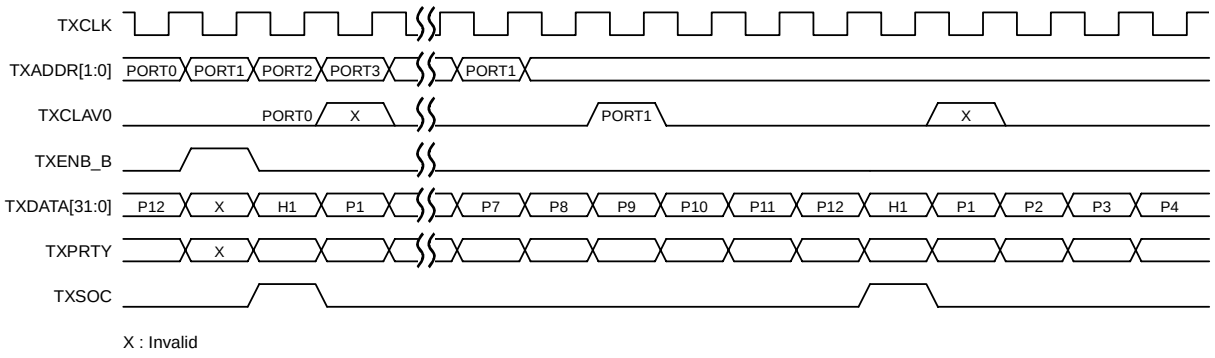
Figure 4-7. Transmit Timing (Status Polling)



X : Invalid

Back-to-back transfer of cells is possible when two cells have to be sent the same port and this port indicates that it can receive the second cell. In the case of back-to-back transfer the ATM device implicitly reselects the μPD98413 port by leaving the TXENB_B asserted during the next to the last cycle of the cell transfer. The second cell is transferred immediately after the previous one and the TXSOC is asserted to indicate the start of cell. This example is illustrated below.

Figure 4-8. Back-to-back Cell Transmission (Status Polling)



4.2.4 Receive operation

The μPD98413 supports both the direct status indication mode and the status-polling mode (Multi-PHY operation with 1 RXCLAV).

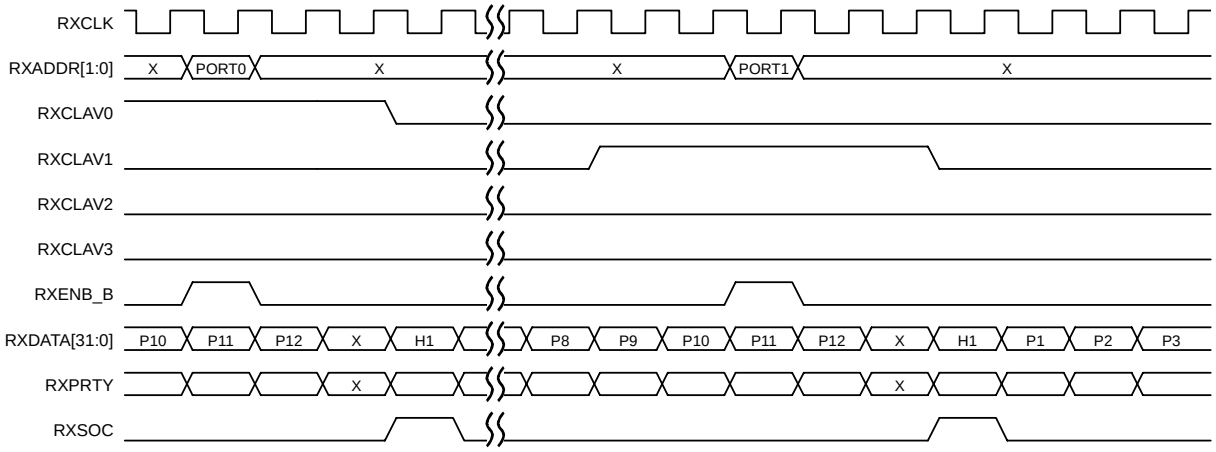
(1) Direct status indication

The μPD98413 implements a dedicated RXCLAV signal for each of the ports. RXCLAV0 corresponds to the port0, while RXCLAV3 corresponds to the port3.

The ATM device controls the flow of data from the μPD98413 on a per cell basis. The μPD98413 indicates receive cell available information to the ATM device. The ATM device can select a port for transfer of a cell when the port has indicated to the ATM device that it has at least one cell available. The μPD98413 deasserts the RXCLAV0-3 coincident with RXSOC to indicate that the corresponding port of the μPD98413 has no subsequent cell available. Once the RXCLAV0-3 has been asserted, it will have to stay asserted until the RXSOC is asserted on that particular port.

A valid RXADDR[1:0] during the clock cycle before asserting the RXENB_B signal will select the port which will transfer the next cell across the ATM interface. The μPD98413 decodes this signal and the specified port will be ready to transfer cell data two clock cycles after RXENB_B goes low. The ATM device must deassert RXENB_B two cycles before the end of the cell transfer, unless a back-to-back transfer is intended. The decode-response timing between the RXENB_B and the RXDATA[31:0] is therefore two clock cycles.

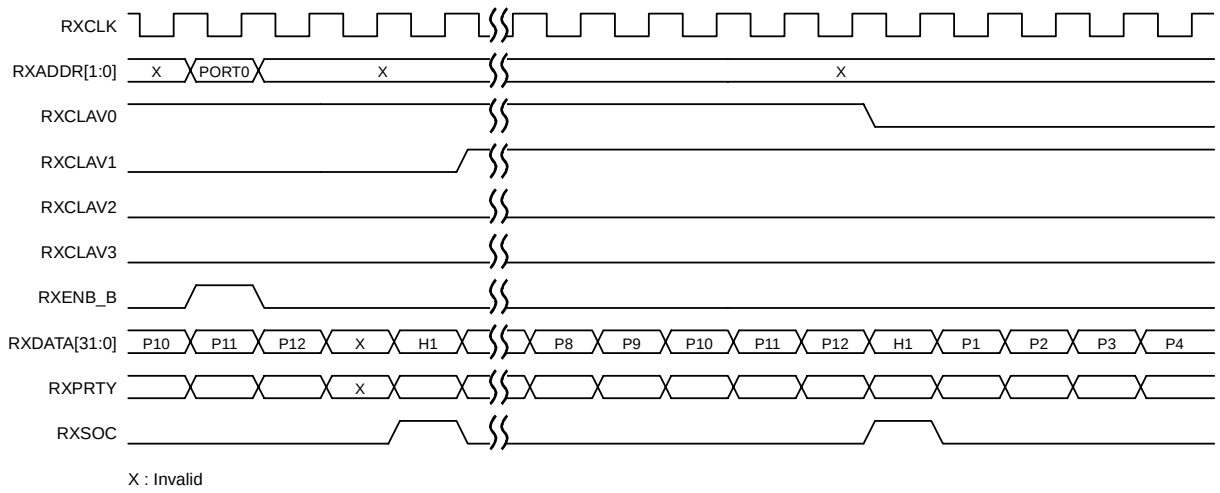
Figure 4-9. Receive Timing (Direct Status Indication)



X : Invalid

The μPD98413 supports back-to-back transfer of cells. In the case of back-to-back transfer the ATM device implicitly reselects the μPD98413 port and RXENB_B asserted during the next to the last cycle of the cell transfer. The second cell is transferred immediately after the previous one and the RXSOC is asserted to indicate the start of cell. This example is illustrated below.

Figure 4-10. Back-to-back Cell Reception (Direct Status Indication)



(2) Status polling (Multi-PHY operation with 1 RXCLAV)

In the status-polling mode, the ATM device can receive the μPD98413 port FIFO status information through the polling mechanism. In this mode, only RXCLAV0 is used. RXCLAV1-3 are not used, and these signals are fixed to low.

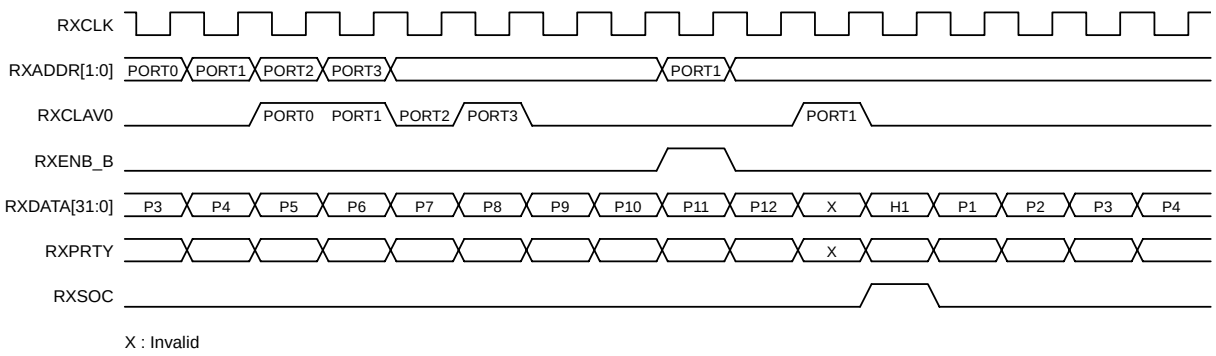
The ATM device controls the flow of data from the μPD98413 on a per cell basis. The ATM device can explicitly select the μPD98413 port for transfer of a cell only when the port has indicated to the ATM device that it has at least one cell available, using the RXCLAV0.

The ATM device polls by presenting the port address on RXADDR[1:0]. The μPD98413 responds two clock cycles later by driving RXCLAV0 high if the port is ready to send one or more complete ATM cells to the ATM device; RXCLAV0 is driven low otherwise. Once the RXCLAV0 response for a particular port indicates cell availability, responses to subsequent polls of that port continues to indicate cell availability until the RXSOC is asserted for that port.

RXADDR[1:0] during the clock cycle before asserting the RXENB_B signal will select the port which will transfer the next cell across the ATM interface. The μPD98413 will decode this signal and the specified port will be ready to transfer cell data two clock cycles before the end of the cell transfer, unless a back-to-back transfer is intended. The decode-response timing between the RXENB_B and the RXDATA[31:0] is therefore two clock cycles.

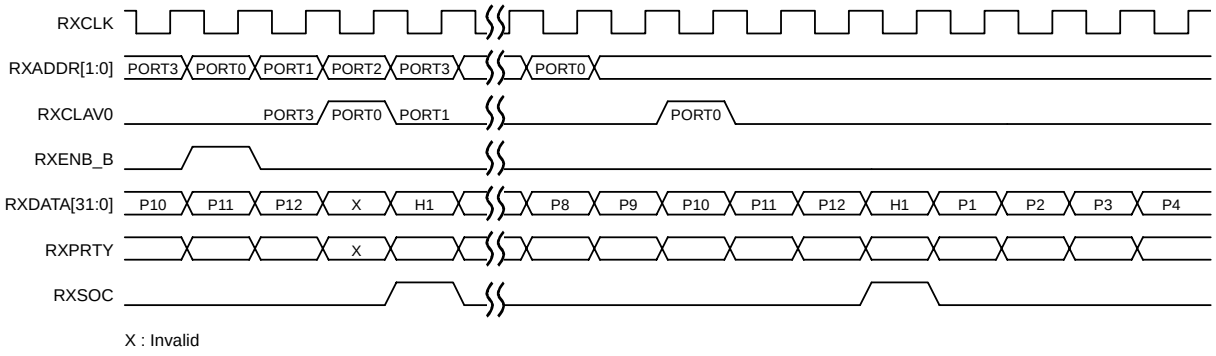
The following figure shows an example of the transmit timing in the status polling.

Figure 4-11. Receive Timing (Status Polling)



Back-to-back reception of cells is possible when two or more cells have to be received from the same port and the ATM device can receive the second cell. In the case of back-to-back transfer the ATM device does not explicitly select the μPD98413 port as transfer to the same port is assumed. The second cell is transferred immediately after the previous one and the RXSOC is asserted to indicate the start of cell. This example is illustrated below.

Figure 4-12. Back-to-back Cell Reception (Status Polling)



4.2.5 Parity

The μPD98413 supports a parity signal for the transmit and receive interface.

(1) Transmit parity

At the transmit side of the ATM interface, the μPD98413 checks a parity input by TXPRTY while TXENB_B is asserted. If a parity error is detected, the μPD98413 indicates the error by the APIET register.

The μPD98413 supports both odd and even parity by setting the MDAPIT register. The default mode is odd.

(2) Receive parity

At the receive side of the ATM interface, the μPD98413 always generates a parity over RXDATA[31:0] and outputs by RXPRTY.

The μPD98413 supports both odd and even parity by setting the MDAPIR register. The default mode is odd.

4.2.6 ATM Interface Error Detection

The μPD98413 can detect some errors in the ATM interface and indicates the error by the register.

(1) Transmit error

At the transmit side of the ATM interface, the μPD98413 detects the following errors and indicates the error by the APIET register.

- Parity error (UTOPIA Interface)

The μPD98413 checks a parity input by TXPRTY while TXENB_B is asserted. If a parity error is detected, the μPD98413 indicates the error by the APIET register.

- Parity error (Transmit FIFO)

The μPD98413 is generate the parity when transmit cell is stored in the transmit FIFO, and check the parity when transmit cell is take out from the transmit FIFO. If a parity error is detected, the μPD98413 indicate the error by the APIET register.

- Cell Discard error

If the μPD98413 detect Cell Discard, because TXCLAV is ignored and transmit FIFO is overflow occurred, the μPD98413 indicate the error by the APIET register.

- TXENB_B and TSOC error

If the μPD98413 detect that TXENB_B is deasserted or TSOC is asserted while a cell transfer, the μPD98413 indicate the error by the APIET register.

(2) Receive error

At the receive side of the ATM interface, the μPD98413 detects the following errors and indicates the error by the APIER register.

- Parity error (Receive FIFO)

The μPD98413 is generate the parity when receive cell is stored in the receive FIFO, and check the parity when receive cell is take out from the receive FIFO. If a parity error is detected, the μPD98413 indicate the error by the APIER register.

- RXENB_B or RXSOC error

If the μPD98413 is detect that RXENB_B is deasserted or RXSOC is asserted while a cell transfer, the μPD98413 indicate the error by the APIER register.

- Port select error

If the μPD98413 select the port although the corresponding RXCLAV is low, the μPD98413 indicate the error by the APIER register.

4.3 POS Interface

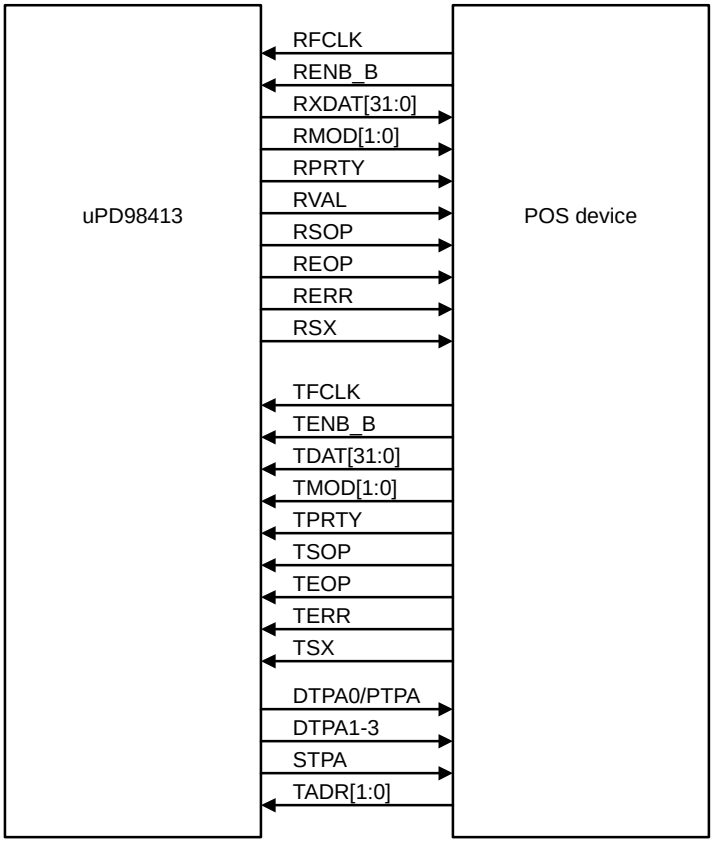
The POS interface transfers transmit and receive packet data to the POS device. The features of this interface are as follows:

- Compliant with POS-PHY™ Level3 issue 4.
- 32-bit, 104 MHz LVTTL FIFO interface.
- Supports direct status indication and status poling for the transmit interface.
- Executes a parity check on transmit data, generates and outputs a parity bit of receive data.
- Selectable FIFO threshold condition for Transmit Packet Available (TPA) signal indicating an available area of transmit FIFO for each port.
- 1K bytes transmit and receive FIFOs for each port.

4.3.1 Signals

An example of connecting the POS interface is shown below.

Figure 4-13. Example of Connecting the POS Interface



(1) Transmit interface

The transmit interface uses the signals defined below.

TFCLK (input): Transmit FIFO write clock.
TFCLK is used to synchronize data transfer transactions between the μPD98413 and the POS device. TFCLK cycles at a rate up to 104MHz.

TDAT[31:0] (input): Transmit packet data bus.
TDAT[31:0] carries the transmit packet data and the in-band port address. The TDAT bus is considered valid only when TENB_B is asserted. TDAT31 is the MSB, TDAT0 is the LSB.

TSOP (input): Transmit start of packet.
TSOP is used to delineate the packet boundaries on the TDAT bus. When TSOP is high, the start of the packet is present on the TDAT bus. TSOP is considered valid only when TENB_B is asserted.

TENB_B (input): Transmit write enable.
TENB_B is used to control the flow of data to the transmit FIFO. When TENB_B is high, the TDAT, TMOD, TSOP, TEOP, and TERR signals are invalid. TSX is valid when TENB_B is high.
When TENB_B is low, the TDAT, TMOD, TSOP, TEOP, and TERR signals are valid. TSX is invalid when TENB_B is low.

TPRTY (input): Transmit bus parity.
TPRTY indicates the parity calculated over the TDAT bus. TPRTY is considered valid only when TENB_B or TSX is asserted.
The μPD98413 supports the odd or even parity. When the μPD98413 detects a parity error, the μPD98413 indicates it by the register. Even if a parity error is detected, data transfer continues without being affected.

TEOP (input): Transmit end of packet.
TEOP is used to delineate the packet boundaries on the TDAT bus. When TEOP is high, the data on TDAT is assumed to be the end of a packet, and the valid bytes of the last word are indicated by TMOD[1:0]. TEOP is considered valid only when TENB_B is asserted.

TMOD[1:0] (input): Transmit word modulo.
TMOD[1:0] indicates the valid bytes of the transmit data on TDAT[31:0]. When TEOP is asserted, the valid bytes on TDAT[31:0] are specified by TMOD[1:0] below.

00: TDAT[31:0] is valid.
01: TDAT[31:8] is valid.
10: TDAT[31:16] is valid.
11: TDAT[31:24] is valid.

TMOD[1:0] is considered valid only when TENB_B is asserted.

TERR (input): Transmit error.

TERR is used to indicate that there is an error in the current packet. TERR must be asserted when TEOP is asserted. When TERR goes high, the current packet is sent as an abort packet. TERR is considered valid only when TENB_B is asserted.

TSX (input): Transmit start of transfer.

TSX indicates when the in-band port address is presented on the TDAT bus. When TSX is high and TENB_B is high, the port used to start transfer can be selected with the port address input to TDAT[7:0]. TSX is considered valid only when TENB_B is not asserted.

The in-band port address specified the port can be set any value by the IADRT register. By default, the following addresses show the corresponding ports.

0: port0, 1: port1, 2: port2, 3: port3

DTPA0-3 (output): Direct transmit packet available.

DTPA provides direct status indication for the corresponding ports in the μPD98413 port. DTPA0 corresponds to the port0, DTPA3 corresponds to the port3. DTPA0-3 are used in the direct status indication mode.

DTPA transitions high when a predefined minimum number of bytes is available in the transmit FIFO. When DTPA transitions low, it indicates that the transmit FIFO is almost full.

DTPA is updated on the rising edge of TFCLK.

STPA (output): Selected port transmit packet available.

STPA always provides status indication for the selected port. The port which STPA reports is updated on the following rising edge of TFCLK after the μPD98413 samples the in-band port address on TDAT.

STPA transitions high when a predefined minimum number of bytes is available in the transmit FIFO. When STPA transitions low, it indicates that the transmit FIFO is almost full.

STPA is updated on the rising edge of TFCLK.

PTPA (output): Polled port transmit packet available.

PTPA allows the polling of the port selected by the TADR[1:0]. The port which PTPA reports is updated on the following rising edge of TFCLK after the μPD98413 samples the in-band port address on TDAT. PTPA is used in the status polling mode.

PTPA transitions high when a predefined minimum number of bytes is available in the transmit FIFO. When STPA transitions low, it indicates that the transmit FIFO is almost full.

PTPA is updated on the rising edge of TFCLK.

TADR[1:0] (input): Transmit port address.

TADR[1:0] is used with the PTPA signal to poll the transmit FIFO's packet available status. TADR[1:0] is used in the status polling mode.

When the μPD98413 samples TADR[1:0] on the rising edge of TFCLK, the PTPA signal is updated with the status of the port specified by TADR[1:0] on the following rising edge of TFCLK. The following addresses show the corresponding ports.

0: port0, 1: port1, 2: port2, 3: port3

(2) Receive interface

The receive interface uses the signals defined below.

RFCLK (input): Receive FIFO write clock.
RFCLK is used to synchronize data transfer transactions between the μPD98413 and the POS device. RFCLK cycles at a rate up to 104MHz.

RDAT[31:0] (output): Receive packet data bus.
RDAT[31:0] carries the receive packet data and the in-band port address. The RDAT bus is considered valid only when RVAL is asserted. RDAT31 is the MSB, RDAT0 is the LSB.

RSOP (output): Receive start of packet.
RSOP is used to delineate the packet boundaries on the RDAT bus. When RSOP is high, the start of the packet is present on the RDAT bus. RSOP is considered valid only when RVAL is asserted.

RENB_B (input): Receive read enable.
RENB_B is used to control the flow of data from the receive FIFO. When RENB_B is low, the RDAT, RPRTY, RMOD, RSOP, REOP, RERR, RSX and RVAL signals are updated on the following rising edge of RFCLK.
When RENB_B is high, the RDAT, RPRTY, RMOD, RSOP, REOP, RERR, RSX and RVAL signals will remain unchanged on the following rising edge of RFCLK.

RPRTY (output): Receive bus parity.
RPRTY indicates the parity calculated over the RDAT bus. RPRTY is considered valid only when RVAL or RSX is asserted.
The μPD98413 supports the odd or even parity.

REOP (output): Receive end of packet.
REOP is used to delineate the packet boundaries on the RDAT bus. When REOP is high, the data on RDAT is assumed to be the end of a packet, and the valid bytes of the last word are indicated by RMOD[1:0]. REOP is considered valid only when RVAL is asserted.

RMOD[1:0] (output): Receive word modulo.
RMOD[1:0] indicates the valid bytes of the transmit data on RDAT[31:0]. When REOP is asserted, the valid bytes on RDAT[31:0] are specified by RMOD[1:0] below.

00: RDAT[31:0] is valid.
01: RDAT[31:8] is valid.
10: RDAT[31:16] is valid.
11: RDAT[31:24] is valid.

RMOD[1:0] is considered valid only when RVAL is asserted. RMOD[1:0] is 0, except during the last word transfer of a packet.

RERR (output): Receive error.
RERR is used to indicate that there is an error in the current packet. The μPD98413 asserts RERR when REOP is asserted. RERR is considered valid only when RVAL is asserted.

RVAL (output): Receive data valid.
RVAL indicates the validity of the receive signals. When RVAL is high, RDAT, RMOD, RSOP, REOP and RERR signals are valid. RSX is invalid when RVAL is high. When RVAL is low, RDAT, RMOD, RSOP, REOP and RERR signals are invalid. RSX is valid when RVAL is low.

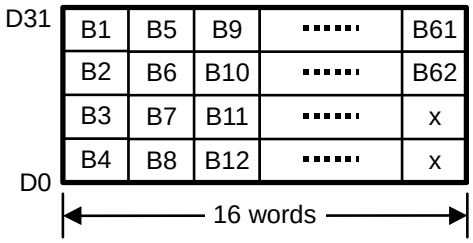
RSX (output): Receive start of transfer.
RSX indicates when the in-band port address is presented on the RDAT bus. When RSX is high and RVAL is low, RDAT[7:0] is the in-band port address selected port.
The in-band port address specified the port can be set any value by the IADRR register. By default, the μPD98413 outputs the following addresses for the corresponding ports.
0: port0, 1: port1, 2: port2, 3: port3

4.3.2 Packet Formats

The format of the packet transferred via the POS interface in the following figure.

Figure 4-14. Packet Format

Example: 62-byte packet



4.3.3 Transmit operation

The μPD98413 supports both the direct status indication mode (Byte-level mode) and the status polling mode (Packet-level mode). This mode is selectable by the APIMM bit of the MDDGEN register.

(1) Direct status indication (Byte-level mode)

The μPD98413 implements a dedicated DTPA signal for each of the ports. DTPA0 corresponds to the port0, while DTPA3 corresponds to the port3. The μPD98413 also implements the STPA signal for selected port.

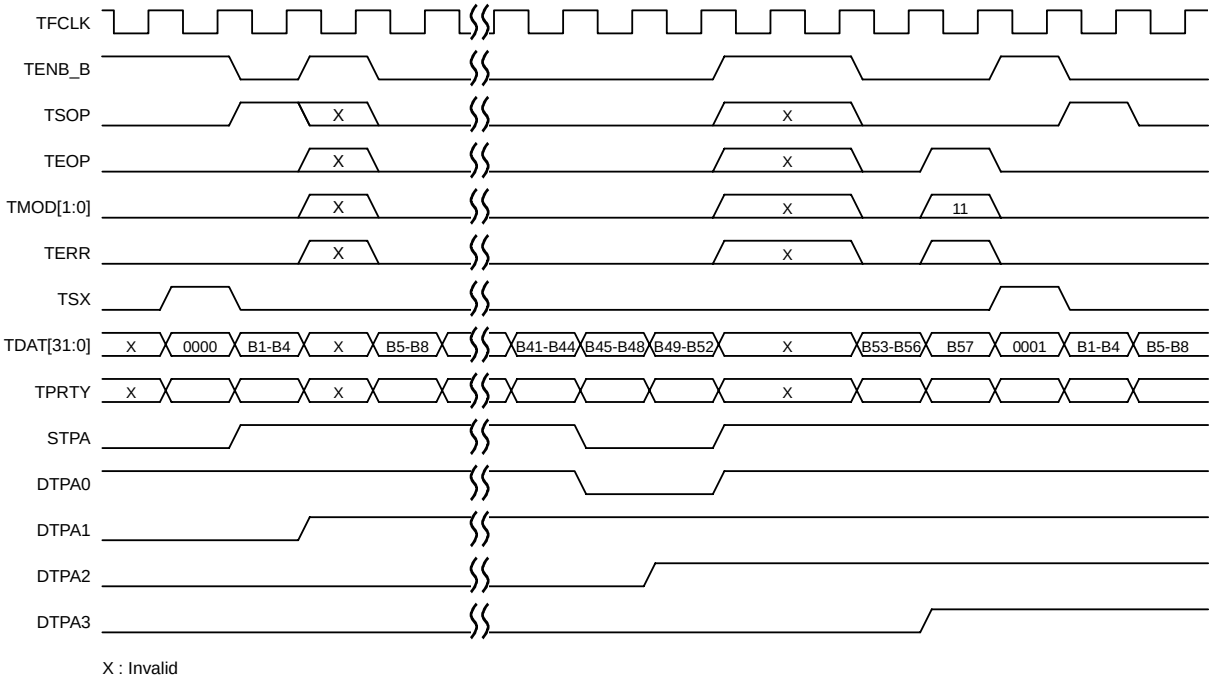
The transmit interface is controlled by the POS device using the TENB_B signal. All signals is updated and sampled using the rising edge of TFCLK.

Figure 4-17 is an example of the transmit timing. The μPD98413 indicates that the FIFO is not full by asserting DTPA. DTPA remains asserted until the transmit FIFO is almost full. The FIFO availability information that indicated by DTPA and STPA is programmable by the FTHT1 and FTHT2 register.

If DTPA is asserted and the POS device is ready to transfer the transmit data, it asserts TSX, deasserts TENB_B and presents the port address on the TDAT bus. Subsequent data transfers with TENB_B low are treated as packet data that is sent to the selected port. At any time, if the POS device does not have data to send, it can deassert TENB_B. The TSOP and TEOP signals must be marked at the start and end of packets on the TDAT bus. When TEOP is asserted, the valid bytes on the TDAT bus are specified by TMOD[1:0]. The POS device can indicate that there is an error in the current packet by TERR. TERR must be asserted when TEOP is asserted.

In the direct status indication mode, the PTPA and TADR[1:0] signals are not used.

Figure 4-15. Transmit Timing (Direct Status Indication)



(2) Status polling (Packet-level mode)

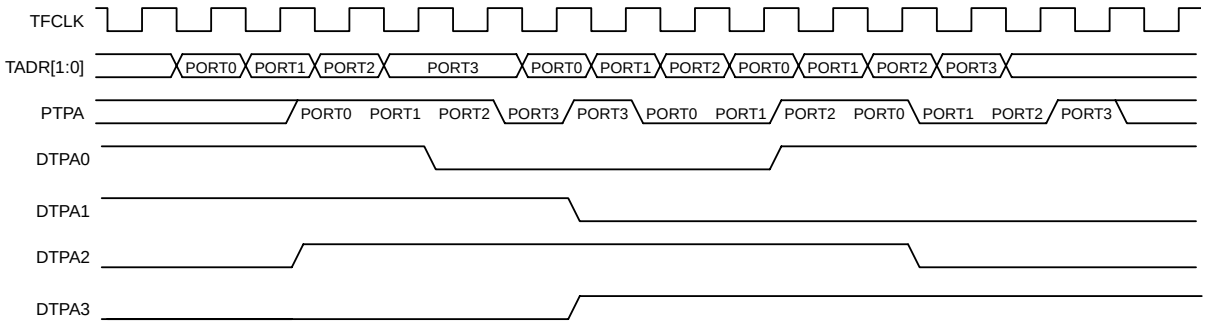
In the status polling mode, the POS device can receive the μPD98413 port FIFO status information through the polling mechanism. In this mode, PTPA is used. DTPA1-3 are not used, and these signals are fixed to low.

Figure4-18 is an example of the status polling timing. The status of a given port is determined by setting the polling address TADR[1:0] to the port address. The polled transmit packet available signal PTPA is updated with the transmit FIFO status in a pipelined manner. The FIFO availability information indicated by PTPA is programmable by the FTHT register.

The POS device is not restricted in its polling order. The PTPA signal allows polling other ports at any time, including while a data transfer is in progress.

In the status polling mode, a data transfer is same operation as the direct status indication mode.

Figure 4-16. Status Polling Timing



4.3.4 Receive operation

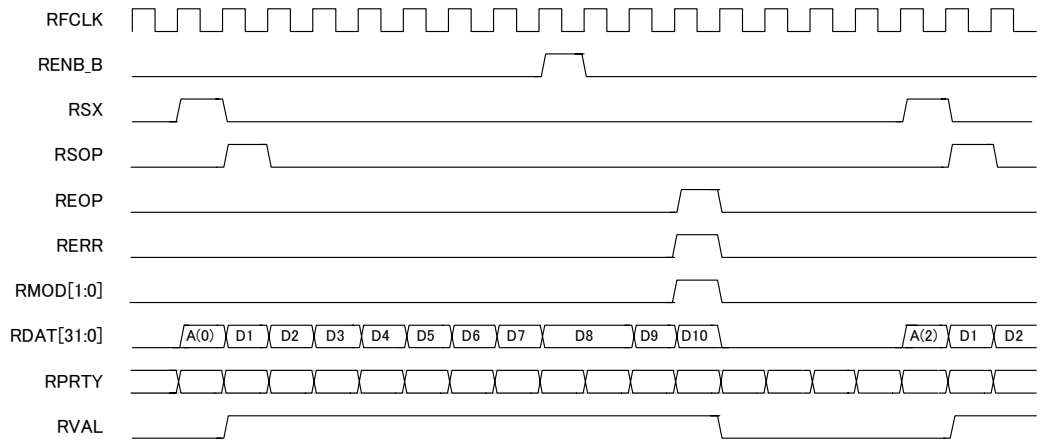
In the receive interface, the μPD98413 selects the port by itself, which there is a receive data in the receive FIFO and it should send the data to the POS device. This selection will be serviced in a round-robin fashion. Traditional polling schemes for the receive side are not supported.

(1) Normal receive operation

The receive interface is controlled by the POS device using the RENB_B signal. All signals are updated using the rising edge of RFCLK, when RENB_B is asserted.

Figure is an example of the receive timing. The μPD98413 informs the POS device of the selected port by asserting RSX with the port address on the RDAT bus.

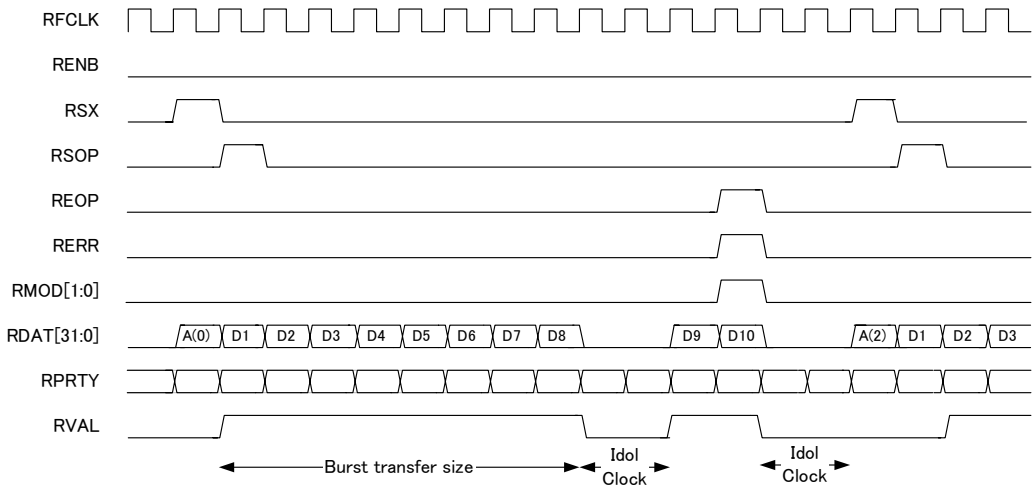
Figure 4-17. Receive Timing



(2) Idol clock inserted receive operation

The µPD98413 support the idol clock inserted receives operation. This receive operation is inserted idol clock (2 clocks) after burst transfer disconnected and resume without the port change. This mode is enabled by the IDLM bit of the MDAPIR register.

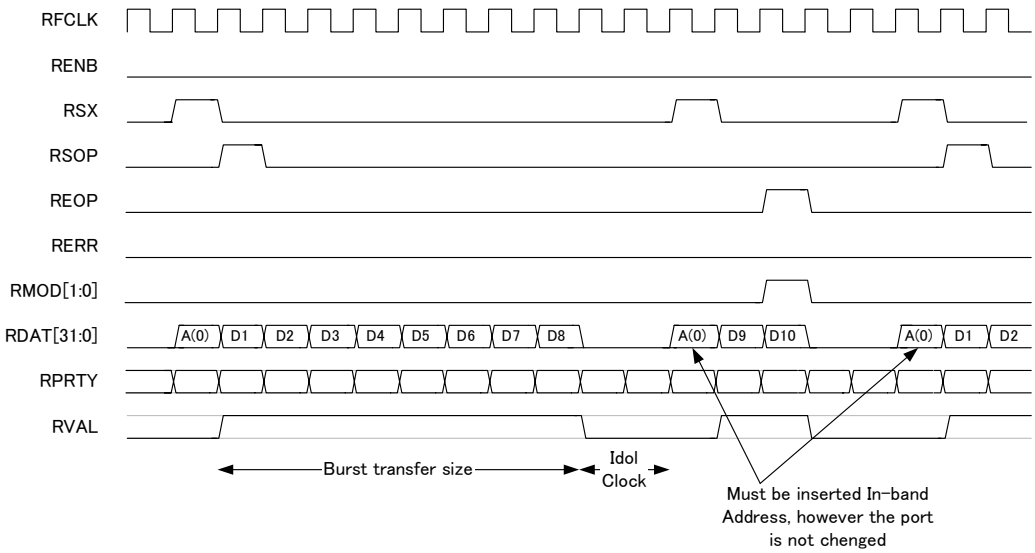
Figure 4-18 Idol clock inserted operation receive timing



(3) In-band address inserted receive operation

This receive operation must be inserted the in-band address after burst transfer disconnected and resume without the port change, however the port is not changed. This mode is enabled by the IADRM bit of the MDAPIR register.

Figure 4-19 In-band address inserted receive operation



4.3.5 Parity

The μPD98413 supports a parity signal for the transmit and receive interface.

(1) Transmit parity

At the transmit side of the POS interface, the μPD98413 checks a parity input by TPRTY while TENB_B or TSX is asserted. If a parity error is detected, the μPD98413 indicates the error by the PARE bit of the APIET register.

The μPD98413 supports both odd and even parity by setting the PARM of the MDAPIT register. The default mode is odd.

(2) Receive parity

At the receive side of the POS interface, the μPD98413 always generates a parity over RDAT[31:0] and outputs by RPRTY.

The μPD98413 supports both odd and even parity by setting the PARM of the MDAPIR register. The default mode is odd.

4.3.6 POS Interface Error Detection

The μPD98413 can detect some errors in the POS interface and indicates the error by the register.

(1) Transmit error

At the transmit side of the POS interface, the μPD98413 detects the following errors and indicates the error by the APIET register.

- End Of Packet (EOP) error (Wrong order for SOP and EOP)

The μPD98413 checks EOP Signal input by TEOP at end of every packet for each port. If EOP is asserting before Start Of Packet (SOP) is asserted, the μPD98413 is detect EOP error. If EOP error is detected, the μPD98413 indicates the error by the APIET register.

- Parity error (POS Interface)

The μPD98413 checks a parity input by TPRTY while TENB_B is asserted. If a parity error is detected, the μPD98413 indicates the error by the APIET register.

- Parity error (Transmit FIFO)

The μPD98413 is generate the parity when transmit packet is stored in the transmit FIFO, and check the parity when transmit packet is take out from the transmit FIFO. If a parity error is detected, the μPD98413 indicate the error by the APIET register.

- Packet discard error

If the μPD98413 detects packet discard, because TPA is ignore and transmit FIFO overflow occurs, the μPD98413 indicate the error by the APIET register.

(2) Receive error

At the receive side of the POS interface, the μPD98413 detects the following errors and indicates the error by the APIER register.

- Parity error (Receive FIFO)

The μPD98413 is generate the parity when receive packet is stored in the receive FIFO, and check the parity when receive packet is take out from the receive FIFO. If a parity error is detected, the μPD98413 indicate the error by the APIER register.

4.4 Overhead Insert/Extract Interfaces and Section/Line DCC Insert/Extract Interface

The μPD98413 has insert interfaces that input TOH and POH to be transmitted from external peripheral devices, and extract interfaces that output the contents of received TOH and POH.

And the μPD98413 provides access to both Section and Line Data Communication Channels (DCC). Both channels are accessed using the serial interface pins TSD, TLD, RSD and RLD, and their associated clocks TSDCLK, TLDCLK, RSDCLK and RLDCLK respectively.

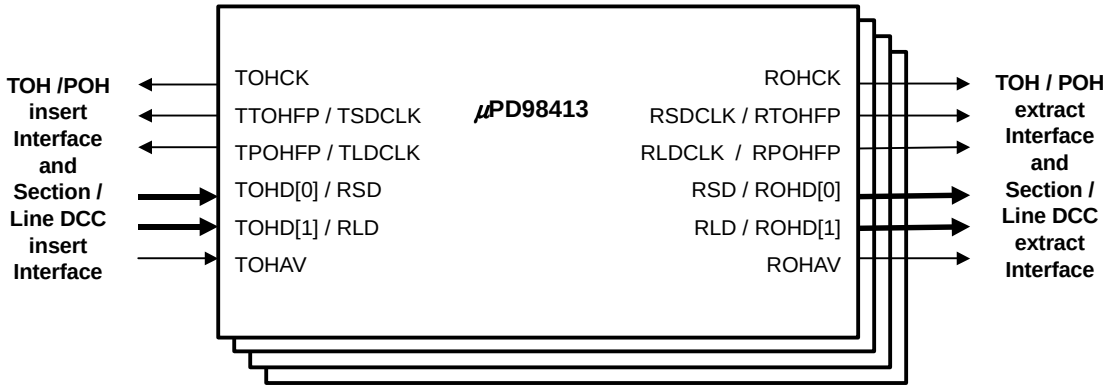
Both Overhead interface and DCC interface is multiplexed. Which interface to use is selected by the MDPT register. If both interfaces are enabled, the overhead interface is take precedence.

Table 4-1 Correspondence table of multiplexed OH interface and DCC interface

Pin Name	OH Interface	DCC Interface
TOHCLK	TOHCLK	Not Use
TTOHFP	TTOHFP	TSDCLK
TPOHFP	TPOHFP	TLDCLK
TOHAV	TOHAV	Not Use
TOHD [0]	TOHD [0]	TSD
TOHD [1]	TOHD [1]	TLD

Pin Name	OH Interface	DCC Interface
ROHCLK	ROHCLK	Not Use
RTOHFP	RTOHFP	RSDCLK
RPOHFP	RPOHFP	RLDCLK
ROHAV	ROHAV	Not Use
ROHD [0]	ROHD [0]	RSD
ROHD [1]	ROHD [1]	RLD

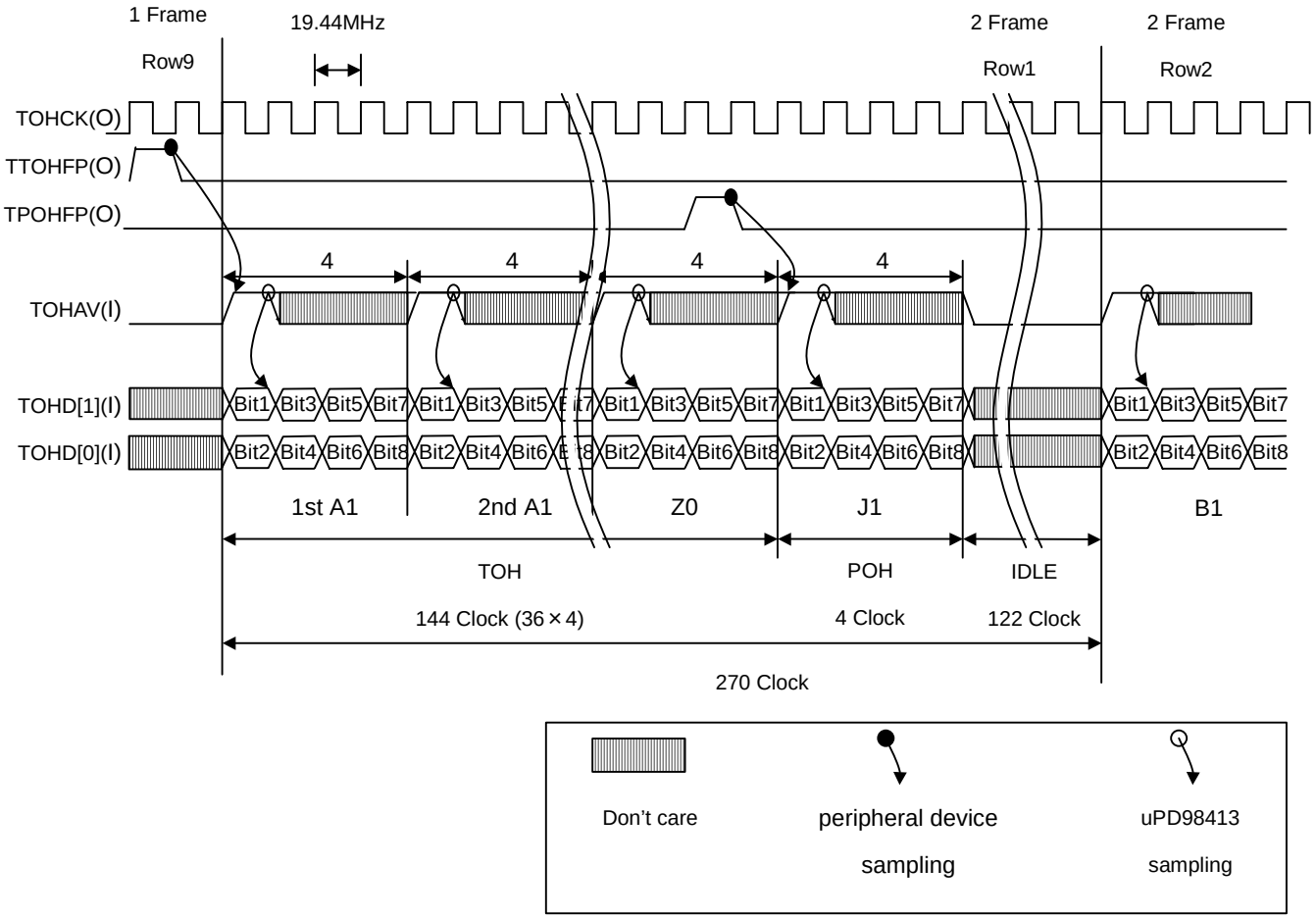
Figure 4-20. OH Insert / Extract Interfaces and Section / Line DCC Interfaces



4.4.1 OH Insert Interface

TOH / POH is input in sync with a 19.44-MHz clock as 2-bit parallel data.

Figure 4-21. TOH and POH Insert Interfaces



Figures 4-21 shows the timing charts of the TOH and POH insert interface.

The μPD98413 outputs a 19.44-MHz clock resulting from dividing the 622.08-MHz clock generated by the internal clock synthesizer by 32 from TOHCK. The μPD98413 outputs a pulse from TTOHFP (TPOHFP) to inform the external OH input controller (peripheral device) of when to start TOH (POH) data insertion. In normal transmission, TTOHFP is held high for one cycle from the second last rising edge of the last row of the previous frame. TPOHFP is held high for one cycle from the second last rising edge of the last Z0 byte on TOH.

The external OH input controller samples TTOHFP and TPOHFP at the rising edge of the clock. If it detects TTOHFP is high, the TOH data is input sequentially, starting from the first A1 byte, to TOHD [1:0] in sync with the next rising edge. If it detects TPOHFP is high, the POH data is input sequentially, starting from the J1 byte, to TOHD [1:0] in sync with the next rising edge.

As TOH (POH) data, one byte is input to the 2-bit parallel data lines TOHD [1:0] in 4 clock cycles. The μPD98413 samples and inputs TOHD [1:0] at the rising edge of TOHCK.

TOHAV is a signal by which the μPD98413 is informed it the external OH input controller is outputting valid data to TOHD [1:0]. The μPD98413 samples TOHAV at the clock edge of the first of the 4 cycles in which the one byte is input. While TOHAV is high, the bytes are input; while it is low, the bytes are ignored. TOHAV is ignored at the edge of the next three cycles.

The insertion timing of the TOH information is allocated to all the TOH bytes of 36 bytes × 9 rows. However, the TOH bytes shown in Table 4-5 cannot be changed by the TOH insert interface because the μPD98413 internally overwrites them for transmission even if they are inserted as valid data by driving TOHAV high.

The insertion timing is allocated to the nine bytes of the POH information. However, the POH bytes shown in Table 4-5 cannot be updated by the POH insert interface because it is internally overwritten by the μPD98413 even if valid data is inserted by driving TPOHAV high.

The OH bytes inputs as valid bytes from the TOH and POH insert interfaces are transmitted, taking precedence over the setting of the insert register and transmission of the J0 and J1 trace messages.

However, because the internal processing of the μPD98413, such as the transmission of BIP and REI and the transmission of a pointer, takes precedence, some bytes may be overwritten even if they are input from the insert interface.

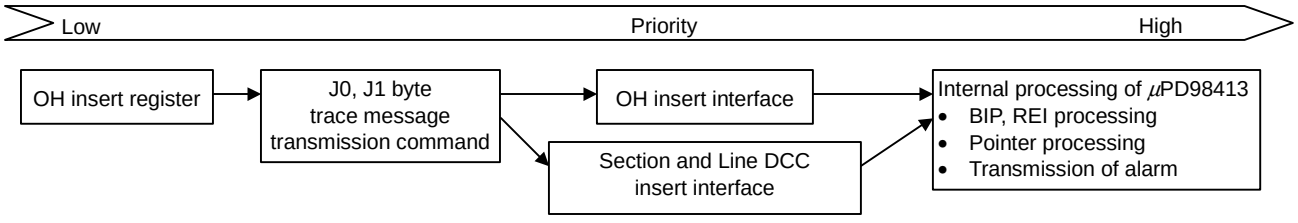


Table 4-5. OH Bytes That Cannot Be Changed from Insert Interface

TOH	A1	Synchronization pattern is always transmitted.
	A2	
	B1	Section BIP-8 is transmitted.
	B2	Line BIP-24 is always transmitted.
	H1	Pointer is always transmitted.
	H2	
	H3	
	M1	Line REI is always transmitted.
POH	B3	Path BIP-8 is always transmitted.
	G1 (bits 1-4)	Path REI is always transmitted.

If the transmission of Line AIS, Line RDI, or Path RDI is specified by using a register or pin, alarm transmission takes precedence, some bytes may be overwritten.

Table 4-6. OH Bytes That Cannot Be Changed When Alarm Is Transmitted

K2 (bits 6-8)	The μPD98413 processing needed to transmit an alarm takes precedence and '110' is transmitted if the automatic return function of Line RDI is effected, if the LRDI bit of the CMALM register is set, or if ‘011’ code is input to the TALMA-C pins.
G1 (bit 5-7)	If the automatic return function of (Enhance) Path RDI is effected, if the PRDI [2:0] bits of the CMALM register is set, alarm transmission takes precedence, and this bit is set to 1.
All bytes of LOH and POH	When the μPD98413 transmits alarm Line AIS, alarm transmission takes precedence, and all the bits are set to 1 for transmission.

4.4.2 OH Extract Interfaces

The OH extract interfaces are used to extract TOH and POH of a receive frame and output them to peripheral devices.

Figure 4-22. Example of Timing Chart of POH Insert Interface

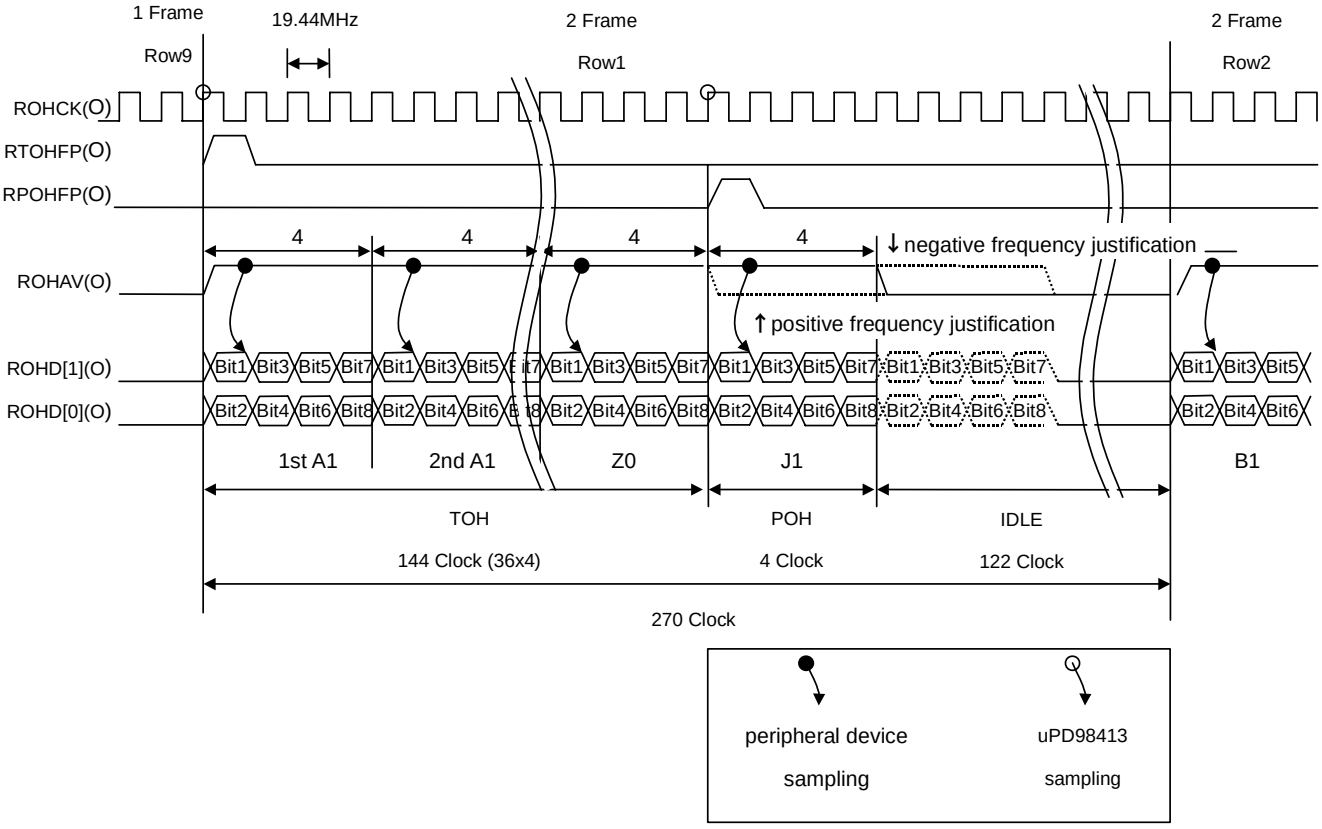


Figure 4-22 shows the timing charts of the TOH and POH extract interface.

This interface outputs all TOH (POH) bytes of the receive frame. The μPD98413 outputs a 19.44-MHz clock that is the receive clock extracted by the internal clock recovery divided by 36.

As TOH (POH) data, one byte is output to the 2-bit parallel data lines ROHD [1:0] in 4 clock cycles.

The μPD98413 outputs a pulse from RTOHFP (RPOHFP) to inform the external OH controller of the output start position of TOH (POH) data. Output of the TOH data is started from the rising edge at which RTOHFP goes high. After the output of the TOH data is complete, it begins the output of the POH data.

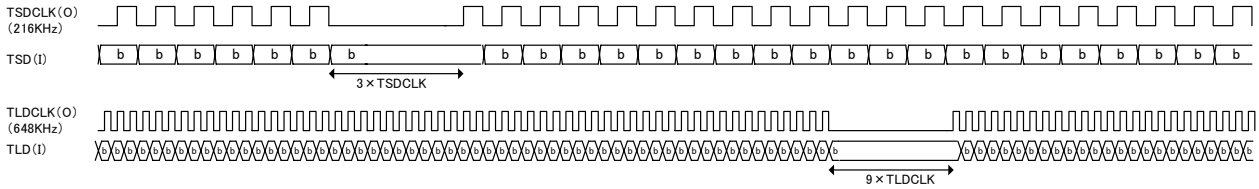
Output of the POH byte is started in sync with the rising edge at which RPOHFP goes high. In case of no frequency justification, the output of POH data is 1 byte. In case of positive frequency justification, POH doesn't sometimes exist. Therefore, in this case, makes ROHAV low to show by the dotted line of figure 4-22 and doesn't output POH. In case of negative frequency justification, sometimes POH exists 2 bytes. Therefore, in this case, ROHAV held high to show by the dotted line of figure 4-22 and output POH 2 bytes.

ROHAV is a signal by which the external OH controller is informed whether the μPD98413 is outputting valid TOH and POH data on ROHD [1:0]. While the frame synchronization has been established and a valid TOH and POH data is extracted, ROHAV is held high. If an alarm or fault such as LOS, LOF, OOF, and Line AIS is detected in the reception line, the μPD98413 drives ROHAV low to indicate that the output data on ROHD [1:0] is invalid.

4.4.3 Transmit Section and Line DCC Insert Interface

TSDCLK is a 216kHz. TLDCLK is a 648kHz. TSD is sampled on the rising edge of TSDCLK. TLD is sampled on the rising edge of TLDCLK. The D1-D3, and D4-D12 bytes shifted in to the μPD98413 in the frame shown are inserted in the corresponding transport overhead channels in the next frame.

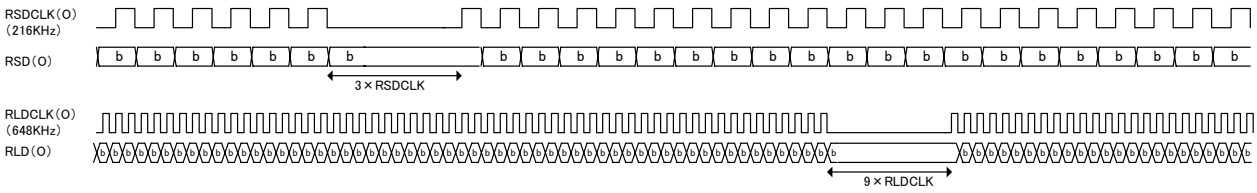
Figure 4-23. DCC Insert timing



4.4.4 Receive Section and Line DCC Extract Interface

RSDCLK is a 216kHz. RLDCLK is a 648kHz. RSD is updated on the falling edge of RSDCLK. RLD is updated on the falling edge of RLDCLK. The D1-D3, and D4-D12 bytes shifted out of the μPD98413 in the frame shown are extracted in the corresponding transport overhead channels in the previous frame.

Figure 4-24. DCC Extract timing



4.5 Frame Pulse input pins

The μPD98413 has a frame pulse input pin (TFPI). TFPI is used to align the SONET/SDH transport frame generated by the μPD98413 device to a system reference. When detected the frame pulse input from external peripheral devices, the μPD98413 starts transmit frame after fixed delay. Therefore, please avoid the usage every frame input. TFPI is sampled on the own rising edge. TFPI must be tied low if not use this pin. TFPI is enabled by the setting of the TFPE bit of the MDPT register.

4.6 General-Purpose Input and Output Ports

The μPD98413 has general-purpose output / input port pins. It is possible to change to input or output with the GPIOM [7:0] bits of MDDGEN register setting. Changes in the input level of a general-purpose input port pin can be used as the cause of an interrupt that is reported to the CPU.

General-Purpose Output

The output levels of these ports change according to the GPOUT register bit settings. When a certain bit is set to 1, the output level of the corresponding port becomes high. When the bit is set to 0, the output level becomes low. (By default, the register bits are set to 0.)

General-Purpose Input

The input levels of these ports are reflected on the status of the GPIN register of μPD98413. For each general-purpose input port, the GPIN register provides a pair of bits, one representing the actual input level and the other indicating the reversed input level. This pair of status bits and the mask setting of the GPIN_M register can be used to specify both negative transition (from high to low) and positive transition (from low to high) of the general-purpose input port as an interrupt cause.

GPIN and GPIN_M registers

D15 - D8	D7 - D0
PIN7L - PIN0L	PIN7H – PIN0H

GPIN register status

Input level	PIN0H-PIN7H	PIN0L-PIN7L
L	0	1
H	1	0

Caution: Note that the GPIN register bits are not latched.

[Example]

To report negative transition of the PIN0 pin as an interrupt

PIN0 = L → PI0L bit = 0
PI0H bit = 1

When the PI0H bit is set to 1 by masking the PI0L bit and unmasking the PI0H bit with the GPIN_M register, the GPIN bit of the INT register is set to 1. As a result, an interrupt is reported. The PIN0L and PIN0H bits of the GPIN register are not latched.

4.7 Alarm Insertion / Detection Pins

The μPD98413 has Alarm Insertion and Alarm Detection Pins.

4.7.1 Alarm Insertion Pins

These are input pins, which input the state signals from external peripheral devices. Each port has 3 pins, and alarm is inserted in the code form. Those input pins inputs synchronization with MCLK.

Signal Name	I/O	Function
TALMA 0-3 TALMB 0-3 TALMC 0-3	I	Alarm signal input. The alarm, which it is possible to insertion, is LAIS, PAIS, LRDI, PRDI, PERDI (Server defect, Connectivity defect, Payload defect) and the following code corresponds to TALMCx-TALMAx. 000: No Alarm 001: LAIS 010: PAIS 011: LRDI 100: One-bit PRDI mode - PRDI (one-bit PRDI, G1 bit5 : 1) Enhanced PRDI mode - PERDI Server defect (G1 bit5-7 : 101) 101: PERDI Connectivity defect (G1 bit5-7 : 110) 110: PERDI Payload defect (G1 bit5-7 : 010) 111: Reserved TALMx 0 corresponds to PORT0, while TALMx 3 corresponds to PORT3. **Example:** TALMA 0 = 1, TALMB 0 = 0, TALMC 0 = 0, then the LAIS alarm is transmitted to port 0.

4.7.2 Alarm Detection Pins

Each port has 3 pins. These pins output a signal indicating that an internally monitored error state has been detected. The pins can output an error either singly or in combination. The errors to be indicated are selected by using the RALMR register. If an event occurs, the corresponding alarm pin goes high.

Signal Name	I/O	Function
RALMA 0-3 RALMB 0-3 RALMC 0-3	O	Alarm signal output. The errors to be indicated are selected by using the RALMR register. RALMx 0 corresponds to PORT0, while RALMx 3 corresponds to PORT3.

4.8 Management Interface

The management interface provides an interface with the microprocessor that controls µPD98413. The microprocessor can access the internal registers of the µPD98413 via the management interface.

The µPD98413 supports 32-bit multiplexed synchronous bus for connecting a microprocessor. These buses are general-purpose bus interfaces that require fewer external circuitries connecting the microprocessor bus.

Signal	I/O	Description
MCLK	I	Microprocessor bus Clock
AD31-0	I/O	Address / data bus
CS_B	I	I/O chip select signal
UWE_B	I	Upper word enable signal
R/W_B	I	Read / write select signal
RDY_B	O	Ready signal
INT_B	O	Interrupt Signal

4.8.1 Endian

The microprocessor bus is set to little endian as the default condition after reset. To connect a microprocessor with a big endian interface, set the MIFM bit of the MDDGEN register to “1”.

The µPD98413 controls access by using AD1 (address) and UWE_B as follows. To UWE_B, a negative logic high-order word valid signal or a negative logic 4-byte valid signal can be connected.

(a) Little endian (MIFM=”0”)

Address	UWE_B	Data	
AD1		AD [31:16]	AD [15:0]
0	0	Bit [31:16]	Bit [15:0]
0	1	Invalid	Bit [15:0]
1	0	Bit [31:16]	Invalid
1	1	Bit [31:16]	Invalid

(b) Big endian (MIFM=”1”)

Address	UWE_B	Data	
AD1		AD [31:16]	AD [15:0]
0	0	Bit [31:16]	Bit [15:0]
0	1	Bit [31:16]	Invalid
1	0	Invalid	Bit [15:0]
1	1	Invalid	Bit [15:0]

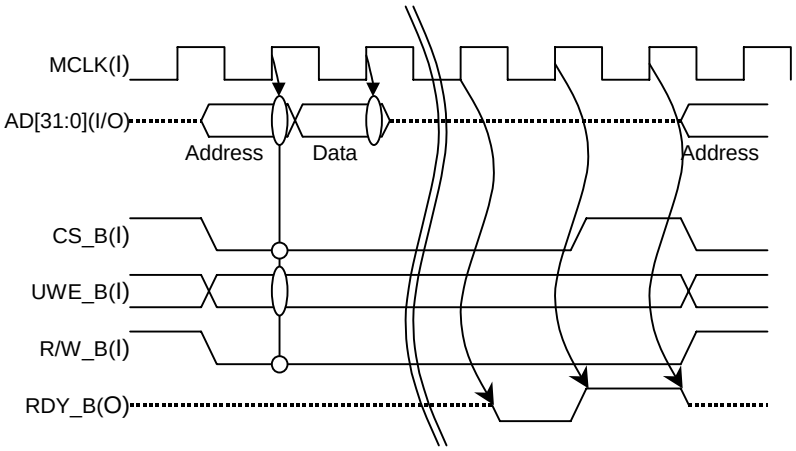
4.8.2 Access timing

When CS_B is asserted, AD [31:0], UWE_B, and R/W_B are loaded in synchronization with the rising of MCLK, and the register at the address indicated by AD [31:0] is accessed.

Write operation

If R/W_B is low, a write operation is started. The data on AD [31:0] is loaded in synchronization with the next rising of MCLK, and RDY_B is asserted when the operation in the next bus cycle is ready. When the write operation is ended, the μPD98413 negates RDY_B, and RDY_B goes into a high-impedance state at the next rising of MCLK. When the μPD98413 negate RDY_B, the microprocessor can deassert CS_B. The microprocessor must deassert CS_B at least 1clock cycle.

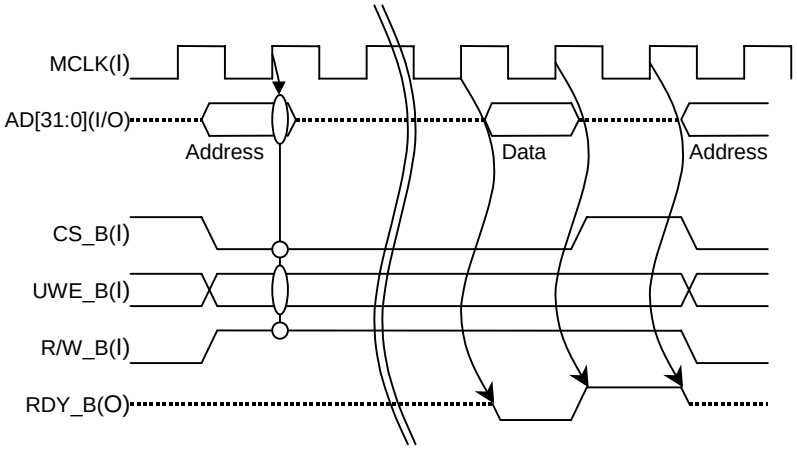
Figure 4-25. Write Access Timing



Read operation

If R/W_B is high, a read operation is started. When data output is ready, the data is output to AD[31:0] in synchronization with the rising of MCLK, and RDY_B is asserted. When the microprocessor has received the data, the μPD98413 negates RDY_B, and AD[31:0] go into a high-impedance state. At the next rising of MCLK, RDY_B goes in to a high-impedance state. When the μPD98413 negate RDY_B, the microprocessor can deassert CS_B. The microprocessor must deassert CS_B at least 1clock cycle.

Figure 4-26. Read Access Timing

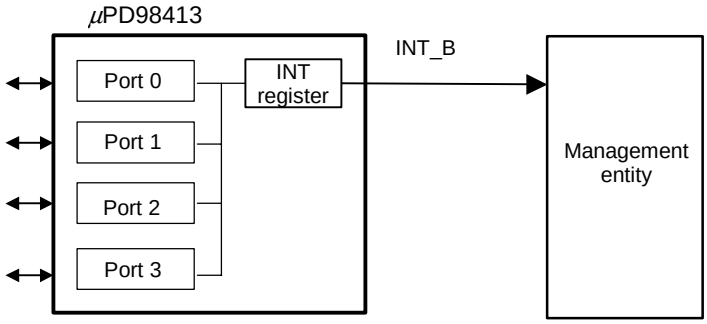

MCLK(I)
AD[31:0](I/O)
Address
Data
Address
CS_B(I)
UWE_B(I)
R/W_B(I)
RDY_B(O)

4.8.3 Interrupt

If an event occurs, such as line defect or alarm detection or performance counter overflow, µPD98413 activates the interrupt signal (INT_B) to notify the host of the event.

The interrupt signals for all four ports are multiplexed and output as a single INT_B pin. The port causing the interrupt signal to be output is indicated in the **INT** register.

Figure 4-27. Interrupt Signal



(1) Interrupt register, Interrupt causes register and detailed cause register

A register that identifies the cause of an interrupt consists of 6 separate registers: the interrupt register (INT), interrupt cause register and detailed cause register. The interrupt signal is activated if any of the INT register bits is set to 1. The bits of the INT register are set when even one of the bits of the corresponding Interrupt cause register is set to 1. The bits of the GEV, ICT and ICR register are set when even one of the bits of the corresponding detailed cause register at the lower stage is set to 1. When the host detects that an interrupt signal has been asserted active, it first reads the INT register, second reads the GEV, ICT and ICR registers and then reads the detailed cause register corresponding to the bit of the GEV, ICT and ICR registers that has been set, to identify the event that has occurred.

The bits of the GEV, ICT and ICR registers are only ORed with the bits of the detailed cause register. They are not latched. If a detailed cause register is cleared to all 0 by reading (or writing), the corresponding bit of the GEV, ICT and ICR register is also cleared to 0.

The GEV, ICT and ICR register and detailed cause register has a mask register. The bit arrangement of this mask register is the same as that of the corresponding cause register, so that each event can be masked or unmasked. Even if a masked bit of the INT register is set to 1, INT_B is not asserted active. Even if a masked bit of a detailed cause register is set to 1, it is not reflected on the GEV, ICT and ICR registers. Even when masked, the bits of the GEV, ICT and ICR registers and detailed cause register are set or reset depending on the detection status of an alarm or fault. In the default mode, all the causes are masked.

Figure 4-23. Types of Interrupt cause Register and Detailed cause Register

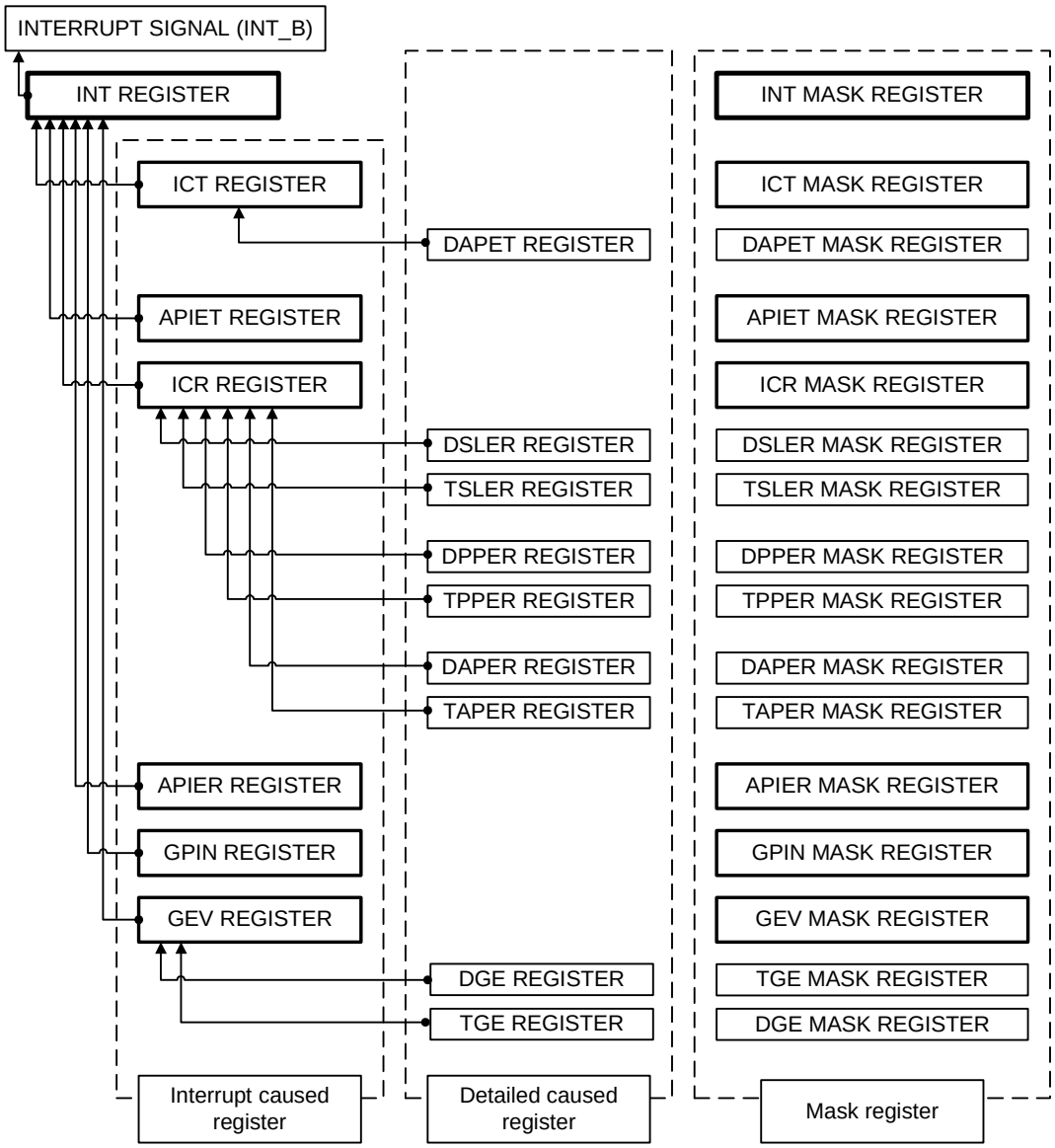


Table 4-7. Interrupt Port Register

Register	Outline
Interrupt register (INT)	• This register indicates the port of an interrupt occurrence. • If any of the bits of this register is set to 1, the interrupt signal (INT_B) is activated.

Table 4-8. Interrupt Cause Register

Register	Outline
Transmit interrupt cause register (ICT)	• This register indicates which detailed transmit cause register bit is set. • When at least one bit in this register is set to 1, the bit of the corresponding port in the INT register is set.
Transmit ATM/POS interface error register (APIET)	• The APIET register indicates the causes of a transmit ATM/POS interface error. • When at least one bit in this register is set to 1, the APIET bit in the INT register is set.
Receive interrupt cause register (ICR)	• This register indicates which detailed receive cause register bit is set. • When at least one bit in this register is set to 1, the bit of the corresponding port in the INT register is set.
Receive ATM/POS interface error register (APIER)	• The APIER register indicates the causes of a receive ATM/POS interface error. • When at least one bit in this register is set to 1, the APIER bit in the INT register is set.
General-purpose input port status register (GPIN)	• The GPIN register indicates the signal label of each general-purpose input pin. • When at least one bit in this register is set to 1, the GPIN bit in the INT register is set.
General event Register (GEV)	• The GEV register indicates cause of the General event. • When at least one bit in this register is set to 1, the GEV bit in the INT register is set.

Table 4-9. Detailed Cause Register

Register	Outline
Transmit ATM/POS layer event detection register (DAPET)	• This register indicates whether the occurrence of event was detected. • When at least one bit in the DAPET register is set to 1, the DAPET bit in the ICT register is set.
Receive section and line layer event detection registers (DSLER)	• This register indicates that section and Line layer event has detected. • When at least one bit in the DSLER register is set to 1, the DSLER bit in the ICR register is set.
Receive section and line layer event termination registers (TSLER)	• This register indicates that section and Line layer event has terminated. • When at least one bit in the TSLER register is set to 1, the TPPER bit in the ICR register is set.
Receive pointer and path layer event detection registers (DPPER)	• This register indicates that pointer and path layer event has detected. • When at least one bit in the DPPER register is set to 1, the DPPER bit in the ICR register is set.
Receive pointer and path layer event termination registers (TPPER)	• This register indicates that pointer and path layer event has terminated. • When at least one bit in the TPPER register is set to 1, the TPPER bit in the ICR register is set.
Receive ATM/POS layer event detection registers (DAPER)	• This register indicates that ATM/POS layer event has detected. • When at least one bit in the DAPER register is set to 1, the DAPER bit in the ICR register is set.
Receive ATM/POS layer event termination registers (TAPER)	• This register indicates that ATM/POS layer event has terminated. • When at least one bit in the TAPER register is set to 1, the TAPER bit in the ICR register is set.
General event termination register (DGE)	• This register indicates that general event has detected. • When at least one bit in the DGE register is set to 1, the DGE bit in the GEV register is set.
General event termination register (TGE)	• This register indicates that general event has terminated. • When at least one bit in the TGE register is set to 1, the TGE bit in the GEV register is set.

(2) Interrupt causes

Table 4-10 lists all the interrupt causes of μPD98413.

Table 4-10. Interrupt Cases List

(1/2)

Type	Event	Register
Section and line layer defect and alarm detection and termination	Detection and termination of Loss Of Signal (LOS) Detection and termination of Out Of Frame (OOF) Detection and termination of Loss Of Frame (LOF) Detection and termination of Section TIM Detection and termination of Section TIU Reception of Line AIS Reception of Line RDI Detection and termination of PSBF Detection and termination of SF Detection and termination of SD Detection of the B1 error Detection of the B2 error Detection of the B1 counter overflow Detection of the B2 counter overflow Reception of Line REI Detection of the Line REI counter overflow Reception of APS (Automatic Protection Signal) Storing J0 message has been completed.	DSLER TSLER
CD pin input activation	Detection and termination of high level of CD pin input.	DSLER TSLER
Pointer and path layer defect and alarm detection and termination	Detection and termination of Loss Of Pointer (LOP) Reception of Path AIS Reception of one-bit Path RDI Reception of Enhanced Path RDI Payload detect Reception of Enhanced Path RDI Connectivity detect Reception of Enhanced Path RDI Server detect Detection and termination of Path PLM Detection and termination of Path UNEQ Detection and termination of Path PLU Detection and termination of Path TIU Detection and termination of Path TIM Detection of the B3 error Detection of the B3 counter overflow Reception of Path REI Detection of the Path REI counter overflow Storing J1 message has been completed.	DPPER TPPER

(2/2)

Type	Event	Register
Receive ATM/POS layer event detection and termination	Detection of Out of Cell Delineation (OCD) Detection of Loss of Cell Delineation (LCD) Detection of the receive abort packet. Detection of the receive address error. Detection of the receive FCS error. Detection of the receive short packet. Detection of the receive long packet. Detection of the received valid cell/packet counter overflow Detection of the received idle cell counter overflow Detection of the received abort packet counter overflow Detection of the receive HEC correct cell counter overflow Detection of the receive address error packet counter overflow Detection of the receive HEC error drop cell counter overflow Detection of the receive FCS error packet counter overflow Detection of the receive FIFO full drop cell counter overflow Detection of the received long packet counter overflow Detection of the received short packet counter overflow	DAPER TAPER
Transmit ATM/POS layer event detection and termination	Detection of the transmit abort packet due to transmit FIFO underflow. Detection of the transmitted valid cell/packet counter overflow Detection of the transmitted abort packet counter overflow Detection of the transmit FIFO underflow packet counter overflow	DAPET TAPET
Receive ATM / POS interface error detection	Detection of that port is selected although the corresponding RXCLAV is Low. Detection of that RXENB_B is deasserted while a cell transfer. Detection of the receive FIFO-RAM parity error.	APIER
Transmit ATM / POS interface error detection	Detection of that TXENB_B is deasserted or TXSOC is asserted while a cell transfer. (ATM mode) Detection of wrong order for SOP and EOP (POS mode) Detection of a packet or cell discard. Detection of the ATM/POS interface parity error. Detection of the transmit FIFO-RAM parity error.	APIET
General event	Detection and termination of the port detection. Detection and termination of the busy status due to port reset.	DGE TGE
General-purpose input pin level change	Change in the PIN0-PIN7 input level	GPIN

(3) Change in bit of detailed causes register and interrupt cause register

The condition under which each bit of the detailed cause register is set or reset differs, as shown below.

Table 4-11. Set and Reset Conditions of Detailed Cause Register and interrupt cause register

Register	Set Condition	Reset Condition
DGE	Event detection	Cleared by CPU
DSLER register		
DPPER register		
DAPER register		
DAPET register		
TGE	Event termination	Cleared by CPU
TSLER register		
TPPER register		
TAPER register		

(4) Usage of Event Detection register and Event Termination registers

These registers indicate the statuses of the 25 events: Event detection and termination registers. By using these registers, the CPU can check the occurrence and end of an event.

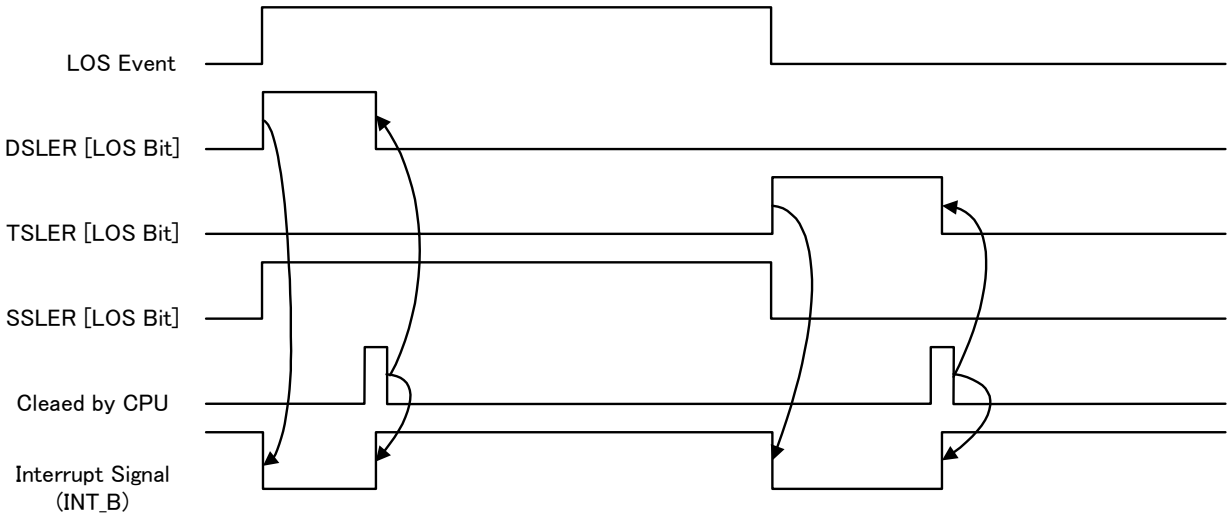
Figure 4-28 shows an example in which event LOS is detected by using the DSLER and TSLER registers. Each mask register is cleared so that the setting of the bits of the DSLER and TSLER registers is reflected on the ICR register. Similarly, the masking of the ICR register is cleared so that setting of the bits of the ICR register is reflected on the interrupt signal.

If the LOS event is detected, the LOS bit of the DSLER register and the DSLER bit of the ICR register are set to 1, and the INT_B signal is asserted active. The CPU that receives an interrupt signal reads the ICR and DSLER registers, in that order, to check the interrupt cause. When the CPU clears the LOS bit of the DSLER register, the DSLER bit of the ICR register is also cleared to 0, and INT_B is deasserted inactive. The LOS bit of the DSLER register remains set to 1 until it is cleared by the CPU.

If the LOS event ends, the LOS bit of the TSLER register and TSLER bit of the ICR register are set, and INT_B is asserted active again. When the LOS bit of the TSLER register is cleared, INT_B is deasserted inactive. The LOS bit of the TSLER register remains set to 1 until it is cleared by the CPU.

The SSLER register indicates the status of an event. The LOS bit of this register is set to 1 since LOS is detected until it ends. The setting the bits of this register is not used as an interrupt cause. If both the TSLER and TSLER bits of the ICR register are set when the register is read by the CPU, whether the LOS event has been detected and ended, or whether it has ended and then has been detected, can be determined by checking the status of the LOS bit of the SSLER register.

Figure 4-28. Bit Operations of DSLER and TSLER Registers



(5) Clearing the detailed cause register

The set bits of the detailed cause registers are cleared by CPU access. These bits may be cleared by reading or writing. Whether to clear by reading or writing can be specified for each bit. Each detailed cause register has three addresses: read clear, write clear, and read clear enable.

(a) Read clear

To clear a bit once it has been read, write 1 to the corresponding bit position at the read clear enable address. When the read clear address is read, only the bit for which 1 has been written to the corresponding bit position at the read clear enable address is cleared to 0. The bit that is disabled from being cleared by the read clear enable register is not cleared. In default mode, all the bits can be cleared once they have been read.

(b) Read only / Write clear

After reading the contents of a register, write 1 to the bit position in the register corresponding to the bit to be cleared. When write 0 to the register, the content of register is not clear.

Figure 4-29. Detailed Cause Register Clearing Method

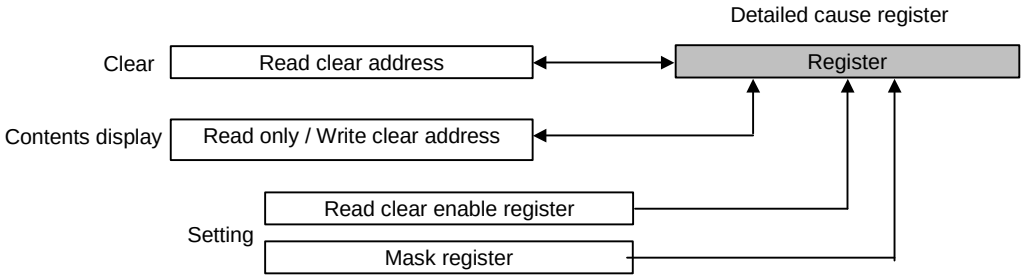


Table 4-12. Functions of the Interrupt Cause Registers

Access Destination	Description
Read clear address	This address is used for reading the contents of the register and then for clearing the register. Note that only those bits enabled in the read clear enable register are cleared to 0. Any attempt to perform write access to this address is ignored.
Read only / Write clear address	This address is used to read the contents of the register and used to write-clear the contents of the register. Write the address so that 1 written over the bit to be write-cleared.
Read clear enable register	This register is used to enable or disable the read clear operation on a per-bit basis. Only those bits set to 1 in this register are cleared to 0 when read access to the read clear address is performed. By default, all the bits are set to 1 (enable).
Mask register	This register is used to mask or unmask each interrupt cause. Masking the detailed cause register masks reflection on the PICR register, and masking of the PICR register masks asserting the interrupt signal active. By default, all the bits are set to 1, meaning that all the interrupt causes are masked.

CHAPTER 5 REGISTERS

The μPD98413 has registers that can be accessed via the CPU interface. These registers are used to specify commands, set operation modes, and analyze interrupt causes.

[Caution]

The data bit string of the SONET/SDH frame is sequentially transmitted from the MSB when it is transmitted from the line interface (circuit side). In this document, the MSB is always shown on the left side in tables and figures. Note that each bit in the overhead byte (OH byte) of the SONET/SDH frame is described in the following two ways:

Description **<1>** Bits 1 to 8

This description is mainly used to indicate the bit string of the overhead byte in the SONET/SDH frame in the order in which the bits are output from the line interface.

Description **<2>** D31 to D0 bits

This description is mainly used to indicate the bits in an internal register of the μPD98413. The bits correspond to the AD31 to AD0 pins of the external CPU interface.

<1> Indicating bits in overhead byte

Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7	Bit 8	Transmission sequence
1	2	3	4	5				→

D31	D30	D29	D28	D27	D26	D25	D24
D23	D22	D21	D20	D19	D18	D17	D16
D15	D14	D13	D12	D11	D10	D9	D8
D7	D6	D5	D4	D3	D2	D1	D0

<2> Indicating bits in internal register

(D31 is input/output to/from data bus AD31 of the CPU interface.)

In this document, the following two descriptions are also used to indicate the same overhead byte in the SDH/SONET frame.

	H1	**H1**	**H1**		**H1**	**H1**	**H2**	**H2**
Description **<1>**	1st H1	2nd H1	3rd H1		47th H1	48th H1	1st H1	2nd H1
Description **<2>**	H1#1	H1#2	H1#3		H1#47	H1#48	H1#1	H1#2

5.1 Register Map

Address (H)				Name	Function	R/W	Default
P0	P1	P2	P3				(H)
0000				MDDGEN	Device general mode	R/W	00000080
0004				PENB	Port enable	R/W	00000000
0008				SRST	Software reset	R/W	00000000
000C				VER	Version	R	--
0010				GPOUT	General-purpose output port control	R/W	00000000
0020	0420	0820	0C20	MDPGEN	Port general mode	R/W	00010000
0024	0424	0824	0C24	MDPT	Transmit port general mode	R/W	00000000
0028	0428	0828	0C28	MDPR	Receive port general mode	R/W	00000000
002C	042C	082C	0C2C	RALMA	Receive alarm port control A	R/W	00000000
0030	0430	0830	0C30	RALMB	Receive alarm port control B	R/W	00000000
0034	0434	0834	0C34	RALMC	Receive alarm port control C	R/W	00000000
0040	0440	0840	0C40	MDSOHT	Transmit SOH mode	R/W	00000000
0044	0444	0844	0C44	MDLOHT	Transmit LOH mode	R/W	00000000
0048	0448	0848	0C48	MDPTRT	Transmit pointer mode	R/W	00000000
004C	044C	084C	0C4C	MDPOHT	Transmit POH mode	R/W	00000000
0050	0450	0850	0C50	MDATMT	Transmit ATM mode	R/W	00000000
0054	0454	0854	0C54	MDPOST	Transmit POS mode	R/W	00000000
0058	0458	0858	0C58	PACT	Transmit POS Address and Control	R/W	000003FF
005C	045C	085C	0C5C	HPTNT	Transmit HALT pattern	R/W	00000000
0060				MDAPIT	Transmit ATM/POS interface mode	R/W	00000000
0064	0464	0864	0C64	FTHT1	ATM/POS transmit FIFO threshold 1	R/W	0010000D
0068	0468	0868	0C68	FTHT2	ATM/POS transmit FIFO threshold 2	R/W	00000010
006C	046C	086C	0C6C	PTADRT	Transmit port address	R/W	P0: 00000000 P1: 00000101 P2: 00000202 P3: 00000303
0070	0470	0870	0C70	MDSOHR	Receive SOH mode	R/W	00007D40
0074	0474	0874	0C74	J0PTN	J0 trace message synchronous pattern	R/W	0D0A0000
0078	0478	0878	0C78	MDLOHR	Receive LOH mode	R/W	0000000C
007C	047C	087C	0C7C	MDPTRR	Receive pointer mode	R/W	00002020
0080	0480	0880	0C80	MDPOHR	Receive POH mode	R/W	001337F0
0084	0484	0884	0C84	J1PTN	J1 trace message synchronous pattern	R/W	0D0A0000
0088	0488	0888	0C88	MDATMR	Receive ATM mode	R/W	000000A8
008C	048C	088C	0C8C	DCHP	Drop cell header pattern	R/W	00000100
0090	0490	0890	0C90	MDPOSR	Receive POS mode	R/W	00000000

0094	0494	0894	0C94	PACR	Receive POS Address and Control	R/W	000003FF
0098	0498	0898	0C98	HPTNR	Receive HALT pattern	R/W	00000000
009C	049C	089C	0C9C	PLENR1	Receive packet length 1	R/W	00000000
00A0	04A0	08A0	0CA0	PLENR2	Receive packet length 2	R/W	000005FC
00A4	04A4	08A4	0CA4	MDAPIR	Receive ATM/POS interface mode	R/W	00000000
00A8	04A(	08A8	0CA8	FTHR	POS receive FIFO threshold	R/W	00000010
00AC	04AC	08AC	0CAC	PTADRR	Receive port address and ATM TAG	R/W	P0: 00000000 P1: 00000101 P2: 00000202 P3: 00000303
00C0	04C0	08C0	0CC0	CMALM	Transmit alarm command	R/W	00000000
00C4	04C4	08C4	0CC4	PESOH	Transmit SOH pseudo error	R/W	00000100
00C8	04C8	08C8	0CC8	PELOH	Transmit LOH pseudo error	R/W	00010100
00CC	04CC	08CC	0CCC	PEPTR	Transmit pointer pseudo error	R/W	00000000
00D0	04D0	08D0	0CD0	PEPOH	Transmit POH pseudo error	R/W	00010100
00D4	04D4	08D4	0CD4	PEATM	Transmit ATM pseudo error	R/W	00000000
00E0	04E0	08E0	0CE0	MDBER	Bit error rate monitoring mode	R/W	00000202
00E4	04E4	08E4	0CE4	SFND	SF detection N parameter	R/W	00000000
00E8	04E8	08E8	0CE8	SFLMD	SF detection L and M parameter	R/W	00000000
00EC	04EC	08EC	0CEC	SFNT	SF termination N parameter	R/W	00000000
00F0	04F0	08F0	0CF0	SFLMT	SF termination L and M parameter	R/W	00000000
00F4	04F4	08F4	0CF4	SDND	SD detection N parameter	R/W	00000000
00F8	04F8	08F8	0CF8	SDLMD	SD detection L and M parameter	R/W	00000000
00FC	04FC	08FC	0CFC	SDNT	SD termination N parameter	R/W	00000000
0100	0500	0900	0D00	SDLMT	SD termination L and M parameter	R/W	00000000
0110	0510	0910	0D10	TMBT	Transmit trace message buffer	R/W	00000000
0114	0514	0914	0D14	TMDT	Transmit trace message buffer data	R/W	00000000
0118	0518	0918	0D18	CMTMT	Transmit trace message command	R/W	00000000
011C	051C	091C	0D1C	TMBR	Receive trace message buffer	R/W	00000000
0120	0520	0920	0D20	TMDR	Receive trace message buffer data	R/W	00000000
0124	0524	0924	0D24	CMTMR	Receive trace message command	R/W	00000000

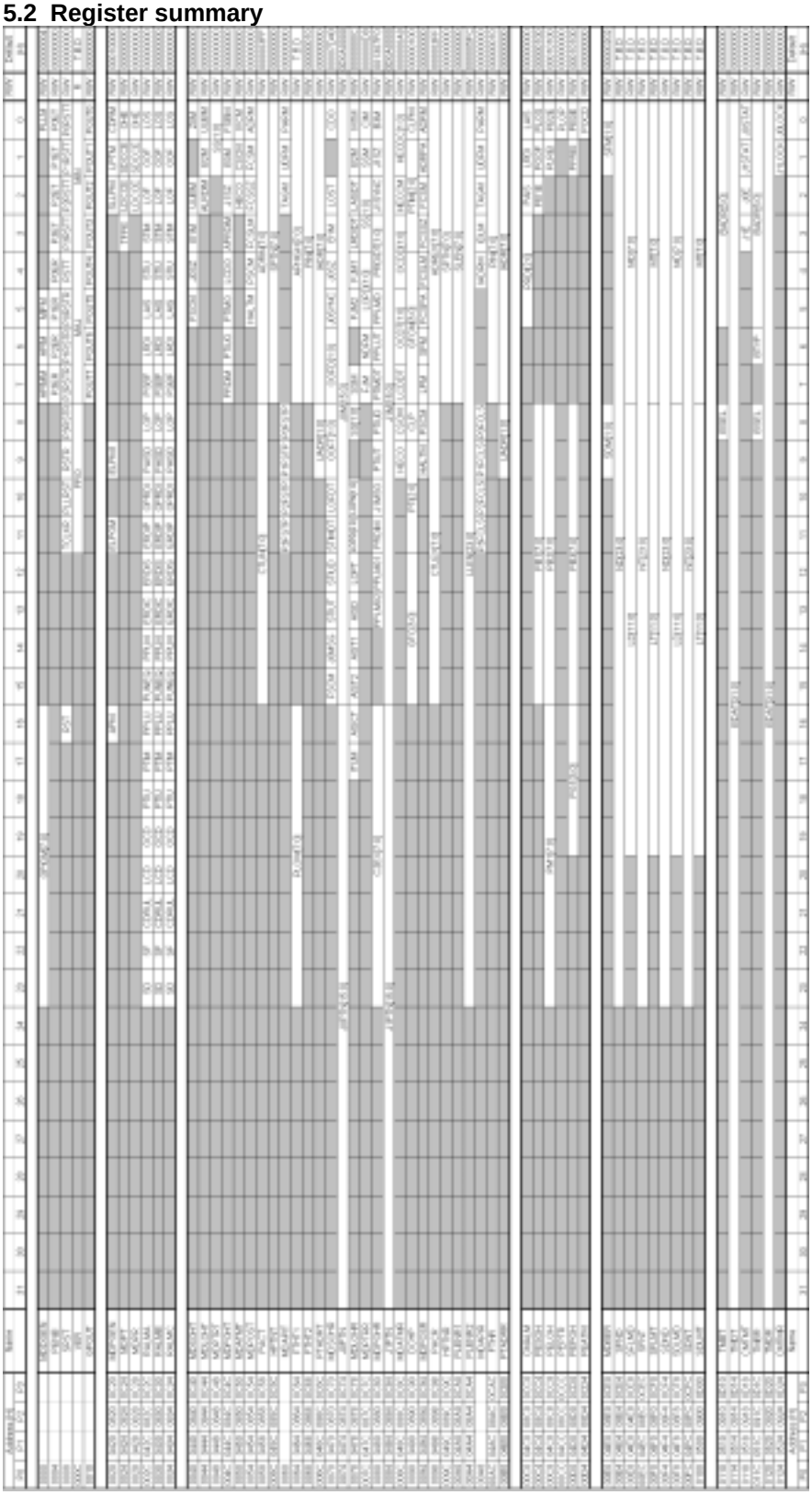
0140				INT_RO	Interrupt read only	R	00000000
0144				INT_M	Interrupt mask	R/W	00000FFF
0150	0550	0950	0D50	ICT_RO	Transmit interrupt cause read only	R	00000000
0154	0554	0954	0D54	ICT_M	Transmit interrupt cause mask	R/W	00000001
0160				APIET_RWC	Transmit ATM/POS interface error read only / write clear	R/WC	00000000
0164				APIET_RC	Transmit ATM/POS interface error read clear	RC	00000000
0168				APIET_RCE	Transmit ATM/POS interface error read clear enable	R/W	001FFFFF
016C				APIET_M	Transmit ATM/POS interface error mask	R/W	001FFFFF
0170	0570	0970	0D70	ICR_RO	Receive interrupt cause read only	R	00000000
0174	0574	0974	0D74	ICR_M	Receive interrupt cause mask	R/W	000001FF
0180				APIER_RWC	Receive ATM/POS interface error read only/ write clear	R/WC	00000000
0184				APIER_RC	Receive ATM/POS interface error read clear	RC	00000000
0188				APIER_RCE	Receive ATM/POS interface error read clear enable	R/W	0000FFFF
018C				APIER_M	Receive ATM/POS interface error mask	R/W	0000FFFF
0190				GPIN_RO	General-purpose input port status read only	R	**Note**
0194				GPIN_M	General-purpose input port status mask	R/W	0000FFFF
01A0				GEV_RO	General event read only	R	00000000
01A4				GEV_M	General event mask	R/W	00000003
01B0	05B0	09B0	0DB0	DAPET_RWC	Transmit ATM/POS layer event detection read only/ write clear	R/WC	00000000
01B4	05B4	09B4	0DB4	DAPET_RC	Transmit ATM/POS layer event detection read clear	RC	00000000
01B8	05B8	09B8	0DB8	DAPET_RCE	Transmit ATM/POS layer event detection read clear enable	R/W	0000007F
01BC	05BC	09BC	0DBC	DAPET_M	Transmit ATM/POS layer event detection mask	R/W	0000007F
01C0	05C0	09C0	0DC0	DSLER_RWC	Receive section and line layer event detection read only/ write clear	R/WC	**Note**
01C4	05C4	09C4	0DC4	DSLER_RC	Receive section and line layer event detection read clear	RC	**Note**
01C8	05C8	09C8	0DC8	DSLER_RCE	Receive section and line layer event detection read clear enable	R/W	03FF0FFF
01CC	05CC	09CC	0DCC	DSLER_M	Receive section and line layer event detection mask	R/W	03FF0FFF
01D0	05D0	09D0	0DD0	TSLER_RWC	Receive section and line layer event termination read only/ write clear	R/WC	**Note**
01D4	05D4	09D4	0DD4	TSLER_RC	Receive section and line layer event termination read clear	RC	**Note**
01D8	05D8	09D8	0DD8	TSLER_RCE	Receive section and line layer event termination read clear enable	R/W	00000FFF
01DC	05DC	09DC	0DDC	TSLER_M	Receive section and line layer event termination mask	R/W	00000FFF

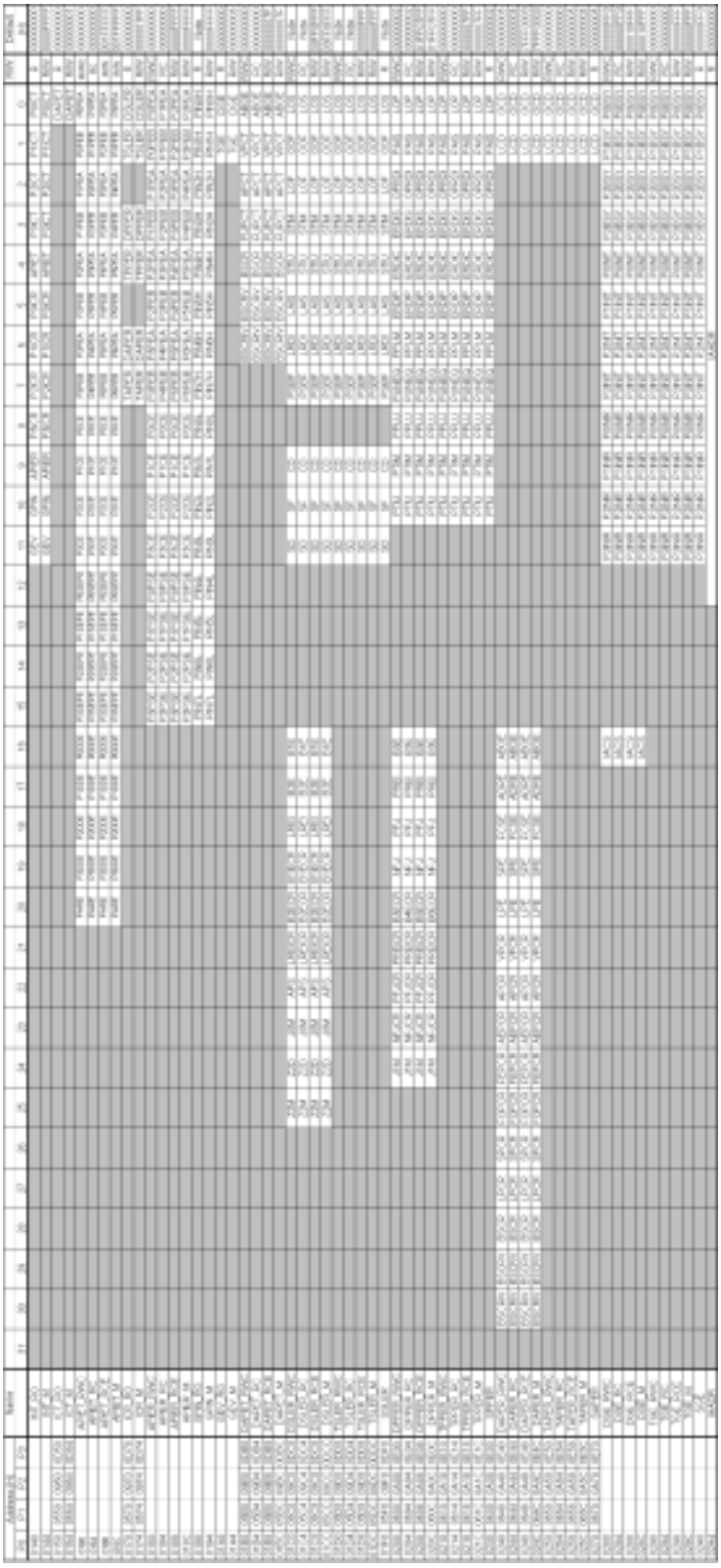
01F0	05F0	09F0	0DF0	SSLER	Receive section and line layer event status	R	**Note**
0200	0600	0A00	0E00	DPPER_RWC	Receive pointer and path layer event detection read only/ write clear	R/WC	00000002
0204	0604	0A04	0E04	DPPER_RC	Receive pointer and path layer event detection read clear	RC	00000002
0208	0608	0A08	0E08	DPPER_RCE	Receive pointer and path layer event detection read clear enable	R/W	01FF07FF
020C	060C	0A0C	0E0C	DPPER_M	Receive pointer and path layer event detection mask	R/W	01FF07FF
0210	0610	0A10	0E10	TPPER_RWC	Receive pointer and path layer event termination read only/ write clear	R/WC	00000000
0214	0614	0A14	0E14	TPPER_RC	Receive pointer and path layer event termination read clear	RC	00000000
0218	0618	0A18	0E18	TPPER_RCE	Receive pointer and path layer event termination read clear enable	R/W	000007FF
021C	061C	0A1C	0E1C	TPPER_M	Receive pointer and path layer event termination mask	R/W	000007FF
0230	0630	0A30	0E30	SPPER	Receive pointer and path layer event status	R	00000002
0240	0640	0A40	0E40	DAPER_RWC	Receive ATM/POS layer event detection read only/ write clear	R/WC	00000003
0244	0644	0A44	0E44	DAPER_RC	Receive ATM/POS layer event detection read clear	RC	00000003
0248	0648	0A48	0E48	DAPER_RCE	Receive ATM/POS layer event detection read clear enable	R/W	7FFF0003
024C	064C	0A4C	0E4C	DAPER_M	Receive ATM/POS layer event detection mask	R/W	7FFF0003
0250	0650	0A50	0E50	TAPER_RWC	Receive ATM/POS layer event termination read only/ write clear	R/WC	00000000
0254	0654	0A54	0E54	TAPER_RC	Receive ATM/POS layer event termination read clear	RC	00000000
0258	0658	0A58	0E58	TAPER_RCE	Receive ATM/POS layer event termination read clear enable	R/W	00000003
025C	065C	0A5C	0E5C	TAPER_M	Receive ATM/POS layer event termination mask	R/W	00000003
0270	0670	0A70	0E70	SAPER	Receive ATM/POS layer event status	R	00000003
0280				DGE_RWC	General event detection read only/ write clear	R/WC	00000FF0
0284				DGE_RC	General event detection read clear	RC	00000FF0
0288				DGE_RCE	General event detection read clear enable	R/W	00010FFF
028C				DGE_M	General event detection mask	R/W	00010FFF
0290				TGE_RWC	General event termination read only/ write clear	R/WC	00000000
0294				TGE_RC	General event termination read clear	RC	00000000
0298				TGE_RCE	General event termination read clear enable	R/W	00000FFF
029C				TGE_M	General event termination mask	R/W	00000FFF
02A0				SGE	General event status	R	00000FF0
02A4				IAADR	Illegal access address	R	00000000

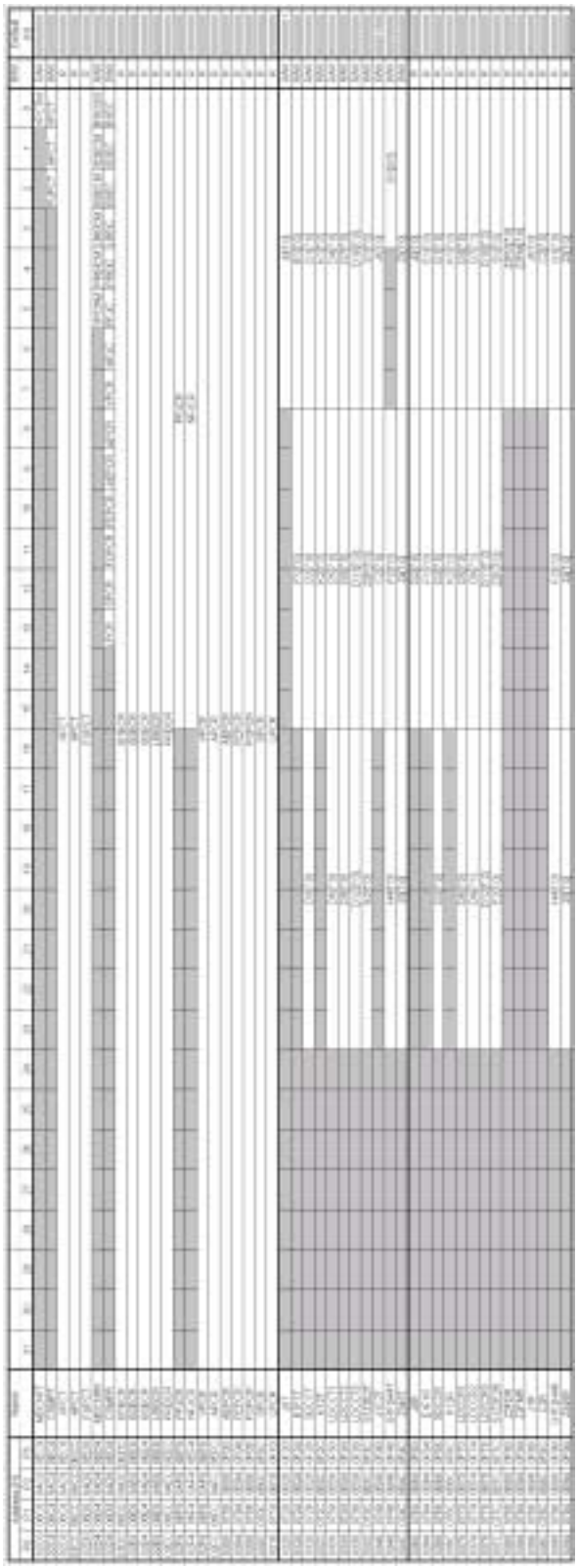
Address (H)				Name	Function	R/W	Default (H)
P0	P1	P2	P3				
02C0	06C0	0AC0	0EC0	MDCNTT	Transmit counter mode	R/W	00000000
02C4	06C4	0AC4	0EC4	CSMPT	Transmit counter sampling	R/W	00000000
02C8	06C8	0AC8	0EC8	VPCT	Transmit valid cell/packet counter load	R	00000000
02CC	06CC	0ACC	0ECC	APCT	Transmit abort packet counter load	R	00000000
02D0	06D0	0AD0	0ED0	FUPCT	Transmit FIFO underflow packet counter load	R	00000000
02D4	06D4	0AD4	0ED4	MDCNTR	Receive counter mode	R/W	00000000
02D8	06D8	0AD8	0ED8	CSMPR	Receive counter sampling	R/W	00000000
02DC	06DC	0ADC	0EDC	B1ECR	Receive B1 error counter load	R	00000000
02E0	06E0	0AE0	0EE0	B2ECR	Receive B2 error counter load	R	00000000
02E4	06E4	0AE4	0EE4	B3ECR	Receive B3 error counter load	R	00000000
02E8	06E8	0AE8	0EE8	LREICR	Receive Line REI counter load	R	00000000
02EC	06EC	0AEC	0EEC	PREICR	Receive Path REI counter load	R	00000000
02F0	06F0	0AF0	0EF0	PFJCR	Receive Positive Frequency Justification counter load	R	00000000
02F4	06F4	0AF4	0EF4	NFJCR	Receive Negative Frequency Justification counter load	R	00000000
02F8	06F8	0AF8	0EF8	VPCR	Receive valid cell/packet counter load	R	00000000
02FC	06FC	0AFC	0EFC	APCR	Receive idle cell and abort packet counter load	R	00000000
0300	0700	0B00	0F00	AEPCR	Receive HEC error correct cell and address error packet counter load	R	00000000
0304	0704	0B04	0F04	FEPCR	Receive HEC error drop cell and FCS error packet counter load	R	00000000
0308	0708	0B08	0F08	FOPCR	Receive FIFO overflow cell/packet counter load	R	00000000
030C	070C	0B0C	0F0C	SPCR	Receive short packet counter load	R	00000000
0310	0710	0B10	0F10	LPCR	Receive long packet counter load	R	00000000

Address (H)				Name	Function	R/W	Default (H)
P0	P1	P2	P3				
0320	0720	0B20	0F20	J0T	Transmit J0 insert	R/W	00000001
0324	0724	0B24	0F24	E1F1T	Transmit E1 and F1 insert	R/W	00000000
0328	0728	0B28	0F28	SDCCT	Transmit Section DCC insert	R/W	00000000
032C	072C	0B2C	0F2C	K12T	Transmit K1 and K2 insert	R/W	00000000
0330	0730	0B30	0F30	LDCCT1	Transmit Line DCC insert 1	R/W	00000000
0334	0734	0B34	0F34	LDCCT2	Transmit Line DCC insert 2	R/W	00000000
0338	0738	0B38	0F38	LDCCT3	Transmit Line DCC insert 3	R/W	00000000
033C	073C	0B3C	0F3C	S1Z2E2T	Transmit S1, 1st Z2 and E2 insert	R/W	00000000
0340	0740	0B40	0F40	J1C2T	Transmit J1 and C2 insert	R/W	00001300
0344	0744	0B44	0F44	G1F2H4T	Transmit G1, F2 and H4 insert	R/W	00000000
0348	0748	0B48	0F48	Z345T	Transmit Z3, Z4 and Z5 insert	R/W	00000000
0360	0760	0B60	0F60	J0R	Receive J0 drop	R	00000000
0364	0764	0B64	0F64	E1F1R	Receive E1 and F1 drop	R	00000000
0368	0768	0B68	0F68	SDCCR	Receive Section DCC drop	R	00000000
036C	076C	0B6C	0F6C	K12R	Receive K1 and K2 drop	R	00000000
0370	0770	0B70	0F70	LDCCR1	Receive Line DCC drop 1	R	00000000
0374	0774	0B74	0F74	LDCCR2	Receive Line DCC drop 2	R	00000000
0378	0778	0B78	0F78	LDCCR3	Receive Line DCC drop 3	R	00000000
037C	077C	0B7C	0F7C	S1Z2E2R	Receive S1, 1st Z2 and E2 drop	R	00000000
0380	0780	0B80	0F80	Z2FDR	Receive 1st Z2 drop 1	R	00000000
0384	0784	0B84	0F84	Z2FMR	Receive 1st Z2 drop 2	R	00000000
0388	0788	0B88	0F88	J1R	Receive J1 drop	R	00000000
038C	078C	0B8C	0F8C	C2R	Receive C2 drop	R	00000000
0390	0790	0B90	0F90	G1F2H4R	Receive G1, F2 and H4 drop	R	00000000
0394	0794	0B94	0F94	Z345R	Receive Z3, Z4 and Z5 drop	R	00000000

5.2 Register summary





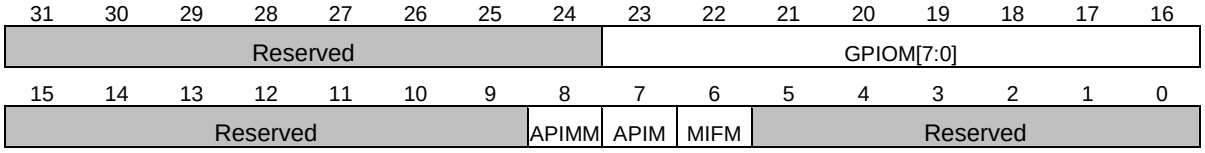


5.3 Function of Registers

(1) Device general mode register (MDDGEN) Common register

The MDDGEN register sets the modes related to general operation of uPD98413.

Register Name	Address	Access	Default
MDDGEN	0000H	R/W	00000080 H

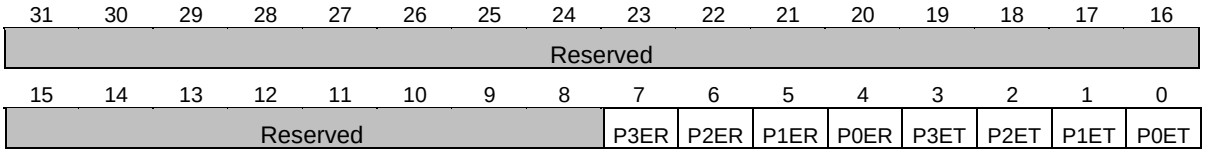


Bit	Field	Function	Default
D31-D24	Reserved	Set to 0.	0
D23-D16	GPIOM[7:0]	Selects the input or output of the general purpose I/O pins. 1: Output 0: Input	0
D15-D18	Reserved	Set to 0.	0
D8	APIMM	Selects the multi-PHY mode of ATM/POS interface. 1: Status polling 0: Direct status indication	0
D7	APIM	Selects the function of ATM/POS interface. 1: UTOPIA L3 0: POS-PHY L3	1
D6	MIFM	Selects the Big or Little endian mode of the management interface. 1: Big endian 0: Little endian	0
D5-D0	Reserved	Set to 0.	0

(2) Port enable register (PENB) Common register

The PENB register controls the enable of all ports.

Register Name	Address	Access	Default
PENB	0004H	R/W	00000000 H

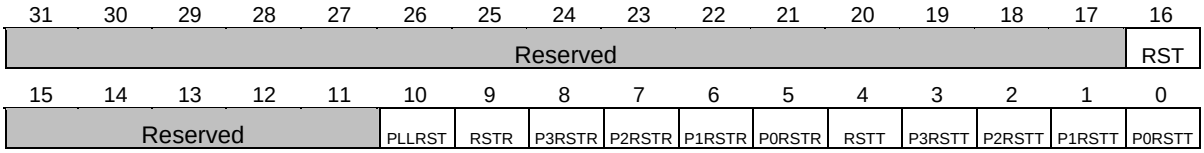


Bit	Field	Function	Default
D31-D8	Reserved	Set to 0.	0
D7	P3ER	1: Enables the receive function of the port3 of the μPD98413. 0: Disable	0
D6	P2ER	1: Enables the receive function of the port2 of the μPD98413. 0: Disable	0
D5	P1ER	1: Enables the receive function of the port1 of the μPD98413. 0: Disable	0
D4	P0ER	1: Enables the receive function of the port0 of the μPD98413. 0: Disable	0
D3	P3ET	1: Enables the transmit function of the port3 of the μPD98413. 0: Disable	0
D2	P2ET	1: Enables the transmit function of the port2 of the μPD98413. 0: Disable	0
D1	P1ET	1: Enables the transmit function of the port1 of the μPD98413. 0: Disable	0
D0	P0ET	1: Enables the transmit function of the port0 of the μPD98413. 0: Disable	0

(3) Software reset register (SRST) Common register

The SRST register initializes the μPD98413.

Register Name	Address	Access	Default
SRST	0008H	R/W	00000000 H



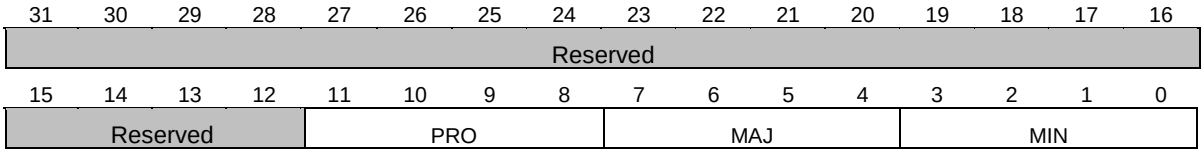
Bit	Field	Function	Default
D31-D17	Reserved	Set to 0.	0
D16	RST	1: Executes software reset of the all functions of the μPD98413. The uPD98413 is the reset condition while this bit is set to 1. Set 0 to this bit to return the normal operation. 0: Normal operation	0
D15-D11	Reserved	Set to 0.	0
D10	PLLRST	1: Executes software reset of the TxPLL function. This function is the reset condition while this bit is set to 1. Set 0 to this bit to return the normal operation. 0: Normal operation	0
D9	RSTR	1: Executes software reset of the receive function including DEMUX, CDR block and ATM/POS interface of all ports. This function is the reset condition while this bit is set to 1. Set 0 to this bit to return the normal operation. 0: Normal operation	0
D8	P3RSTR	1: Executes software reset of the receive function including DEMUX, CDR block of the port3. This function is the reset condition while this bit is set to 1. Set 0 to this bit to return the normal operation. 0: Normal operation	0
D7	P2RSTR	1: Executes software reset of the receive function including DEMUX, CDR block of the port2. This function is the reset condition while this bit is set to 1. Set 0 to this bit to return the normal operation. 0: Normal operation	0
D6	P1RSTR	1: Executes software reset of the receive function including DEMUX, CDR block of the port1. This function is the reset condition while this bit is set to 1. Set 0 to this bit to return the normal operation. 0: Normal operation	0
D5	P0RSTR	1: Executes software reset of the receive function of the port0. This function is the reset condition while this bit is set to 1. Set 0 to this bit to return the normal operation. 0: Normal operation	0
D4	RSTT	1: Executes software reset of the transmit function including MUX block and ATM/POS interface of all ports, excepted TxPLL function. This function is the reset condition while this bit is set to 1. Set 0 to this bit to return the normal operation. 0: Normal operation	0

D3	P3RSTT	1: Executes software reset of the transmit function of the port3 excepted TxPLL function. This function is the reset condition while this bit is set to 1. Set 0 to this bit to return the normal operation. 0: Normal operation	0
D2	P2RSTT	1: Executes software reset of the transmit function of the port2 excepted TxPLL function. This function is the reset condition while this bit is set to 1. Set 0 to this bit to return the normal operation. 0: Normal operation	0
D1	P1RSTT	1: Executes software reset of the transmit function of the port1 excepted TxPLL function. This function is the reset condition while this bit is set to 1. Set 0 to this bit to return the normal operation. 0: Normal operation	0
D0	P0RSTT	1: Executes software reset of the transmit function of the port0 excepted TxPLL function. This function is the reset condition while this bit is set to 1. Set 0 to this bit to return the normal operation. 0: Normal operation	0

(4) Version register (VER) Common register

The version of the μPD98413 is stored in the VER register.

Register Name	Address	Access	Default
VER	000CH	R	-



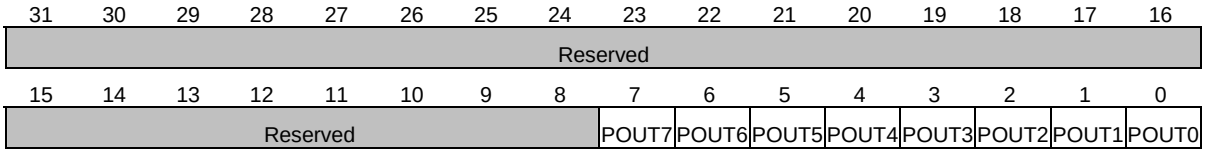
Bit	Field	Function	Default
D31-D12	Reserved		0
D11-D8	PRO	Product version.	-
D7-D4	MAJ	Major version.	-
D3-D0	MIN	Minor version.	-

Note that contact NEC for the current version.

(5) General-purpose output port control register (GPOUT) Common register

The GPOUT register changes the output level of each general-purpose output port. Each bit is available when each general-purpose I/O pin is output mode.

Register Name	Address	Access	Default
GPOUT	0010H	R/W	00000000 H

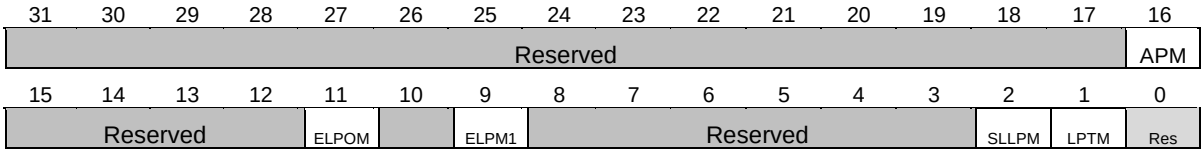


Bit	Field	Function	Default
D31-D8	Reserved	Set to 0.	0
D7	POUT7	1: Outputs a high level from the PIO7 pin. 0: Outputs a low level from the pin.	0
D6	POUT6	1: Outputs a high level from the PIO6 pin. 0: Outputs a low level from the pin.	0
D5	POUT5	1: Outputs a high level from the PIO5 pin. 0: Outputs a low level from the pin.	0
D4	POUT4	1: Outputs a high level from the PIO4 pin. 0: Outputs a low level from the pin.	0
D3	POUT3	1: Outputs a high level from the PIO3 pin. 0: Outputs a low level from the pin.	0
D2	POUT2	1: Outputs a high level from the PIO2 pin. 0: Outputs a low level from the pin.	0
D1	POUT1	1: Outputs a high level from the PIO1 pin. 0: Outputs a low level from the pin.	0
D0	POUT0	1: Outputs a high level from the PIO0 pin. 0: Outputs a low level from the pin.	0

(6) Port general mode register (MDPGEN)

The MDPGEN register sets the modes related to general operation per port.

Register Name	Address				Access	Default
	Port0:	Port1:	Port2:	Port3:		
MDPGEN	0020H	0420H	0820H	0C20H	R/W	00010000 H

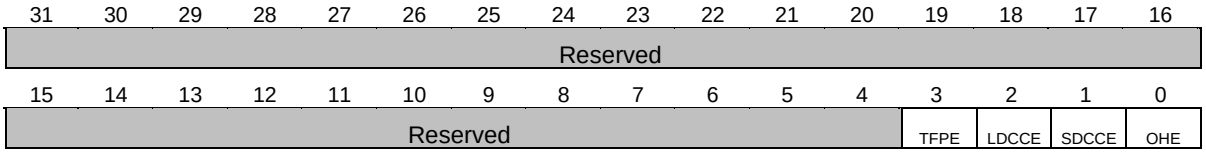


Bit	Field	Function	Default
D31-D17	Reserved	Set to 0.	0
D16	APM	Selects the function of the ATM/POS processor. 1: ATM 0: POS	1
D15-D12	Reserved	Set to 0.	0
D11	ELPOM	1: Outputs loop data to the line in equipment loopback mode. 0: Does not output loop data to the line in equipment loopback mode. Line AIS frame is transmitted to the line.	0
D10	Reserved	Set to 0.	0
D9	ELPM1	1: Sets Equipment loopback mode. 0: Normal operation	0
D8-D3	Reserved	Set to 0.	0
D2	SLLPM	1: Sets Line loopback mode of the SEDRDES block. 0: Normal operation	0
D1	LPTM	Sets the looptime mode using the receive clock for transmit. 1: Looptime 0: Normal	0
D0	Reserved	Set to 0.	0

(7) Transmit port general mode register (MDPT)

The MDPT register sets the modes related to general operation per transmit port.

Register Name	Address				Access	Default
	Port0:	Port1:	Port2:	Port3:		
MDPT	0024H	0424H	0824H	0C24H	R/W	00000000 H

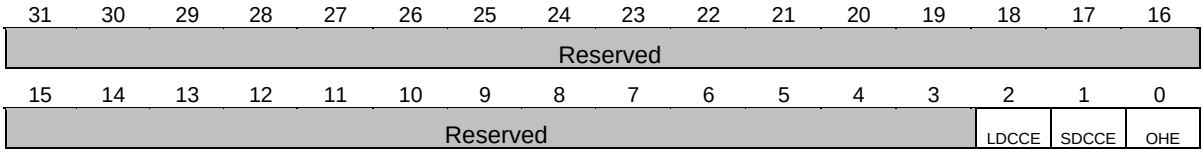


Bit	Field	Function	Default
D31-D3	Reserved	Set to 0.	0
D3	TFPE	Controls if the transmit SONET frame is aligned with TFPI signal when the active high transmit frame pulse is input. 1: Enable 0: Disable	0
D2	LDCCE	Controls the function of the Line DCC insert interface. 1: Enable 0: Disable	0
D1	SDCCE	Controls the function of the Section DCC insert interface. 1: Enable 0: Disable	0
D0	OHE	Controls the function of the OH insert interface. 1: Enable 0: Disable	0

(8) Receive port general mode register (MDPR)

The MDPR register sets the modes related to general operation per receive port.

Register Name	Address				Access	Default
	Port0:	Port1:	Port2:	Port3:		
MDPR	0028H	0428H	0828H	0C28H	R/W	00000000 H



Bit	Field	Function	Default
D31-D3	Reserved	Set to 0.	0
D2	LDCCE	Controls the function of the Line DCC extract interface. 1: Enable 0: Disable	0
D1	SDCCE	Controls the function of the Section DCC extract interface. 1: Enable 0: Disable	0
D0	OHE	Controls the function of the OH extract interface. 1: Enable 0: Disable	0

(9) Receive alarm port control register (RALM)

The RALM register sets the alarm output from each receive alarm port. Each RALM pin is high while at least one error set to 1 in the corresponding bits of the RALM register occur.

Register Name	Address				Access	Default
	Port0:	Port1:	Port2:	Port3:		
RALMA	002CH	042CH	082CH	0C2CH	R/W	00000000 H
RALMB	0030H	0430H	0830H	0C30H	R/W	00000000 H
RALMC	0034H	0434H	0834H	0C34H	R/W	00000000 H

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved								SD	SF	CDRUL	LCD	OCD	PTIU	PTIM	PPLU

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PUNEQ	PPLM	ERDIC	ERDIS	ERDIP	OPRDI	PAISD	LOP	PSBF	LRDI	LAIS	STIU	STIM	LOF	OOF	LOS

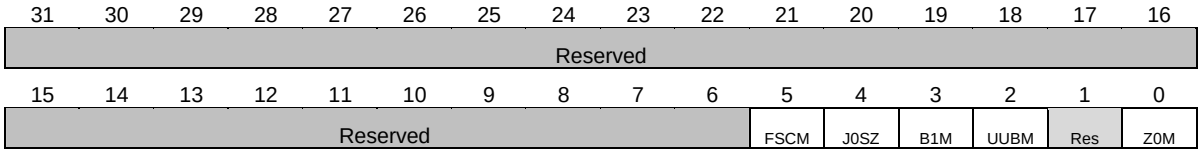
Bit	Field	Function	Default
D31-D24	Reserved	Set to 0.	0
D23	SD	1: SD event is indicated. 0: SD event is not indicated.	0
D22	SF	1: SF event is indicated. 0: SF event is not indicated.	0
D21	CDRUL	1: CDR unlock event is indicated. 0: CDR unlock event is not indicated.	0
D20	LCD	1: LCD event is indicated. 0: LCD event is not indicated.	0
D19	OCD	1: OCD event is indicated. 0: OCD event is not indicated.	0
D18	PTIU	1: Path TIU event is indicated. 0: Path TIU event is not indicated.	0
D17	PTIM	1: Path TIM event is indicated. 0: Path TIM event is not indicated.	0
D16	PPLU	1: Path PLU event is indicated. 0: Path PLU event is not indicated.	0
D15	PUNEQ	1: Path UNEQ event is indicated. 0: Path UNEQ event is not indicated.	0
D14	PPLM	1: Path PLM event is indicated. 0: Path PLM event is not indicated.	0
D13	ERDIC	1: Enhanced Path RDI Connectivity defect event is indicated. 0: Enhanced Path RDI Connectivity defect event is not indicated.	0
D12	ERDIS	1: Enhanced Path RDI Server defect event is indicated. 0: Enhanced Path RDI Server defect event is not indicated.	0
D11	ERDIP	1: Enhanced Path RDI Payload defect event is indicated. 0: Enhanced Path RDI Payload defect event is not indicated.	0
D10	OPRDI	1: One-bit Path RDI event is indicated. 0: One-bit Path RDI event is not indicated.	0
D9	PAISD	1: Path AIS event is indicated. 0: Path AIS event is not indicated.	0
D8	LOP	1: LOP event is indicated. 0: LOP event is not indicated.	0
D7	PSBF	1: PSBF event is indicated. 0: PSBF event is not indicated.	0
D6	LRDI	1: Line RDI event is indicated. 0: Line RDI event is not indicated.	0

D5	LAIS	1: Line AIS event is indicated.	0: Line AIS event is not indicated.	0
D4	STIU	1: Section TIU event is indicated.	0: Section TIU event is not indicated.	0
D3	STIM	1: Section TIM event is indicated.	0: Section TIM event is not indicated.	0
D2	LOF	1: LOF event is indicated.	0: LOF event is not indicated.	0
D1	OOF	1: OOF event is indicated.	0: OOF event is not indicated.	0
D0	LOS	1: LOS event is indicated.	0: LOS event is not indicated.	0

(10) Transmit SOH mode register (MDSOHT)

The MDSOHT register sets the modes related to transmit SOH operation.

Register Name	Address				Access	Default
	Port0:	Port1:	Port2:	Port3:		
MDSOHT	0040H	0440H	0840H	0C40H	R/W	00000000 H

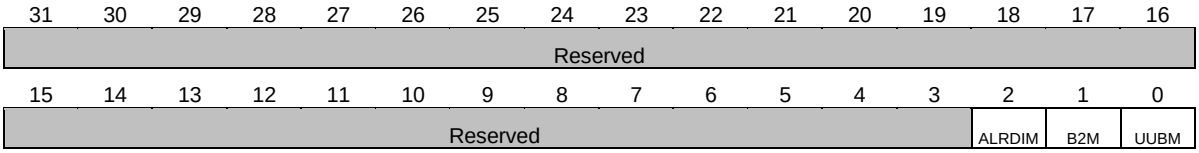


Bit	Field	Function	Default
D31-D6	Reserved	Set to 0.	0
D5	FSCM	Controls scramble of a frame. 1: Not scramble 0: Scramble	0
D4	J0SZ	Selects the size of the transmit J0 section trace message. 1: 16 bytes 0: 64 bytes	0
D3	B1M	Selects even or odd parity for BIP-8 (B1) parity operation of transmit section. 1: Odd parity 0: Even parity	0
D2	UUBM	Selects a value to be inserted in the unused byte area of the section overhead. 1: Inserts FFH. 0: Inserts 00H.	0
D1	Reserved	Set to 0.	0
D0	Z0M	Selects a value to be inserted in the 4th Z0 to 11th Z0 bytes of the transmit overhead. 1: Inserts AAH. 0: Sequentially inserts 5 to 36.	0

(11) Transmit LOH mode register (MDLOHT)

The MDLOHT register sets the modes related to transmit LOH operation.

Register Name	Address				Access	Default
	Port0:	Port1:	Port2:	Port3:		
MDLOHT	0044H	0444H	0844H	0C44H	R/W	00000000 H

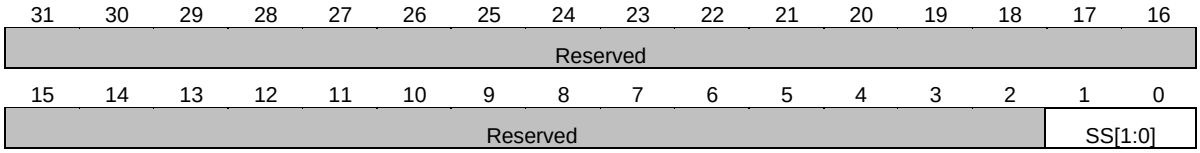


Bit	Field	Function	Default
D31-D3	Reserved	Set to 0.	0
D2	ALRDIM	Controls the automatic loopback transmission function of Line RDI. 1: Not automatic loopback 0: Automatic loopback	0
D1	B2M	Selects even or odd parity for BIP-96 (B2) parity operation of transmit line. 1: Odd parity 0: Even parity	0
D0	UUBM	Selects a value to be inserted in the unused byte area of the transmit overhead. 1: Inserts FFH. 0: Inserts 00H.	0

(12) Transmit pointer mode register (MDPTRT)

The MDPTRT register sets the modes related to transmit pointer operation.

Register Name	Address				Access	Default
	Port0:	Port1:	Port2:	Port3:		
MDPTRT	0048H	0448H	0848H	0C48H	R/W	00000000 H

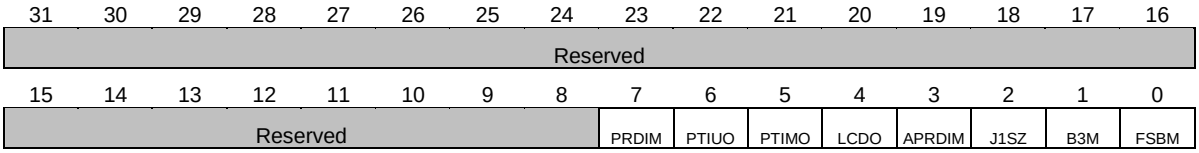


Bit	Field	Function	Default
D31-D2	Reserved	Set to 0.	0
D1-D0	SS[1:0]	Sets the contents of the SS bits of the transmit pointer.	0

(13) Transmit POH mode register (MDPOHT)

The MDPOHT register sets the modes related to transmit POH operation.

Register Name	Address				Access	Default
	Port0:	Port1:	Port2:	Port3:		
MDPOHT	004CH	044CH	084CH	0C4CH	R/W	00000000 H

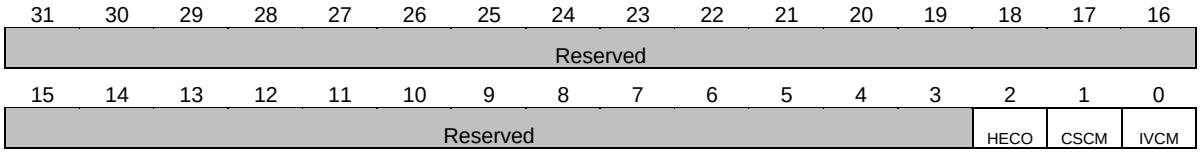


Bit	Field	Function	Default
D31-D8	Reserved	Set to 0.	0
D7	PRDIM	Selects the Path RDI function. 1: Enhanced Path RDI 0: One-bit Path RDI	0
D6	PTIUO	Specifies whether Path TIU detection is included in the condition of automatic loopback transmission of Enhanced Path RDI connectivity. 1: Includes Path TIU. 0: Does not include Path TIU.	0
D5	PTIMO	Specifies whether Path TIM detection is included in the condition of automatic loopback transmission of Enhanced Path RDI connectivity. 1: Includes Path TIM. 0: Does not include Path TIM.	0
D4	LCDO	Specifies whether LCD detection is included in the condition of automatic loopback transmission of Path RDI. 1: Includes LCD. 0: Does not include LCD.	0
D3	APRDIM	Controls the automatic loopback transmission function of Path RDI. 1: Not automatic loopback 0: Automatic loopback	0
D2	J1SZ	Selects the size of the transmit J1 path trace message. 1: 16 bytes 0: 64 bytes	0
D1	B3M	Selects even or odd parity for BIP-8 (B3) parity operation of transmit path. 1: Odd parity 0: Even parity	0
D0	FSBM	Selects a value to be inserted in the Fixed Stuff byte area of the transmit frame. 1: Inserts 00H. 0: Inserts FFH.	0

(14) Transmit ATM mode register (MDATMT)

The MDATMT register sets the modes related to transmit ATM operation.

Register Name	Address				Access	Default
	Port0:	Port1:	Port2:	Port3:		
MDATMT	0050H	0450H	0850H	0C50H	R/W	00000000 H

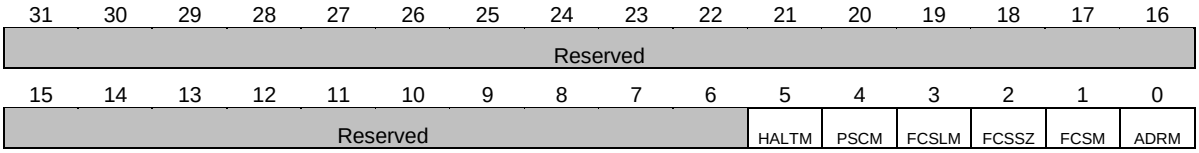


Bit	Field	Function	Default
D31-D3	Reserved	Set to 0.	0
D2	HECO	Controls the HEC insertion to a transmit cell. 1: Disabled 0: Enabled	0
D1	CSCM	Controls scramble of a cell. 1: Not scramble 0: Scramble	0
D0	IVCM	Selects the format of an invalid cell to be transmitted. 1: Unassigned cell 0: Idle cell	0

(15) Transmit POS Mode register (MDPOST)

The MDPOST register sets the modes related to transmit POS operation.

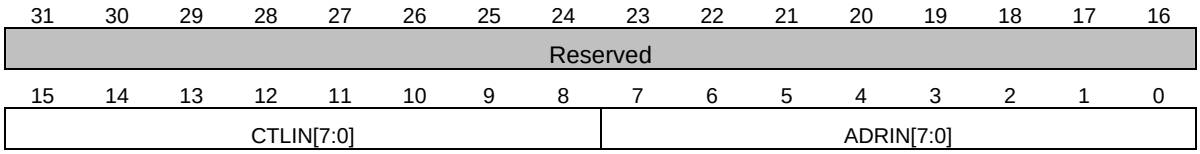
Register Name	Address				Access	Default
	Port0:	Port1:	Port2:	Port3:		
MDPOST	0054H	0454H	0854H	0C54H	R/W	00000000 H



Bit	Field	Function	Default
D31-D6	Reserved	Set to 0.	0
D5	HALTM	Sets the HALT mode. 1: HALT mode 0: Normal operation	0
D4	PSCM	Controls scramble of a packet. 1: Not scramble 0: Scramble	0
D3	FCSLM	Selects the FCS calculation order whether it is calculated from the LSB or MSB of the transmit packet. 1: MSB first 0: LSB first	0
D2	FCSSZ	Selects the transmit FCS length. 1: 16 bits 0: 32 bits	0
D1	FCSM	Controls the insertion of FCS field in the transmit packet. 1: Disabled. FCS field are not inserted in the transmit packet. 0: Inserts FCS field.	0
D0	ADRM	Controls the insertion of Address and Control fields in the transmit packet. 1: Disabled. Address and Control fields are not inserted in the transmit packet. 0: Inserts Address and Control fields.	0

(16) Transmit POS Address and Control register (PACT)

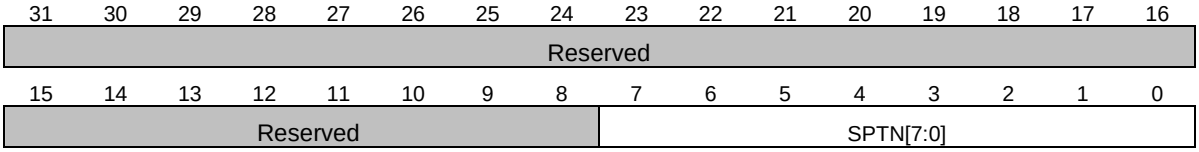
Register Name	Address				Access	Default
	Port0:	Port1:	Port2:	Port3:		
PACT	0058H	0458H	0858H	0C58H	R/W	000003FF H



Bit	Field	Function	Default
D31-D16	Reserved	Set to 0.	0
D15-D8	CTLIN[7:0]	Sets the Control value inserted into the transmit packet.	03H
D7-D0	ADRIN[7:0]	Sets the Address value inserted into the transmit packet.	FFH

(17) Transmit HALT pattern register (HPTNT)

Register Name	Address				Access	Default
	Port0:	Port1:	Port2:	Port3:		
HPTNT	005CH	045CH	085CH	0C5CH	R/W	00000000 H

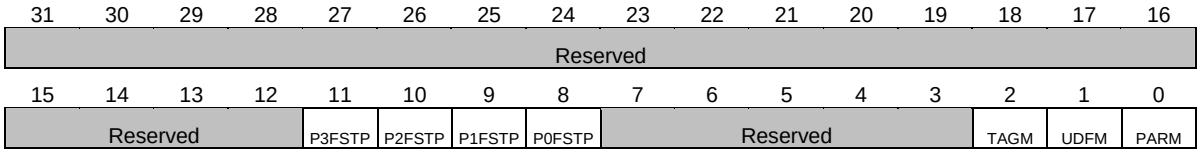


Bit	Field	Function	Default
D31-D8	Reserved	Set to 0.	0
D7-D0	SPTN[7:0]	Sets the suspended pattern during the packet transmission. Set the value except “5D”, “5E”, “7D”.	0H

(18) Transmit ATM/POS interface mode register (MDAPIT) Common register

The MDAPIT register sets the mode related to the transmit ATM/POS interface block.

Register Name	Address	Access	Default
MDAPIT	0060H	R/W	00000000 H

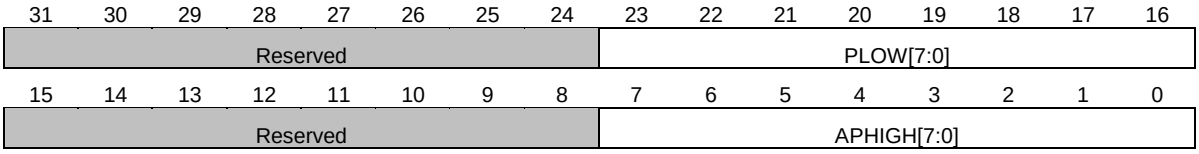


Bit	Field	Function	Default
D31-D12	Reserved	Set to 0.	0
D11	P3FSTP	Stops the data output from the transmit FIFO of port3 to port 0. 1: Stop 0: Normal operation	0
D10	P2FSTP	Stops the data output from the transmit FIFO of port3 to port 0. 1: Stop 0: Normal operation	0
D9	P1FSTP	Stops the data output from the transmit FIFO of port3 to port 0. 1: Stop 0: Normal operation	0
D8	P0FSTP	Stops the data output from the transmit FIFO of port3 to port 0. 1: Stop 0: Normal operation	0
D7-D3	Reserved	Set to 0.	0
D2	TAGM	Selects whether TAG is used in the format of the transmit cell to be transferred via the ATM interface. 1: Used 0: Not used	0
D1	UDFM	Selects whether UDF is used in the format of the transmit cell to be transferred via the ATM interface. 1: Used 0: Not used	0
D0	PARM	Selects even or odd parity for the parity operation of the transmit ATM/POS interface. 1: Even 0: Odd	0

(19) Transmit FIFO threshold register1 (FTHT1)

The FTHT1 register sets the threshold of the transmit FIFO.

Register Name	Address				Access	Default
	Port0:	Port1:	Port2:	Port3:		
FTHT1	0064H	0464H	0864H	0C64H	R/W	0010000D

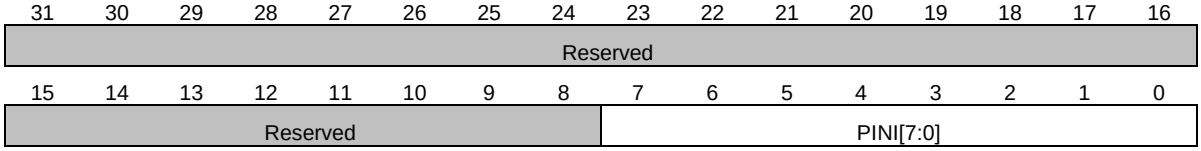


Bit	Field	Function	Default
D31-D24	Reserved	Set to 0.	0
D23-D16	PLOW[7:0]	Sets the low threshold which the TPA signal is asserted when the number of words (32-bit width) for the transmit FIFO space is higher than this field.	10 H
D15-D8	Reserved	Set to 0.	0
D7-D0	APHIGH[7:0]	ATM mode: Sets the high threshold which the TCLAV signal is deasserted when the number of words (32-bit width) for the transmit FIFO space is lower than this field. POS mode: Sets the high threshold which the TPA signal is deasserted when the number of words (32-bit width) for the transmit FIFO space is lower than this field.	0D H

(20) Transmit FIFO threshold register2 (FTHT2)

The FTHT2 register sets the threshold of the transmit FIFO.

Register Name	Address				Access	Default
	Port0:	Port1:	Port2:	Port3:		
FTHT2	0068 H	0468 H	0868 H	0C68 H	R/W	00000010 H

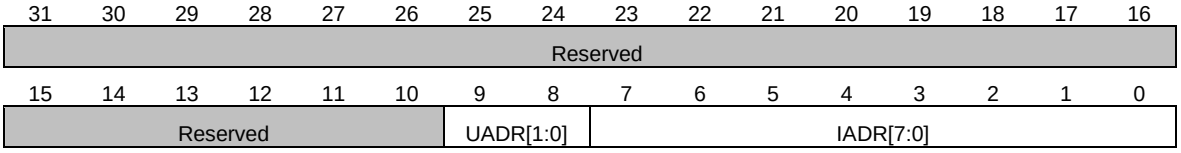


Bit	Field	Function	Default
D31-D9	Reserved	Set to 0.	0
D8-D0	PINI[7:0]	Sets the initial number of bytes when uPD98413 start to transmit the POS packet. The uPD98413 start to transmit the data when either the number of words (32-bit width) stored in the transmit FIFO exceeds this field or a complete packet is stored in the FIFO.	10 H

(21) Transmit port address register (PTADRT)

The PTADRT register sets the transmit port address.

Register Name	Address	Access	Default
PTADRT	Port0: 006C H Port1: 046C H Port2: 086C H Port3: 0C6C H	R/W	00000000 H 00010001 H 00020002 H 00030003 H

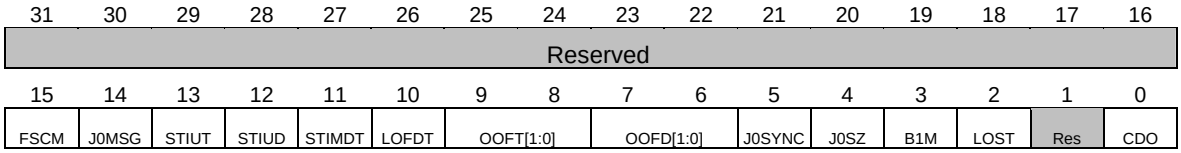


Bit	Field	Function	Default
D31-D10	Reserved	Set to 0.	0
D9-D8	UADR [1:0]	UTOPIA mode: Sets the transmit port address for UTOPIA. POS-PHY mode: Sets the polling address for POS-PHY.	Port0: 0 Port1: 1 Port2: 2 Port3: 3
D7-D0	IADR [7:0]	Sets the transmit in-band port address.	Port0: 0 Port1: 1 Port2: 2 Port3: 3

(22) Receive SOH mode register (MDSOHR)

The MDSOHR register sets the modes related to receive SOH operation.

Register Name	Address				Access	Default
	Port0:	Port1:	Port2:	Port3:		
MDSOHR	0070 H	0470 H	0870 H	0C70 H	R/W	00007D40 H

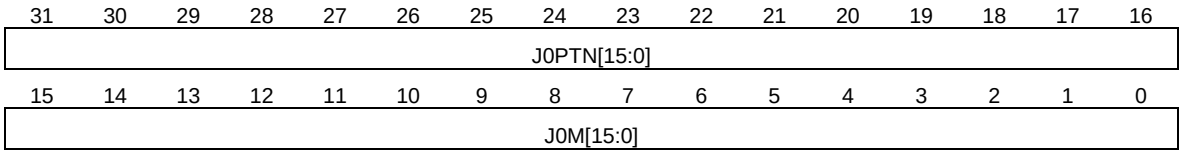


Bit	Field	Function	Default
D31-D16	Reserved	Set to 0.	0
D15	FSCM	Controls descramble of a frame. 1: Not descramble 0: Descramble	0
D14	J0MSG	Changes "n" of the received trace message drop condition. 1: n = 5 0: n = 3	1
D13	STIUT	Changes "n" of the Section TIU termination condition. 1: n = 5 0: n = 3	1
D12	STIUD	Changes "n" of the Section TIU detection condition. 1: n = 8 0: n = 5	1
D11	STIMDT	Changes "n" of the Section TIM detection/termination condition. 1: n = 5 0: n = 3	1
D10	LOFDT	Changes the LOF detection/termination condition. 1: LOF status is detected if OOF status lasts for 3 ms. LOF status is terminated if the μPD98413 is not in the OOF status for 3ms. 0: LOF status is detected at the same time as OOF detection. LOF status is terminated at the same time as OOF termination.	1
D9-D8	OOFT[1:0]	Changes the number of backward protection stages δ for OOF detection. The OOF status is cleared if the frame synchronization pattern has been detected in the receive cell stream δ times in a row. 11: 4 10: 3 01: 2 00: Reserved	01
D7-D6	OOFD[1:0]	Changes the number of forward protection stages α for OOF detection. The μPD98413 is placed in the OOF status if it cannot detect a frame synchronization pattern in the receive data stream α times in a row. 11: 6 10: 5 01: 4 00: 3	01
D5	J0SYNC	Specifies whether the first pattern of a message or end pattern is selected as a synchronization pattern when the J0 section trace message is received. 1: Selects the first word of the message as a synchronization pattern. 0: Selects the last word of the message as a synchronization pattern.	0
D4	J0SZ	Selects the size of the receive J0 section trace message. 1: 16 bytes 0: 64 bytes	0
D3	B1M	Selects even or odd parity for BIP-8 (B1) parity operation of receive section. 1: Odd parity 0: Even parity	0

D2	LOST	Selects LOS termination condition. 1: Bellcore mode 0: ANSI mode	0
D1	Reserved	Set to 0.	0
D0	CDO	Includes low level of the CD pin input in the LOS detection condition. 1: LOS status if the CD pin input goes low. 0: Not LOS status even if the CD pin input goes low.	0

(23) J0 trace message synchronous pattern register (J0PTN)

Register Name	Address				Access	Default
	Port0:	Port1:	Port2:	Port3:		
J0PTN	0074 H	0474 H	0874 H	0C74 H	R/W	0D0A0000 H

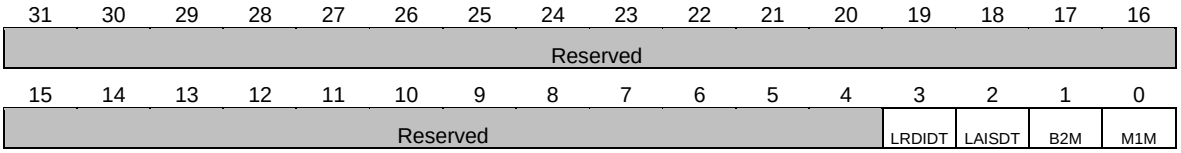


Bit	Field	Function	Default
D31-D16	J0PTN[15:0]	Sets the synchronous pattern of J0 trace message.	0D0A H
D15-D0	J0M[15:0]	Sets the mask value of the synchronous pattern. When the bits of this field is set to 1, the corresponding bits of synchronous pattern are masked	0000 H

(24) Receive LOH mode register (MDLOHR)

The MDLOHR register sets the modes related to receive LOH operation.

Register Name	Address				Access	Default
	Port0:	Port1:	Port2:	Port3:		
MDLOHR	0078 H	0478 H	0878 H	0C78 H	R/W	0000000C H

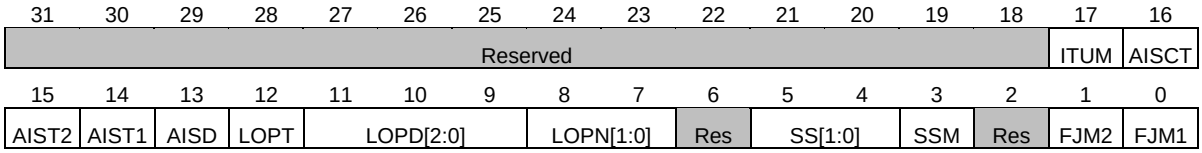


Bit	Field	Function	Default
D31-D4	Reserved	Set to 0.	0
D3	LRDIDT	Changes "n" of the Line RDI detection condition Line RDI is detected when a frame with K2 byte (bits 6 to 8) being "110" has been received n times." 1: n = 5 0: n = 3	1
D2	LAISDT	Changes "n" of the Line AIS detection condition Line AIS is detected when a frame with the K2 byte (bits 6 to 8) set to "111" has been received n times." 1: n = 5 0: n = 3	1
D1	B2M	Selects even or odd parity for BIP-96 (B2) parity operation of receive line. 1: Odd parity 0: Even parity	0
D0	M1M	Controls if ignored of the bit1 in the received M1 bytes when detect the Line REI. 1: Ignored 0: Not ignored	0

(25) Receive pointer mode register (MDPTRR)

The MDPTRR register sets the modes related to receive pointer operation.

Register Name	Address				Access	Default
	Port0:	Port1:	Port2:	Port3:		
MDPTRR	007C H	047C H	087C H	0C7C H	R/W	00002020 H



Bit	Field	Function	Default
D31-D18	Reserved	Set to 0.	0
D17	ITUM	Sets the status transition mode. 1: ITU-T mode 0: Bellcore mode	0
D16	AISCT	Selects the AISC termination condition 1: Corresponding Conc STS is 3 x conc_ind, or 1st STS is NDF_enable and all Conc STS is conc_ind. 0: Corresponding Conc STS is 3 x conc_ind.	0
D15	AIST2	Selects the AIS termination condition by NDF_enable whether include conc_ind of all H1#2 and H2#2 to H1#12 and H2#12 Concatenation Interpretation 1: Not include 0: Include	0
D14	AIST1	Selects the AIS termination condition by 3 x norm_point whether Include 3×conc_ind of all H1#2 and H2#2 to H1#12 and H2#12 Concatenation Interpretation 1: Not include 0: Include	0
D13	AISD	Selects the AIS detection condition whether include 3xAIS_ind of all H1#2 and H2#2 to H1#12 and H2#12 Concatenation Interpretation 1: Not include 0: include	1
D12	LOPT	Selects the LOP termination condition whether include 3×conc_ind of all H1#2 and H2#2 to H1#12 and H2#12 Concatenation Interpretation. 1: Not include 0: Include	0

D11-D9	LOPD[2:0]	These bits can be changed condition of transition to LOP status. 000: Not detect 3×norm_point or 3×conc_ind of 1 or more H1#2 and H2#2 to H1#12 and H2#12 Concatenation Interpretation in N frame (but not include AIS detection). 001: Not detect 3 consecutive norm_point and conc_ind of all H1#2 and H2#2 to H1#12 and H2#12 Concatenation Interpretation in N frame (but not include AIS detection). 010: Not detect 3×norm_point in N frame (but not include AIS detection). 011: Detect N×Inv_point of H1#1 and H2#1 (but not include 3 x norm_point) or N×Inv_point of 1 or more H1#2 and H2#2 to H1#12 and H2#12 Concatenation Interpretation. 100: Detect N×Inv_point of H1#1 and H2#1 (but not include 3 x norm_point). Other than above: Reserved	000
D8-D7	LOPN[1:0]	Sets the number of protection stages n for LOP detection in status transition of pointer processing. 11: Reserved 10: n = 10 01: n = 9 00: n = 8	00
D6	Reserved	Set to 0.	0
D5-D4	SS[1:0]	Sets the expected value of the SS bits to be verified if the SS bits are checked when the receive pointer action is identified (when SSM = 1).	10
D3	SSM	Selects whether the SS bits are checked when the receive pointer action is identified. 1: Checked 0: Don't care	0
D2	Reserved	Set to 0.	0
D1	FJM2	Select the incr_ind and decr_ind indication condition 1: Mach of 8 bits or more of the 10 bits I-bits and D-bits to either the increment and decrement indication. 0: incr_ind : 3 or more I-bits are inverted and 3 or more D-bits are not inverted decr_ind : 3 or more D-bits are inverted and 3 or more I-bits are not inverted	0
D0	FJM1	Select the incr_ind and decr_ind indication condition, which include NDF_enable, incr_ind and decr_ind is not receive at least 3 flames. 1: Not include NDF_enable, incr_ind and decr_ind is not receive at least 3 flames. 0: Include NDF_enable, incr_ind and decr_ind is not receive at least 3 flames.	0

(26) Receive POH mode register (MDPOHR)

The MDPOHR register sets the modes related to receive POH operation.

Register Name	Address				Access	Default
	Port0:	Port1:	Port2:	Port3:		
MDPOHR	0080 H	0480 H	0880 H	0C80 H	R/W	001337F0 H

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved								C2EX[7:0]							

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved		PPLM02	PPLM01	PRDIM	J1MSG	PTIUT	PTIUD	PTIMDT	PPLUT	PPLMDT	PRDIDT[1:0]		J1SYNC	J1SZ	B3M

Bit	Field	Function	Default
D31-D24	Reserved	Set to 0.	0
D23-D16	C2EX[7:0]	Sets the expected value of the receive C2 byte (Signal Label).	13H
D15-D14	Reserved	Set to 0.	0
D13	PPLM02	1: Except the value by setting the C2EX[7:0] for detection Path PLM. 0: Not Except.	1
D12	PPLM01	1: Except the value “01h” for detection Path PLM. 0: Not Expect.	1
D11	PRDIM	Selects the Path RDI function. 1: Enhanced Path RDI 0: One-bit Path RDI	0
D10	J1MSG	Changes "n" of the received trace message drop condition. 1: n = 5 0: n = 3	1
D9	PTIUT	Changes "n" of the Path TIU termination condition. 1: n = 5 0: n = 3	1
D8	PTIUD	Changes "n" of the Path TIU detection condition. 1: n = 8 0: n = 5	1
D7	PTIMDT	Changes "n" of the Path TIM detection/termination condition. 1: n = 5 0: n = 3	1
D6	PPLUT	Changes "n" of the Path PLU clearing and received C2 byte drop condition. 1: n = 5 0: n = 3	1
D5	PPLMDT	Changes "n" of the Path PLM and UNEQ detection/clearing condition. 1: n = 5 0: n = 3	1
D4-D3	PRDIDT[1:0]	Changes "n" of the Path RDI detection condition "Path RDI is detected when a frame with the G1 byte set to "1" has been received n times." 11: Reserved 10: n = 10 01: n = 5 00: n = 3	10
D2	J1SYNC	Specifies whether the first pattern of a message or end pattern is selected as a synchronization pattern when the J1 path trace message is received. 1: Selects the first word of the message as a synchronization pattern. 0: Selects the last word of the message as a synchronization pattern.	0

D1	J1SZ	Selects the size of the receive J1 path trace message. 1: 16 bytes 0: 64 bytes	0
D0	B3M	Selects even or odd parity for BIP-8 (B3) parity operation of receive line. 1: Odd parity 0: Even parity	0

(27) J1 trace message synchronous pattern register (J1PTN)

Register Name	Address				Access	Default
	Port0:	Port1:	Port2:	Port3:		
J1PTN	0084 H	0484 H	0884 H	0C84 H	R/W	0D0A0000H

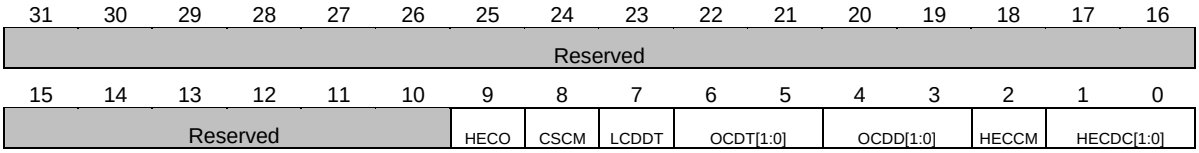
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
J1PTN[15:0]															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
J1M[15:0]															

Bit	Field	Function	Default
D31-D16	J1PTN[15:0]	Sets the synchronous pattern of J1 trace message.	0D0AH
D15-D0	J1M[15:0]	Sets the mask value of the synchronous pattern. When the bits of this field is set to 1, the corresponding bits of synchronous pattern are masked	0000H

(28) Receive ATM mode register (MDATMR)

The MDATMR register sets the modes related to receive ATM operation.

Register Name	Address				Access	Default
	Port0:	Port1:	Port2:	Port3:		
MDATMR	0088 H	0488 H	0888 H	0C88 H	R/W	000000A8 H

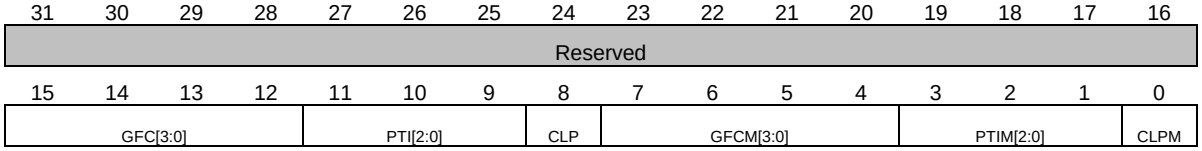


Bit	Field	Function	Default
D31-D10	Reserved	Set to 0.	0
D9	HECO	Controls the HEC verification of a receive cell. 1: Disabled 0: Enabled	0
D8	CSCM	Controls descramble of a cell. 1: Not descramble 0: Descramble	0
D7	LCDDT	Changes the LCD detection and termination condition. 1: LCD status is detected if OCD status lasts for 4 ms. LCD status is terminated if cell synchronization status lasts for 4ms. 0: LCD status is detected at the same time as OCD detection. LCD status is terminated at the same time as OCD termination.	1
D6-D5	OCDT[1:0]	Changes the number of backward protection stages δ for OCD detection. The OCD status is cleared if the correct HEC has been detected in the receive cell stream δ+1 times in a row. 11: 8 10: 7 01: 6 00: 5	01
D4-D3	OCDD[1:0]	Sets the number of forward protection stages α for OCD detection. The μPD98413 is placed in the OCD status if it cannot detect the correct HEC in the receive cell stream α times in a row. 11: 9 10: 8 01: 7 00: 6	01
D2	HECCM	Controls 1-bit error correction of a header by HEC verification. 1: Does not correct bit error and drops cell. 0: Corrects bit error and passes cell.	0
D1-D0	HECDC[1:0]	Changes the number of recovery stages ε from "detection mode" to "correction mode" in HEC verification status transition. 11: Setting prohibited 10: 4 01: 2 00: 1	00

(29) Drop cell header pattern register (DCHP)

The DCHP register sets the header pattern of a receive cell to be discarded as an invalid cell. By default, the idle cells are dropped.

Register Name	Address				Access	Default
	Port0:	Port1:	Port2:	Port3:		
DCHP	008C H	048C H	088C H	0C8C H	R/W	00000100 H

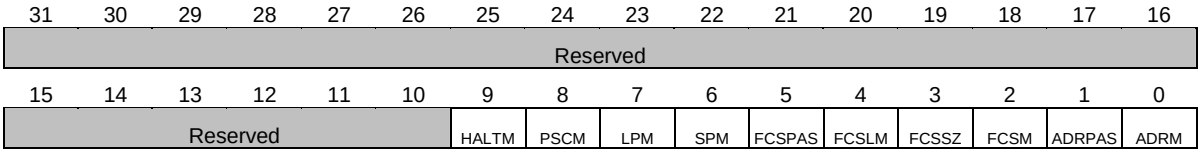


Bit	Field	Function	Default
D31-D16	Reserved	Set to 0.	0
D15-D12	GFC[3:0]	A receive cell with VPI/VCI being all 0 is verified with the pattern that is the cell header area other than the VPI/VCI area set in this area. The cell that coincides with the pattern in this area is not stored to the receive FIFO but dropped. However, the bit that is masked by the low-order eight bits of this area is not masked but treated as Don't Care.	0000
D11-D9	PTI[2:0]		000
D8	CLP		1
D7-D4	GFCM[3:0]	This field masks the high-order eight bits. The bit of the cell header that is set to 1 in this area is not verified with the bit setting of the high-order eight bits.	0000
D3-D1	PTIM[2:0]		000
D0	CLPM		0

(30) Receive POS Mode register (MDPOSR)

The MDPOSR register sets the modes related to receive POS operation.

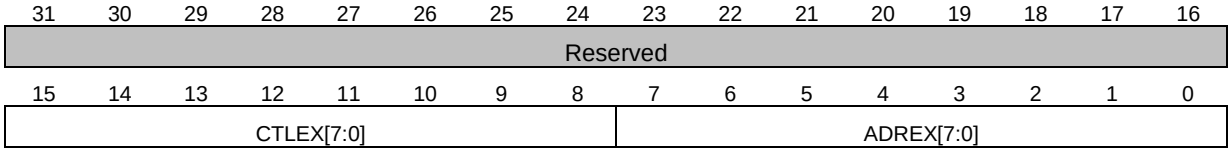
Register Name	Address				Access	Default
	Port0:	Port1:	Port2:	Port3:		
MDPOSR	0090 H	0490 H	0890 H	0C90 H	R/W	00000000 H



Bit	Field	Function	Default
D31-D10	Reserved	Set to 0.	0
D9	HALTM	Sets the HALT mode. 1: HALT mode 0: Normal operation	0
D8	PSCM	Controls descramble of a packet. 1: Not descramble 0: Descramble	0
D7	LPM	Controls the check function of receive long size packet. 1: Disabled. 0: Checks long size packet.	0
D6	SPM	Controls the check function of receive short size packet. 1: Disabled. 0: Checks short size packet.	0
D5	FCSPAS	Selects if the receive FCS is passed through the POS interface or stripped. 1: FCS is passed. 0: FCS is stripped.	0
D4	FCSLM	Selects the FCS calculation order whether it is calculated from the LSB or MSB of the receive packet. 1: MSB first 0: LSB first	0
D3	FCSSZ	Selects the receive FCS length. 1: 16 bits 0: 32 bits	0
D2	FCSM	Controls the check function of FCS field in the receive packet. 1: Disabled. FCS field are not checked in the receive packet. 0: Checks FCS field. If FCS error occurs, the error is indicated by RERR signal.	0
D1	ADRPAS	Selects if the receive Address and Control fields is passed through the POS interface or stripped when the Address and Control check is enabled and no error. 1: Address and Control fields is passed. 0: Address and Control fields is stripped.	0
D0	ADRM	Controls the check function of Address and Control fields in the receive packet. 1: Disabled. Address and Control fields are not checked in the receive packet. 0: Checks Address and Control fields. If Address and Control errors occur, the packet is dropped and the error is indicated by interrupt.	0

(31) Receive POS Address and Control register (PACR)

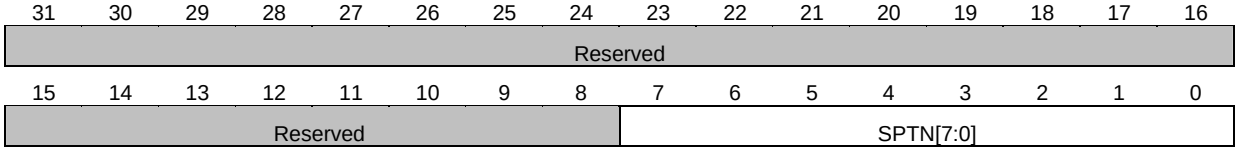
Register Name	Address				Access	Default
	Port0:	Port1:	Port2:	Port3:		
PACR	0094 H	0494 H	0894 H	0C94 H	R/W	000003FF H



Bit	Field	Function	Default
D31-D16	Reserved	Set to 0.	0
D15-D8	CTLEX[7:0]	Sets the expected value of the receive Control byte.	03H
D7-D0	ADREX[7:0]	Sets the expected value of the receive Address byte.	FFH

(32) Receive HALT pattern register (HPTNR)

Register Name	Address				Access	Default
	Port0:	Port1:	Port2:	Port3:		
HPTNR	0098 H	0498 H	0898 H	0C98 H	R/W	00000000 H

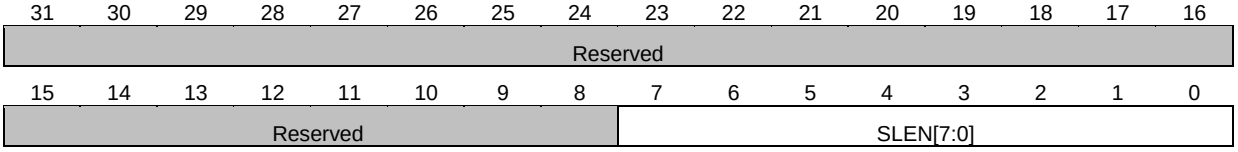


Bit	Field	Function	Default
D31-D8	Reserved	Set to 0.	0
D7-D0	SPTN[7:0]	Sets the expected value of the suspended pattern.	00 H

(33) Receive packet length register 1 (PLENR1)

The PLENR1 register sets the receive packet length.

Register Name	Address				Access	Default
	Port0:	Port1:	Port2:	Port3:		
PLENR1	009C H	049C H	089C H	0C9C H	R/W	00000000 H

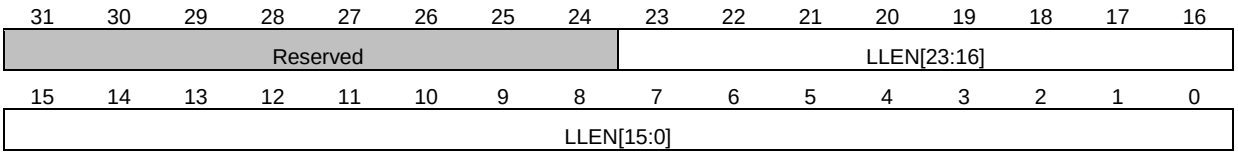


Bit	Field	Function	Default
D31-D8	Reserved	Set to 0.	0
D7-D0	SLEN[7:0]	Sets the minimum packet length in byte units. Packets smaller than this length are indicated with short packet error. This length is defined as the number of payload bytes received POS packet.	0H

(34) Receive packet length register 2 (PLENR2)

The PLENR2 register sets the receive packet length.

Register Name	Address				Access	Default
	Port0:	Port1:	Port2:	Port3:		
PLENR2	00A0 H	04A0 H	08A0 H	0CA0 H	R/W	000005FC H

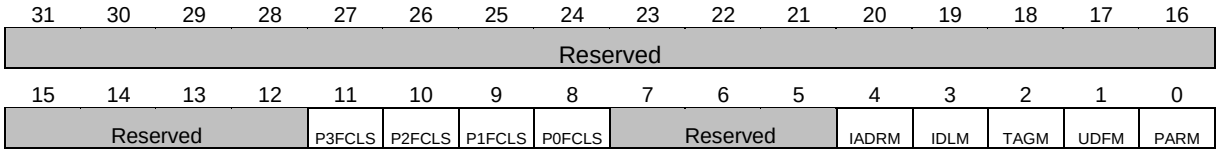


Bit	Field	Function	Default
D31-D24	Reserved	Set to 0.	0
D23-D0	LLEN[23:0]	Sets the maximum packet length in byte units. Packets larger than this length are indicated with long packet error. This length is defined as the number of payload bytes received POS packet.	05FCH

(35) Receive ATM/POS interface mode register (MDAPIR) Common register

The MDAPIR register sets the mode related to the receive ATM/POS interface block.

Register Name	Address	Access	Default
MDAPIR	00A4 H	R/W	00000000 H

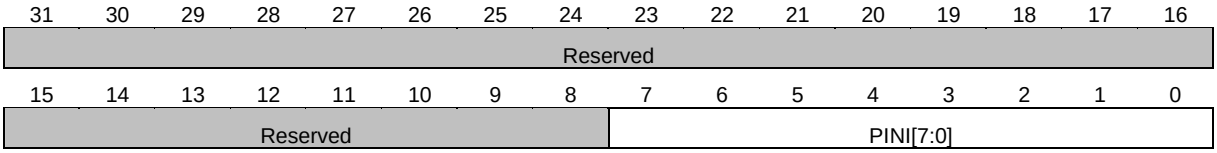


Bit	Field	Function	Default
D31-D12	Reserved	Set to 0.	0
D11	P3FCLS	Stops the data input into the receive FIFO of port3. 1: Stop 0: Normal operation	0
D10	P2FCLS	Stops the data input into the receive FIFO of port2. 1: Stop 0: Normal operation	0
D9	P1FCLS	Stops the data input into the receive FIFO of port1. 1: Stop 0: Normal operation	0
D8	P0FCLS	Stops the data input into the receive FIFO of port0. 1: Stop 0: Normal operation	0
D7-D5	Reserved	Set to 0.	0
D4	IADRM	Sets the insertion of the receive in-band address even if the receive burst transfer is disconnected and resume without the port change. 1: In-band address is inserted every receive transfer. 0: In-band address is not inserted when no port change.	0
D3	IDLM	Sets the idle clocks (RFCLK) inserted after the burst transfer is terminated on the receive POS interface (ex. the port is changed and whole packet transfer is completed). 1: Two idle clocks insert 0: No idle	0
D2	TAGM	Selects whether TAG is used in the format of the receive cell to be transferred via the ATM interface. TAG field is set to any value in the TAGR register when TAG is used. 1: Used 0: Not used	0
D1	UDFM	Selects whether UDF is used in the format of the receive cell to be transferred via the ATM interface. 1: Used 0: Not used	0
D0	PARM	Selects even or odd parity for the parity operation of the receive ATM/POS interface. 1: Even 0: Odd	0

(36) Receive FIFO threshold register (FTHR)

The FTHR register sets the threshold of the receive FIFO.

Register Name	Address				Access	Default
	Port0:	Port1:	Port2:	Port3:		
FTHR	00A8 H	04A8 H	08A8 H	0CA8 H	R/W	00000010 H

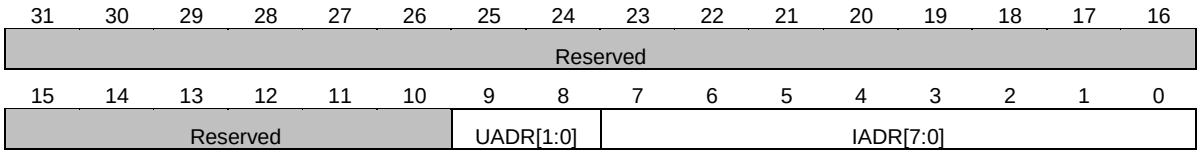


Bit	Field	Function	Default
D31-D8	Reserved	Set to 0.	0
D7-D0	PINI[7:0]	Sets the initial number of words (32-bit width) when uPD98413 start to send the received POS packet to the POS device via receive POS interface. The uPD98413 start to send the data when either the number of words (32-bit width) stored in the receive FIFO exceeds this field or a complete packet is stored in the FIFO.	10H

(37) Receive port address and ATM TAG register (PTADRR)

The PTADRR register sets the receive port address and the value of TAG field of the receive cell.

Register Name	Address	Access	Default
PTADRR	Port0: 00AC H Port1: 04AC H Port2: 08AC H Port3: 0CAC H	R/W	00000000 H 00000101 H 00000202 H 00000303 H

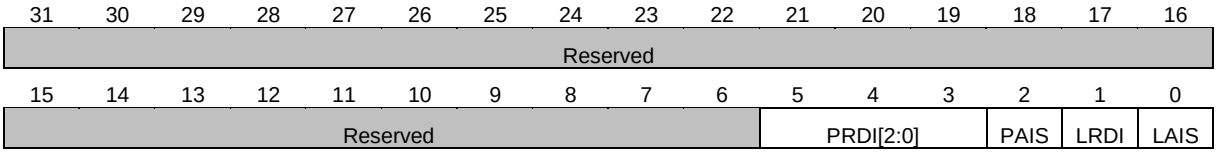


Bit	Field	Function	Default
D31-D10	Reserved	Set to 0.	0
D9-D8	UADR[1:0]	Sets the receive port address for UTOPIA.	Port0: 0 H Port1: 1 H Port2: 2 H Port3: 3 H
D7-D0	IADR[7:0]	UTOPIA mode: Sets the value of TAG field added to the receive cell. POS-PHY mode: Sets the receive in-band port address.	Port0: 00 H Port1: 01 H Port2: 02 H Port3: 03 H

(38) Alarm command register (CMALM)

The CMALM register sets alarm transmission.

Register Name	Address				Access	Default
	Port0:	Port1:	Port2:	Port3:		
CMALM	00C0 H	04C0 H	08C0 H	0CC0 H	R/W	00000000 H

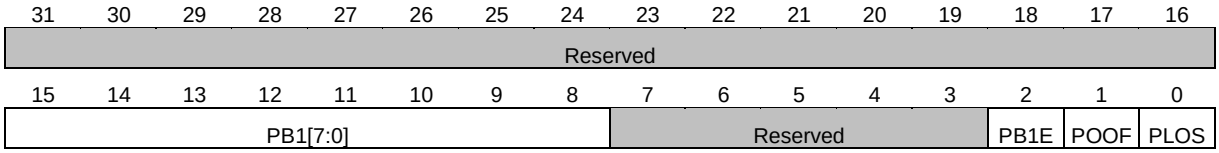


Bit	Field	Function	Default
D31-D6	Reserved	Set to 0.	0
D5-D3	PRDI	One-bit Path RDI mode (PRDI=0 of MDGEN register) 100: Transmission of One-bit Path RDI frame (G1 bit5: 1). One-bit Path RDI frames are successively transmitted while this field are set to 100. Other than 100: Normal operation Enhanced Path RDI mode (PRDI=1 of MDGEN register) 100: Transmission of ERDI-P Server defect frame (G1 bit5-7: 101). ERDI-P Server defect frames are successively transmitted while this field are set to 100. 101: Transmission of ERDI-P Connectivity defect frame (G1 bit5-7: 110). ERDI-P Connectivity defect frames are successively transmitted while this field are set to 101. 110: Transmission of ERDI-P Payload defect frame (G1 bit5-7: 010). ERDI-P Payload defect frames are successively transmitted while this field are set to 110. Other than above value: Normal operation	000
D2	PAIS	1: Transmission of Path AIS frame. Path AIS frames are successively transmitted while this bit is set to 1. 0: Normal operation	0
D1	LRDI	1: Transmission of Line RDI frame. Line RDI frames are successively transmitted while this bit is set to 1. 0: Normal operation	0
D0	LAIS	1: Transmission of Line AIS frame. Line AIS frames are successively transmitted while this bit is set to 1. 0: Normal operation	0

(39) Transmit SOH pseudo error register (PESOH)

The PESOH register sets pseudo error frame transmission related to the SOH operation as a test function.

Register Name	Address				Access	Default
	Port0:	Port1:	Port2:	Port3:		
PESOH	00C4 H	04C4 H	08C4 H	0CC4H	R/W	00000100 H

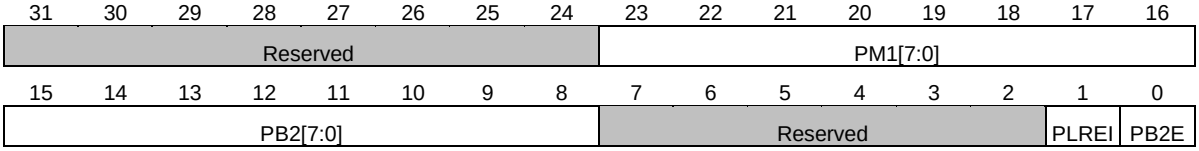


Bit	Field	Function	Default
D31-D16	Reserved	Set to 0.	0
D15-D8	PB1[7:0]	Sets pseudo B1 error frame. Pseudo B1 error frames are inverted the corresponding bits of B1 byte set to “1” in this field.	1 H
D7-D3	Reserved	Set to 0.	0
D2	PB1E	1: Transmits pseudo frame for B1 error generation. Pseudo frames are successively transmitted while this bit is 1. Pseudo error frames are set in the PB1 field. 0: Normal operation	0
D1	POOF	1: Transmits pseudo frame for OOF/LOF generation. Pseudo frames are successively transmitted while this bit is 1. 0: Normal operation	0
D0	PLOS	1: Transmits pseudo frame for LOS generation. Pseudo frames are successively transmitted while this bit is 1. 0: Normal operation	0

(40) Transmit LOH pseudo error register (PELOH)

The PELOH register sets pseudo error frame transmission related to the LOH operation as a test function.

Register Name	Address				Access	Default
	Port0:	Port1:	Port2:	Port3:		
PELOH	00C8 H	04C8 H	08C8 H	0CC8 H	R/W	00010100 H

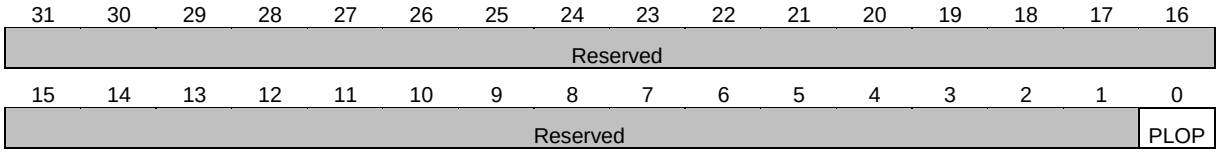


Bit	Field	Function	Default
D31-D24	Reserved	Set to 0.	0
D23-D16	PM1[7:0]	Sets pseudo Line REI error frame. M1 byte is set to any value in this field as Pseudo Line REI error frames.	01 H
D15-D8	PB2[7:0]	Sets pseudo B2 error frame. Pseudo B2 error frames are inverted the corresponding bits of 12th B2 byte set to “1” in this field.	01 H
D7-D2	Reserved	Set to 0.	0
D1	PLREI	1: Transmits pseudo frame for Line REI generation. Pseudo frames are successively transmitted while this bit is 1. Pseudo error frames are set in the M1 field. 0: Normal operation	0
D0	PB2E	1: Transmits pseudo frame for B2 error generation. Pseudo frames are successively transmitted while this bit is 1. Pseudo error frames are set in the B2 field. 0: Normal operation	0

(41) Transmit pointer pseudo error register (PEPTR)

The PEPTR register sets pseudo error frame transmission related to the pointer operation as a test function.

Register Name	Address				Access	Default
	Port0:	Port1:	Port2:	Port3:		
PEPTR	00CC H	04CC H	08CC H	0CCC H	R/W	00000000 H

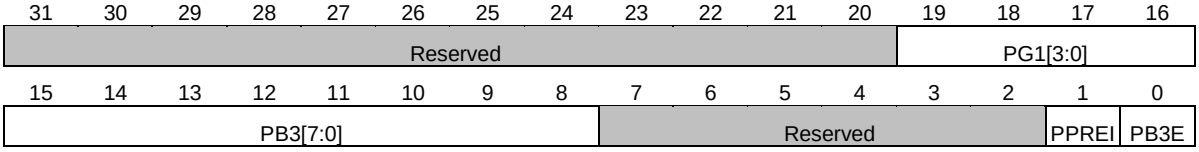


Bit	Field	Function	Default
D31-D1	Reserved	Set to 0.	0
D0	PLOP	1: Transmits pseudo frame for LOP generation. Pseudo frames are successively transmitted while this bit is 1. 0: Normal operation	0

(42) Transmit POH pseudo error register (PEPOH)

The PEPOH register sets pseudo error frame transmission related to the POH operation as a test function.

Register Name	Address				Access	Default
	Port0:	Port1:	Port2:	Port3:		
PEPOH	00D0 H	04D0 H	08D0 H	0CD0 H	R/W	00010100 H

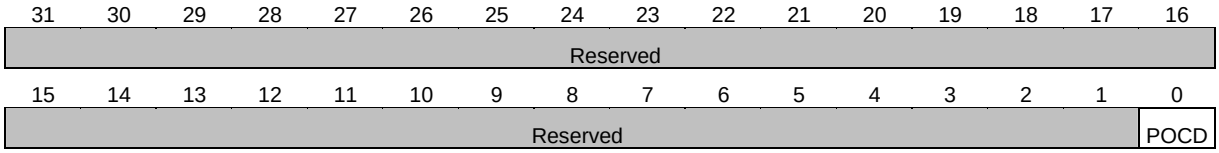


Bit	Field	Function	Default
D31-D20	Reserved	Set to 0.	0
D19-D16	PG1[3:0]	Sets pseudo Path REI error frame. Bit 1 to 4 of G1 byte is set to any value in this field as Pseudo Path REI error frames.	1H
D15-D8	PB3[7:0]	Sets pseudo B3 error frame. Pseudo B3 error frames are inverted the corresponding bits of B3 byte set to “1” in this field.	1H
D7-D2	Reserved	Set to 0.	0
D1	PPREI	1: Transmits pseudo frame for Path REI generation. Pseudo frames are successively transmitted while this bit is 1. Pseudo error frames are set in the G1 field. 0: Normal operation	0
D0	PB3E	1: Transmits pseudo frame for B3 error generation. Pseudo frames are successively transmitted while this bit is 1. Pseudo error frames are set in the B3 field. 0: Normal operation	0

(43) Transmit ATM pseudo error register (PEATM)

The PEATM register sets pseudo error frame transmission related to the ATM operation as a test function.

Register Name	Address				Access	Default
	Port0:	Port1:	Port2:	Port3:		
PEATM	00D4 H	04D4 H	08D4 H	0CD4 H	R/W	00000000 H

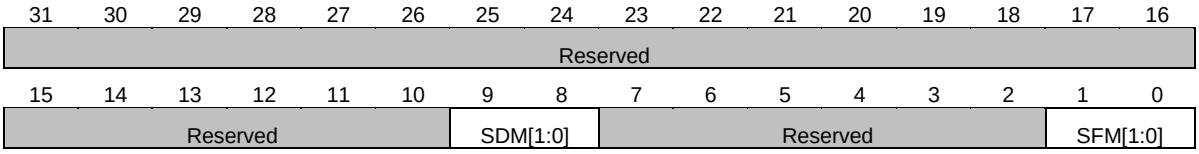


Bit	Field	Function	Default
D31-D1	Reserved	Set to 0.	0
D0	POCD	1: Transmits pseudo frame for OCD/LCD generation. Pseudo frames are successively transmitted while this bit is 1. 0: Normal operation	0

(44) Bit error rate monitoring mode register (MDBER)

The MDBER register sets the monitoring bytes of the bit error rate monitoring function.

Register Name	Address				Access	Default
	Port0:	Port1:	Port2:	Port3:		
MDBER	00E0 H	04E0 H	08E0 H	0CE0 H	R/W	00000202 H

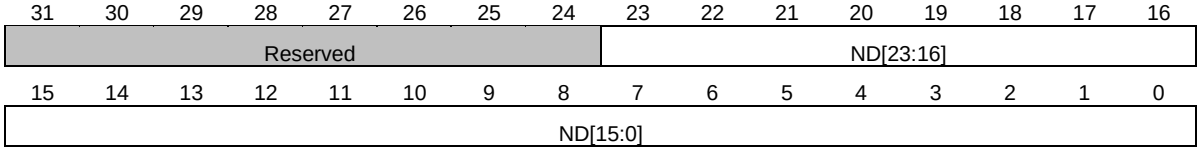


Bit	Field	Function	Default
D31-D10	Reserved	Set to 0.	0
D9-D8	SDM[1:0]	Selects the source and enable which SD condition of the bit error rate monitoring is detected. 11: B3 errors 10: B2 errors 01: B1 errors 00: Disable	10
D7-D2	Reserved	Set to 0.	0
D1-D0	SFM[1:0]	Selects the source and enable which SF condition of the bit error rate monitoring is detected. 11: B3 errors 10: B2 errors 01: B1 errors 00: Disable	10

(45) SF detection N parameter register (SFND)

This register sets the parameters of SF detection.

Register Name	Address				Access	Default
	Port0:	Port1:	Port2:	Port3:		
SFND	00E4 H	04E4 H	08E4 H	0CE4 H	R/W	00000000 H

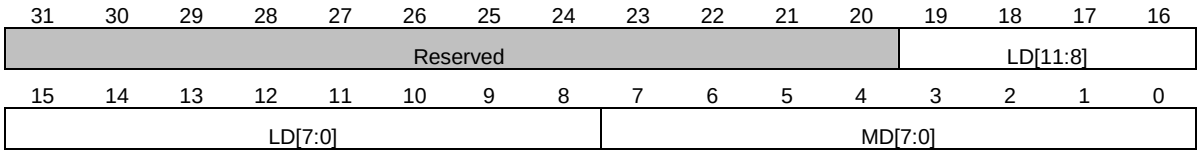


Bit	Field	Function	Default
D31-D24	Reserved	Set to 0.	0
D23-D0	ND[23:0]	Sets parameter "ND" for SF detection. ND defines the length of one frame to be monitored as SF detection condition.	0

(46) SF detection L and M parameters register (SFLMD)

This register sets the parameters of SF detection.

Register Name	Address				Access	Default
	Port0:	Port1:	Port2:	Port3:		
SFLMD	00E8 H	04E8 H	08E8 H	0CE8 H	R/W	00000000 H

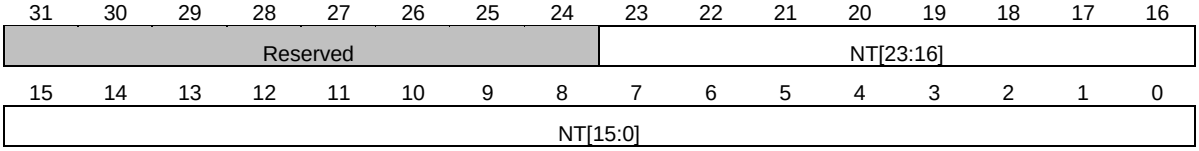


Bit	Field	Function	Default
D31-D20	Reserved	Set to 0.	0
D19-D8	LD[11:0]	Sets parameter "LD" for SF detection. LD defines the threshold of the number of errors that are detected in the ND frame as SF detection condition.	0
D7-D0	MD[7:0]	Sets parameter "MD" for SF detection. MD defines the number of consecutive events as SF detection condition, in each of which LD or more errors are detected in one frame to be monitored (successive ND frames).	0

(47) SF termination N parameter register (SFNT)

This register sets the parameters of SF termination.

Register Name	Address				Access	Default
	Port0:	Port1:	Port2:	Port3:		
SFNT	00EC H	04EC H	08EC H	0CEC H	R/W	00000000 H

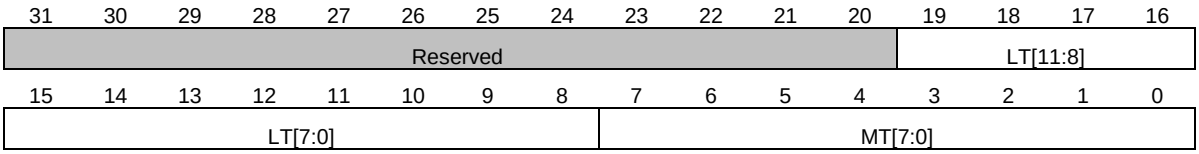


Bit	Field	Function	Default
D31-D24	Reserved	Set to 0.	0
D23-D0	NT[23:0]	Sets parameter "NT" for SF termination. NT defines the length of one frame to be monitored as SF termination condition.	0

(48) SF termination L and M parameters register (SFLMT)

This register sets the parameters of SF termination.

Register Name	Address				Access	Default
	Port0:	Port1:	Port2:	Port3:		
SFLMT	00F0 H	04F0 H	08F0 H	0CF0 H	R/W	00000000 H

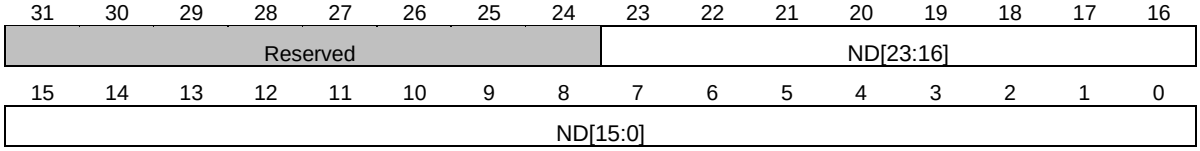


Bit	Field	Function	Default
D31-D20	Reserved	Set to 0.	0
D19-D8	LT[11:0]	Sets parameter "LT" for SF termination. LT defines the threshold of the number of errors that are detected in the NT frame as SF termination condition.	0
D7-D0	MT[7:0]	Sets parameter "MT" for SF termination. MT defines the number of consecutive events as SF termination condition, in each of which less than LT errors are detected in one frame to be monitored (successive NT frames).	0

(49) SD detection N parameter register (SDND)

This register sets the parameters of SD detection.

Register Name	Address				Access	Default
	Port0:	Port1:	Port2:	Port3:		
SDND	00F4 H	04F4 H	08F4 H	0CF4 H	R/W	00000000 H

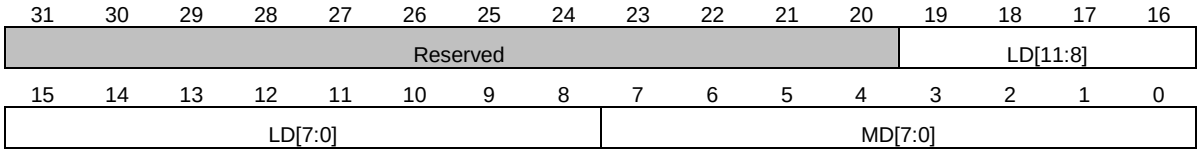


Bit	Field	Function	Default
D31-D24	Reserved	Set to 0.	0
D23-D0	ND[23:0]	Sets parameter "ND" for SD detection. ND defines the length of one frame to be monitored as SD detection condition.	0

(50) SD detection L and M parameters register (SDLMD)

This register sets the parameters of SD detection.

Register Name	Address				Access	Default
	Port0:	Port1:	Port2:	Port3:		
SDLMD	00F8 H	04F8 H	08F8 H	0CF8 H	R/W	00000000 H

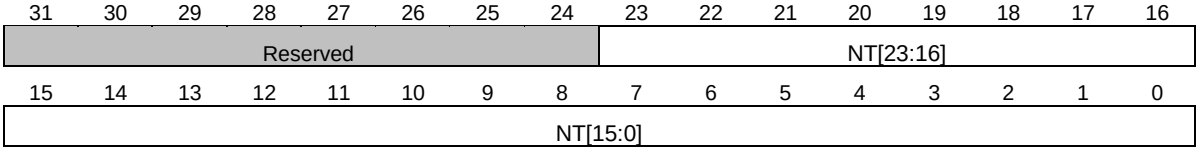


Bit	Field	Function	Default
D31-D20	Reserved	Set to 0.	0
D19-D8	LD[11:0]	Sets parameter "LD" for SD detection. LD defines the threshold of the number of errors that are detected in the ND frame as SD detection condition.	0
D7-D0	MD[7:0]	Sets parameter "MD" for SD detection. MD defines the number of consecutive events as SD detection condition, in each of which LD or more errors are detected in one frame to be monitored (successive ND frames).	0

(51) SD termination N parameter register (SDNT)

This register sets the parameters of SD termination.

Register Name	Address				Access	Default
	Port0:	Port1:	Port2:	Port3:		
SDNT	00FC H	04FC H	08FC H	0CFC H	R/W	00000000 H

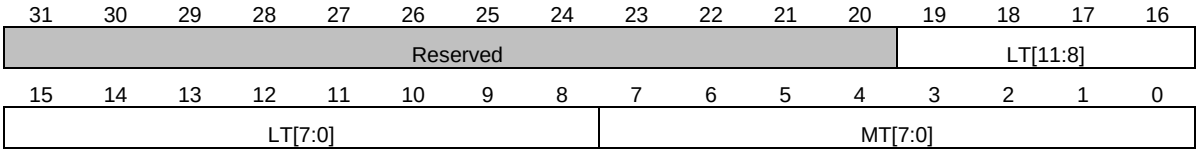


Bit	Field	Function	Default
D31-D24	Reserved	Set to 0.	0
D23-D0	NT[23:0]	Sets parameter "NT" for SD termination. NT defines the length of one frame to be monitored as SD termination condition.	0

(52) SD termination L and M parameters register (SDLMT)

This register sets the parameters of SD termination.

Register Name	Address				Access	Default
	Port0:	Port1:	Port2:	Port3:		
SDLMT	0100 H	0500 H	0900 H	0D00 H	R/W	00000000 H

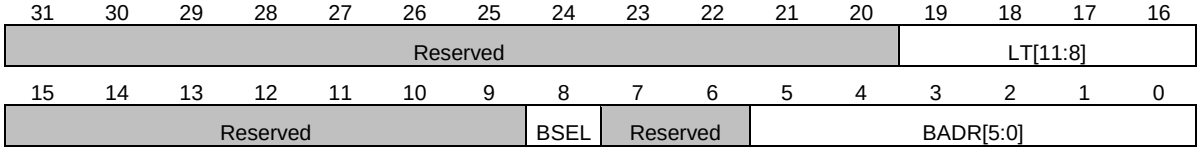


Bit	Field	Function	Default
D31-D20	Reserved	Set to 0.	0
D19-D8	LT[11:0]	Sets parameter "LT" for SD termination. LT defines the threshold of the number of errors that are detected in the NT frame as SD termination condition.	0
D7-D0	MT[7:0]	Sets parameter "MT" for SD termination. MT defines the number of consecutive events as SD termination condition, in each of which less than LT errors are detected in one frame to be monitored (successive NT frames).	0

(53) Transmit trace message buffer register (TMBT)

This register controls the transmit trace message buffer.

Register Name	Address				Access	Default
	Port0:	Port1:	Port2:	Port3:		
TMBT	0110 H	0510 H	0910 H	0D10 H	R/W	00000000 H

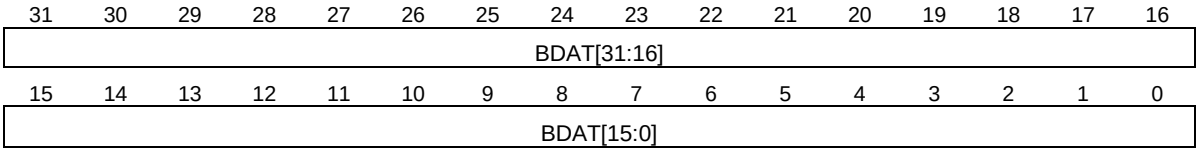


Bit	Field	Function	Default
D31-D9	Reserved	Set to 0.	0
D8	BSEL	Selects the section or path trace message buffer. 1: J1 buffer 0: J0 buffer	0
D7-D6	Reserved	Set to 0.	0
D5-D0	BADR[5:0]	Sets the offset address of the trace message buffer.	00H

(54) Transmit trace message buffer data register (TMDT)

This register is the read/write data of the transmit trace message buffer.

Register Name	Address				Access	Default
	Port0:	Port1:	Port2:	Port3:		
TMDT	0114 H	0514 H	0914 H	0D14 H	R/W	00000000 H

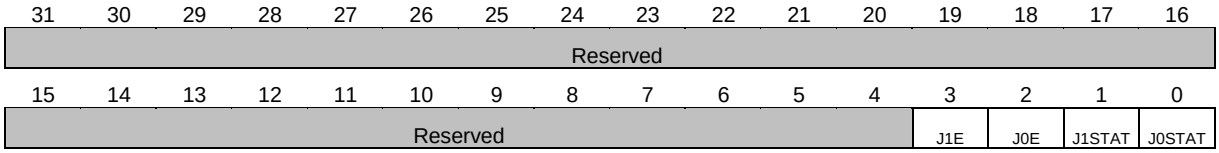


Bit	Field	Function	Default
D31-D0	BDAT[31:0]	32-bit data of the trace message buffer. When read access, the data will be read from the trace message buffer set by TMBT register. When write access, the data will be written into the trace message buffer set by TMBT register.	00000000H

(55) Transmit trace message command register (CMTMT)

This register controls the transmit trace message.

Register Name	Address				Access	Default
	Port0:	Port1:	Port2:	Port3:		
CMTMT	0118 H	0518 H	0918 H	0D18 H	R/W	00000000 H

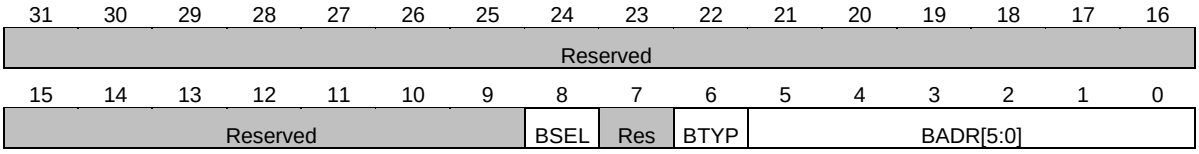


Bit	Field	Function	Default
D31-D4	Reserved	Set to 0.	0
D3	J1E	Enables to transmit the path trace message. 1: Enable 0: Disable	0
D2	J0E	Enables to transmit the section trace message. 1: Enable 0: Disable	0
D1	J1STAT	Starts to transmit new path trace message. 1: Transmits new message 0: Does not change message	0
D0	J0STAT	Starts to transmit new section trace message. 1: Transmits new message 0: Does not change message	0

(56) Receive trace message buffer register (TMBR)

This register controls the receive trace message buffer.

Register Name	Address				Access	Default
	Port0:	Port1:	Port2:	Port3:		
TMBR	011C H	051C H	091C H	0D1C H	R/W	00000000 H

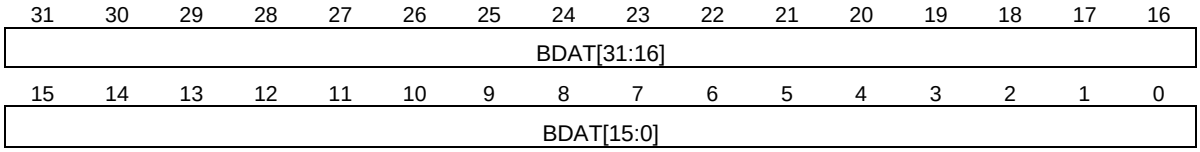


Bit	Field	Function	Default
D31-D9	Reserved	Set to 0.	0
D8	BSEL	Selects the section or path trace message buffer. 1: J1 buffer 0: J0 buffer	0
D7	Reserved	Set to 0.	0
D6	BTYP	Selects the message buffer. 1: Accepted buffer 0: Expected buffer	0
D5-D0	BADR[5:0]	Sets the offset address of the trace message buffer.	00 H

(57) Receive trace message buffer data register (TMDR)

This register is the read/write data of the receive trace message buffer.

Register Name	Address				Access	Default
	Port0:	Port1:	Port2:	Port3:		
TMDR	0120 H	0520 H	0920 H	0D20 H	R/W	00000000 H

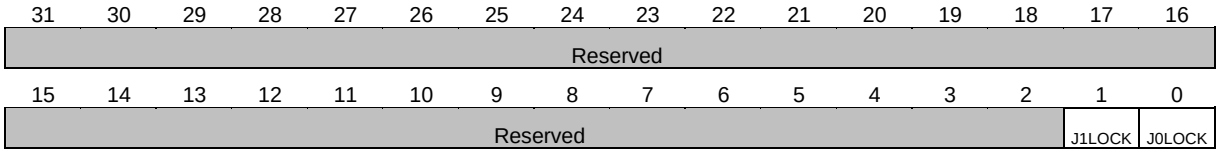


Bit	Field	Function	Default
D31-D0	BDAT[31:0]	32-bit data of the trace message buffer. When read access, the data will be read from the trace message buffer set by TMBR register. When write access, the data will be written into the trace message buffer set by TMBR register.	0H

(58) Receive trace message command register (CMTMR)

This register controls the receive trace message.

Register Name	Address				Access	Default
	Port0:	Port1:	Port2:	Port3:		
CMTMR	0124 H	0524 H	0924 H	0D24 H	R/W	00000000 H

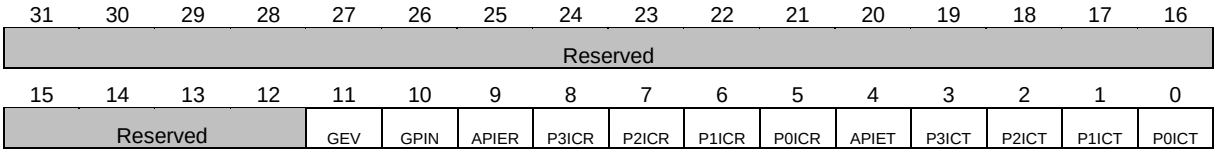


Bit	Field	Function	Default
D31-D2	Reserved	Set to 0.	0
D1	J1LOCK	Indicated and sets to lock the accepted buffer of the path trace message. 1: Lock 0: Unlock	0
D0	J0LOCK	Indicated and sets to lock the accepted buffer of the section trace message. 1: Lock 0: Unlock	0

(59) Interrupt register (INT) Common register

The INT register indicates an interrupt occurrence of the lower cause.

Register Name	Address	Access	Default	Function
INT_RO	0140 H	R	00000000 H	Read-only



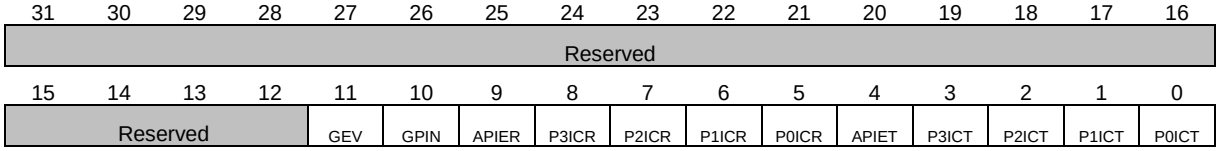
Bit	Field	Function	Default
D31-D12	Reserved		All 0
D11	GEV	1: Indicates that the bits of the GEV register are set. 0: GEV register is all 0.	0
D10	GPIN	1: Indicates that the bits of the GPIN register are set. 0: GPIN register is all 0.	0
D9	APIER	1: Indicates that the ATM/POS interface errors occur. 0: APIER register is all 0.	0
D8	P3ICR	1: Indicates that the receive interrupt occurs in Port3. 0: Corresponding ICR register is all 0.	0
D7	P2ICR	1: Indicates that the receive interrupt occurs in Port2. 0: Corresponding ICR register is all 0.	0
D6	P1ICR	1: Indicates that the receive interrupt occurs in Port1. 0: Corresponding ICR register is all 0.	0
D5	P0ICR	1: Indicates that the receive interrupt occurs in Port0. 0: Corresponding ICR register is all 0.	0
D4	APIET	1: Indicates that the ATM/POS interface errors occur. 0: APIET register is all 0.	0
D3	P3ICT	1: Indicates that the transmit interrupt occurs in Port3. 0: Corresponding ICT register is all 0.	0
D2	P2ICT	1: Indicates that the transmit interrupt occurs in Port2. 0: Corresponding ICT register is all 0.	0
D1	P1ICT	1: Indicates that the transmit interrupt occurs in Port1. 0: Corresponding ICT register is all 0.	0
D0	P0ICT	1: Indicates that the transmit interrupt occurs in Port0. 0: Corresponding ICT register is all 0.	0

Note : Depends on the corresponding register status.

(60) Interrupt mask register (INT_M) Common register

The INT_M resister is mask register of the INT register.

Register Name	Address	Access	Default	Function
INT_M	0144 H	R/W	00000FFF H	Mask register

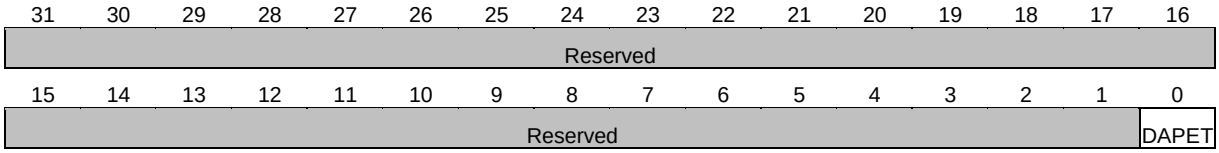


Bit	Field	Function	Default
D31-D12	Reserved	Set to 0.	All 0
D11	GEV	1: Mask 0: Unmask	1
D10	GPIN	1: Mask 0: Unmask	1
D9	APIER	1: Mask 0: Unmask	1
D8	P3ICR	1: Mask 0: Unmask	1
D7	P2ICR	1: Mask 0: Unmask	1
D6	P1ICR	1: Mask 0: Unmask	1
D5	P0ICR	1: Mask 0: Unmask	1
D4	APIET	1: Mask 0: Unmask	1
D3	P3ICT	1: Mask 0: Unmask	1
D2	P2ICT	1: Mask 0: Unmask	1
D1	P1ICT	1: Mask 0: Unmask	1
D0	P0ICT	1: Mask 0: Unmask	1

(61) Transmit interrupt cause register (ICT)

The ICT register indicates interrupt causes.

Register Name	Address				Access	Default	Function
	Port0:	Port1:	Port2:	Port3:			
ICT_RO	0150 H	0550 H	0950 H	0D50 H	R	00000000 H	Read-only

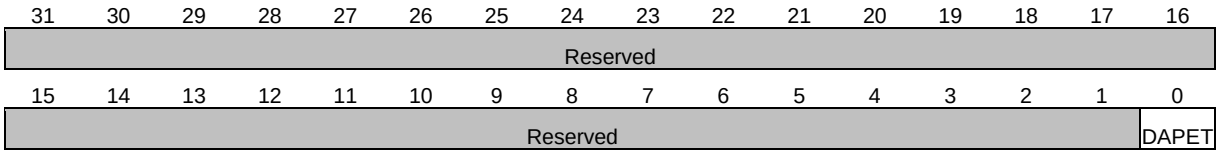


Bit	Field	Function	Default
D31-D1	Reserved	Reserved	All 0
D0	DAPET	1: Indicates that the bits of the DAPET register are set. 0: DAPET register is all 0.	0

(62) Transmit interrupt cause Mask register (ICT_M)

The ICT_M register is mask register of the ICT register.

Register Name	Address				Access	Default	Function
	Port0:	Port1:	Port2:	Port3:			
ICT_M	0154 H	0554 H	0954 H	0D54 H	R/W	00000001 H	Mask register

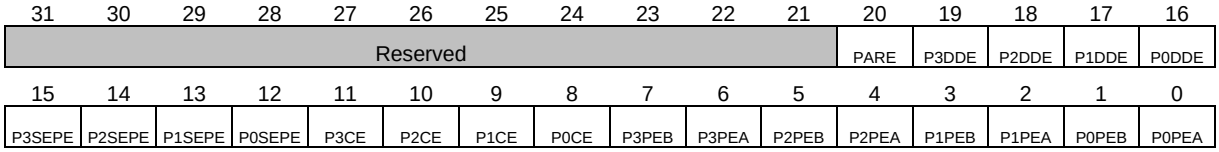


Bit	Field	Function	Default
D31-D1	Reserved	Set to 0	All 0
D0	DAPET	1: Mask 0: Unmask	1

(63) Transmit ATM/POS interface error register (APIET) Common register

The APIET register indicates the causes of a transmit ATM/POS interface error.

Register Name	Address	Access	Default	Function
APIET_RWC	0160 H	R/WC	00000000 H	Read-only / Write clear
APIET_RC	0164 H	RC	00000000 H	Read clear



Bit	Field	Function	Default
D31-D21	Reserved		All 0
D20	PARE	1: Detects a parity error in the transmit ATM/POS interface. 0: Does not detect.	0
D19	P3DDE	1: Detects a cell or packet discard, because TXCLAV or TPA is ignored and transmit FIFO overflow occurs for port 3. 0: Does not detect.	0
D18	P2DDE	1: Detects a cell or packet discard, because TXCLAV or TPA is ignored and transmit FIFO overflow occurs for port 2. 0: Does not detect.	0
D17	P1DDE	1: Detects a cell or packet discard, because TXCLAV or TPA is ignored and transmit FIFO overflow occurs for port 1. 0: Does not detect.	0
D16	P0DDE	1: Detects a cell or packet discard, because TXCLAV or TPA is ignored and transmit FIFO overflow occurs for port 0. 0: Does not detect.	0
D15	P3SEPE	POS-PHY mode (APIM=0 in MDDGEN): 1: Detects the wrong order for SOP and EOP of port 3. 0: Does not detect. UTOPIA mode (APIM=1 in MDDGEN): This field is no function and always 0. uPD98413 does not indicate this error.	0
D14	P2SEPE	POS-PHY mode (APIM=0 in MDDGEN): 1: Detects the wrong order for SOP and EOP of port 2. 0: Does not detect. UTOPIA mode (APIM=1 in MDDGEN): This field is no function and always 0. uPD98413 does not indicate this error.	0

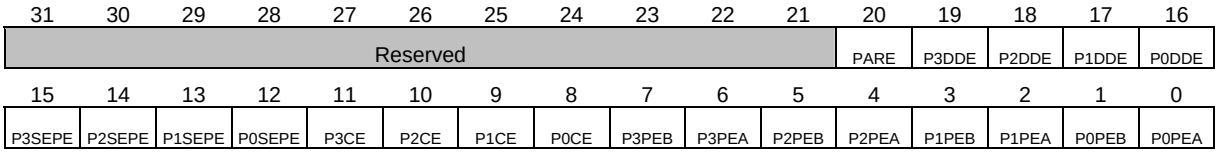
D13	P1SEPE	POS-PHY mode (APIM=0 in MDDGEN): 1: Detects the wrong order for SOP and EOP of port 1. 0: Does not detect. UTOPIA mode (APIM=1 in MDDGEN): This field is no function and always 0. uPD98413 does not indicate this error.	0
D12	P0SEPE	POS-PHY mode (APIM=0 in MDDGEN): 1: Detects the wrong order for SOP and EOP of port 0. 0: Does not detect. UTOPIA mode (APIM=1 in MDDGEN): This field is no function and always 0. uPD98413 does not indicate this error.	0
D11	P3CE	UTOPIA mode (APIM=1 in MDDGEN): 1: Detects that TXENB_B is deasserted or TXSOC is asserted while a cell transfer of port 3. 0: Does not detect. Cell on POS-PHY mode (APIM=0 in MDDGEN and APM=1 in MDPGEN): 1: Detects that the data size is not 53 bytes from TSOP to TEOP of port 3. 0: Does not detect. Packet on POS-PHY mode (APIM=0 in MDDGEN and APM=0 in MDPGEN): This field is no function and always 0. uPD98413 does not indicate this error.	0
D10	P2CE	UTOPIA mode (APIM=1 in MDDGEN): 1: Detects that TXENB_B is deasserted or TXSOC is asserted while a cell transfer of port 2. 0: Does not detect. Cell on POS-PHY mode (APIM=0 in MDDGEN and APM=1 in MDPGEN): 1: Detects that the data size is not 53 bytes from TSOP to TEOP of port 2. 0: Does not detect. Packet on POS-PHY mode (APIM=0 in MDDGEN and APM=0 in MDPGEN): This field is no function and always 0. uPD98413 does not indicate this error.	0
D9	P1CE	UTOPIA mode (APIM=1 in MDDGEN): 1: Detects that TXENB_B is deasserted or TXSOC is asserted while a cell transfer of port 1. 0: Does not detect. Cell on POS-PHY mode (APIM=0 in MDDGEN and APM=1 in MDPGEN): 1: Detects that the data size is not 53 bytes from TSOP to TEOP of port 1. 0: Does not detect. Packet on POS-PHY mode (APIM=0 in MDDGEN and APM=0 in MDPGEN): This field is no function and always 0. uPD98413 does not indicate this error.	0

D8	P0CE	UTOPIA mode (APIM=1 in MDDGEN): 1: Detects that TXENB_B is deasserted or TXSOC is asserted while a cell transfer of port 0. 0: Does not detect. Cell on POS-PHY mode (APIM=0 in MDDGEN and APM=1 in MDPGEN): 1: Detects that the data size is not 53 bytes from TSOP to TEOP of port 0. 0: Does not detect. Packet on POS-PHY mode (APIM=0 in MDDGEN and APM=0 in MDPGEN): This field is no function and always 0. uPD98413 does not indicate this error.	0
D7	P3PEB	1: Detects a parity error in the transmit FIFO RAM-B of port 3. 0: Does not detect.	0
D6	P3PEA	1: Detects a parity error in the transmit FIFO RAM-A of port 3. 0: Does not detect.	0
D5	P2PEB	1: Detects a parity error in the transmit FIFO RAM-B of port 2. 0: Does not detect.	0
D4	P2PEA	1: Detects a parity error in the transmit FIFO RAM-A of port 2. 0: Does not detect.	0
D3	P1PEB	1: Detects a parity error in the transmit FIFO RAM-B of port 1. 0: Does not detect.	0
D2	P1PEA	1: Detects a parity error in the transmit FIFO RAM-A of port 1. 0: Does not detect.	0
D1	P0PEB	1: Detects a parity error in the transmit FIFO RAM-B of port 0. 0: Does not detect.	0
D0	P0PEA	1: Detects a parity error in the transmit FIFO RAM-A of port 0. 0: Does not detect.	0

(64) Transmit ATM/POS interface error Read Clear Enable register (APIET_RCE) Common register

The APIET_RCE register is Read Clear Enable register of APIET_RC register.

Register Name	Address	Access	Default	Function
APIET_RCE	0168 H	R/W	001FFFFF H	Read clear enable

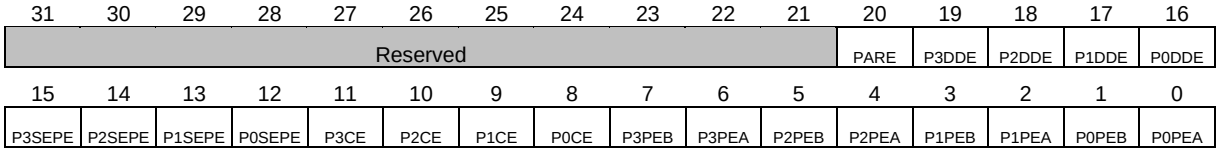


Bit	Field	Function		Default
D31-D21	Reserved	Reserved		All 0
D20	PARE	1: Enable	0: Disable	1
D19	P3DDE	1: Enable	0: Disable	1
D18	P2DDE	1: Enable	0: Disable	1
D17	P1DDE	1: Enable	0: Disable	1
D16	P0DDE	1: Enable	0: Disable	1
D15	P3SEPE	1: Enable	0: Disable	1
D14	P2SEPE	1: Enable	0: Disable	1
D13	P1SEPE	1: Enable	0: Disable	1
D12	P0SEPE	1: Enable	0: Disable	1
D11	P3CE	1: Enable	0: Disable	1
D10	P2CE	1: Enable	0: Disable	1
D9	P1CE	1: Enable	0: Disable	1
D8	P0CE	1: Enable	0: Disable	1
D7	P3PEB	1: Enable	0: Disable	1
D6	P3PEA	1: Enable	0: Disable	1
D5	P2PEB	1: Enable	0: Disable	1
D4	P2PEA	1: Enable	0: Disable	1
D3	P1PEB	1: Enable	0: Disable	1
D2	P1PEA	1: Enable	0: Disable	1
D1	P0PEB	1: Enable	0: Disable	1
D0	P0PEA	1: Enable	0: Disable	1

(65) Transmit ATM/POS interface error Mask register (APIET_M) Common register

The APIET_M register is mask register of APIET register.

Register Name	Address	Access	Default	Function
APIET_M	016C H	R/W	001FFFFF H	Mask register

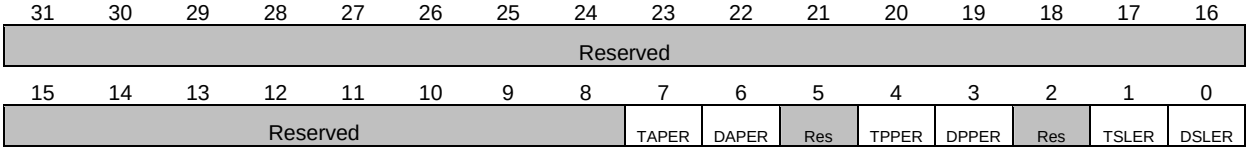


Bit	Field	Function		Default
D31-D21	Reserved	Set to 0.		All 0
D20	PARE	1: Mask	0: Unmask	1
D19	P3DDE	1: Mask	0: Unmask	1
D18	P2DDE	1: Mask	0: Unmask	1
D17	P1DDE	1: Mask	0: Unmask	1
D16	P0DDE	1: Mask	0: Unmask	1
D15	P3SEPE	1: Mask	0: Unmask	1
D14	P2SEPE	1: Mask	0: Unmask	1
D13	P1SEPE	1: Mask	0: Unmask	1
D12	P0SEPE	1: Mask	0: Unmask	1
D11	P3CE	1: Mask	0: Unmask	1
D10	P2CE	1: Mask	0: Unmask	1
D9	P1CE	1: Mask	0: Unmask	1
D8	P0CE	1: Mask	0: Unmask	1
D7	P3PEB	1: Mask	0: Unmask	1
D6	P3PEA	1: Mask	0: Unmask	1
D5	P2PEB	1: Mask	0: Unmask	1
D4	P2PEA	1: Mask	0: Unmask	1
D3	P1PEB	1: Mask	0: Unmask	1
D2	P1PEA	1: Mask	0: Unmask	1
D1	P0PEB	1: Mask	0: Unmask	1
D0	P0PEA	1: Mask	0: Unmask	1

(66) Receive interrupt cause register (ICR)

The ICR register indicates interrupt causes.

Register Name	Address				Access	Default	Function
	Port0:	Port1:	Port2:	Port3:			
ICR_RO	0170 H	0570 H	0970 H	0D70 H	R	00000000 H	Read-only



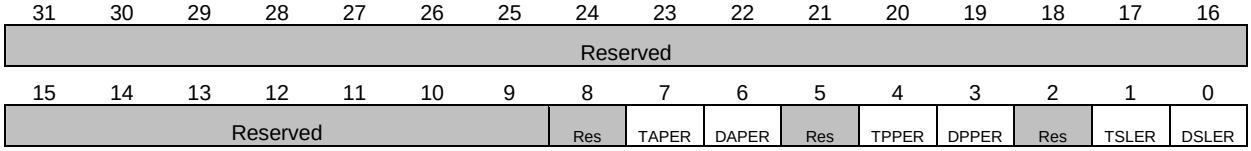
Bit	Field	Function	Default
D31-D8	Reserved	Reserved	All 0
D7	TAPER	1: Indicates that the bits of the TAPER register are set. 0: TAPER register is all 0.	0
D6	DAPER	1: Indicates that the bits of the DAPER register are set. 0: DAPER register is all 0.	0
D5	Reserved	Reserved	All 0
D4	TPPER	1: Indicates that the bits of the TPPER register are set. 0: TPPER register is all 0.	0
D3	DPPER	1: Indicates that the bits of the DPPER register are set. 0: DPPER register is all 0.	0
D2	Reserved	Reserved	All 0
D1	TSLER	1: Indicates that the bits of the TSLER register are set. 0: TSLER register is all 0.	0
D0	DSLER	1: Indicates that the bits of the DSLER register are set. 0: DSLER register is all 0.	0

Note : Default value of this register is depends on status of corresponding register.

(67) Receive interrupt cause Mask register (ICR_M)

The ICR_M register is the mask register of ICR register.

Register Name	Address				Access	Default	Function
	Port0:	Port1:	Port2:	Port3:			
ICR_M	0174 H	0574 H	0974 H	0D74 H	R/W	000001FF H	Mask register

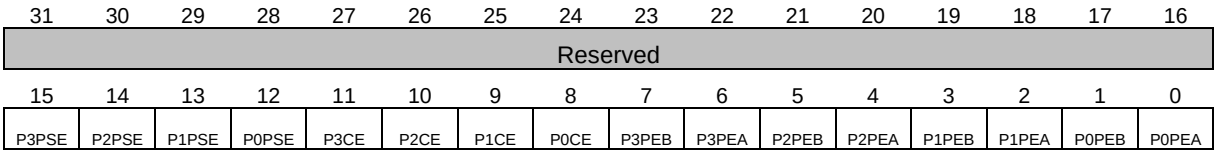


Bit	Field	Function	Default
D31-D9	Reserved	Set to 0	0
D8	Reserved	Set to 1	1
D7	TAPER	1: Mask 0: Unmask	1
D6	DAPER	1: Mask 0: Unmask	1
D5	Reserved	Set to 1	1
D4	TPPER	1: Mask 0: Unmask	1
D3	DPPER	1: Mask 0: Unmask	1
D2	Reserved	Set to 1	1
D1	TSLER	1: Mask 0: Unmask	1
D0	DSLER	1: Mask 0: Unmask	1

(68) Receive ATM/POS interface error register (APIER) Common register

The APIER register indicates the causes of a receive ATM/POS interface error.

Register Name	Address	Access	Default	Function
APIER_RWC	0180 H	R/WC	00000000 H	Read-only / Write clear
APIER_RC	0184 H	RC	00000000 H	Read clear



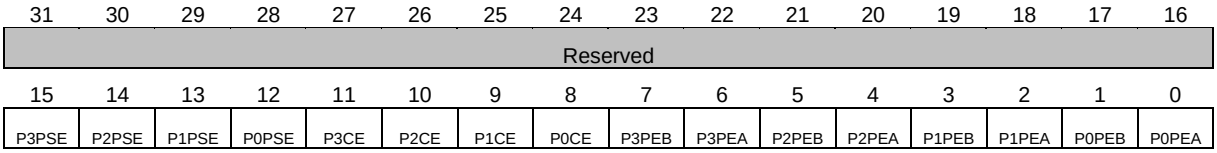
Bit	Field	Function	Default
D31-D16	Reserved	Reserved	All 0
D15	P3PSE	UTOPIA mode (APIM=1 in MDDGEN): 1: Detects that port3 is selected although the corresponding RXCLAV is low (not active). 0: Does not detect. POS-PHY mode (APIM=0 in MDDGEN): This field is no function and always 0. uPD98413 does not indicate this error.	0
D14	P2PSE	UTOPIA mode (APIM=1 in MDDGEN): 1: Detects that port2 is selected although the corresponding RXCLAV is low (not active). 0: Does not detect. POS-PHY mode (APIM=0 in MDDGEN): This field is no function and always 0. uPD98413 does not indicate this error.	0
D13	P1PSE	UTOPIA mode (APIM=1 in MDDGEN): 1: Detects that port1 is selected although the corresponding RXCLAV is low (not active). 0: Does not detect. POS-PHY mode (APIM=0 in MDDGEN): This field is no function and always 0. uPD98413 does not indicate this error.	0
D12	P0PSE	UTOPIA mode (APIM=1 in MDDGEN): 1: Detects that port0 is selected although the corresponding RXCLAV is low (not active). 0: Does not detect. POS-PHY mode (APIM=0 in MDDGEN): This field is no function and always 0. uPD98413 does not indicate this error.	0

D11	P3CE	UTOPIA mode (APIM=1 in MDDGEN): 1: Detects that RXENB_B is deasserted while a cell transfer of port 3. 0: Does not detect. POS-PHY mode (APIM=0 in MDDGEN): This field is no function and always 0. uPD98413 does not indicate this error.	0
D10	P2CE	UTOPIA mode (APIM=1 in MDDGEN): 1: Detects that RXENB_B is deasserted while a cell transfer of port 2. 0: Does not detect. POS-PHY mode (APIM=0 in MDDGEN): This field is no function and always 0. uPD98413 does not indicate this error.	0
D9	P1CE	UTOPIA mode (APIM=1 in MDDGEN): 1: Detects that RXENB_B is deasserted while a cell transfer of port 1. 0: Does not detect. POS-PHY mode (APIM=0 in MDDGEN): This field is no function and always 0. uPD98413 does not indicate this error.	0
D8	P0CE	UTOPIA mode (APIM=1 in MDDGEN): 1: Detects that RXENB_B is deasserted while a cell transfer of port 0. 0: Does not detect. POS-PHY mode (APIM=0 in MDDGEN): This field is no function and always 0. uPD98413 does not indicate this error.	0
D7	P3PEB	1: Detects a parity error in the receive FIFO RAM-B of port 3. 0: Does not detect.	0
D6	P3PEA	1: Detects a parity error in the receive FIFO RAM-A of port 3. 0: Does not detect.	0
D5	P2PEB	1: Detects a parity error in the receive FIFO RAM-B of port 2. 0: Does not detect.	0
D4	P2PEA	1: Detects a parity error in the receive FIFO RAM-A of port 2. 0: Does not detect.	0
D3	P1PEB	1: Detects a parity error in the receive FIFO RAM-B of port 1. 0: Does not detect.	0
D2	P1PEA	1: Detects a parity error in the receive FIFO RAM-A of port 1. 0: Does not detect.	0
D1	P0PEB	1: Detects a parity error in the receive FIFO RAM-B of port 0. 0: Does not detect.	0
D0	P0PEA	1: Detects a parity error in the receive FIFO RAM-A of port 0. 0: Does not detect.	0

(69) Receive ATM/POS interface error Read Clear Enable register (APIER_RCE) Common register

The APIER register is read clear enable register of APIER_RC register.

Register Name	Address	Access	Default	Function
APIER_RCE	0188 H	R/W	0000FFFF H	Read clear enable

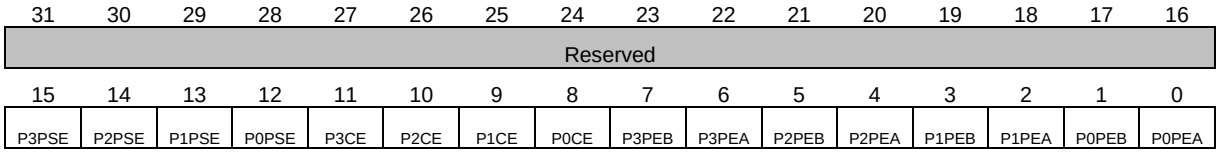


Bit	Field	Function	Default
D31-D16	Reserved	Reserved	All 0
D15	P3PSE	1: Enable 0:disable	1
D14	P2PSE	1: Enable 0:disable	1
D13	P1PSE	1: Enable 0:disable	1
D12	P0PSE	1: Enable 0:disable	1
D11	P3CE	1: Enable 0:disable	1
D10	P2CE	1: Enable 0:disable	1
D9	P1CE	1: Enable 0:disable	1
D8	P0CE	1: Enable 0:disable	1
D7	P3PEB	1: Enable 0:disable	1
D6	P3PEA	1: Enable 0:disable	1
D5	P2PEB	1: Enable 0:disable	1
D4	P2PEA	1: Enable 0:disable	1
D3	P1PEB	1: Enable 0:disable	1
D2	P1PEA	1: Enable 0:disable	1
D1	P0PEB	1: Enable 0:disable	1
D0	P0PEA	1: Enable 0:disable	1

(70) Receive ATM/POS interface error Mask register (APIER_M) Common register

The APIER register is mask register of APIER register.

Register Name	Address	Access	Default	Function
APIER_M	018C H	R/W	0000FFFF H	Mask register

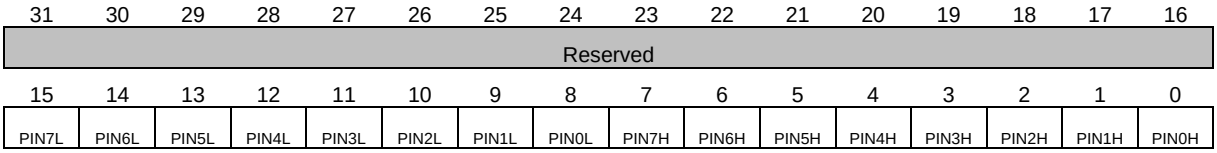


Bit	Field	Function		Default
D31-D16	Reserved	Reserved		All 0
D15	P3PSE	1: mask	0: unmask	1
D14	P2PSE	1: mask	0: unmask	1
D13	P1PSE	1: mask	0: unmask	1
D12	P0PSE	1: mask	0: unmask	1
D11	P3CE	1: mask	0: unmask	1
D10	P2CE	1: mask	0: unmask	1
D9	P1CE	1: mask	0: unmask	1
D8	P0CE	1: mask	0: unmask	1
D7	P3PEB	1: mask	0: unmask	1
D6	P3PEA	1: mask	0: unmask	1
D5	P2PEB	1: mask	0: unmask	1
D4	P2PEA	1: mask	0: unmask	1
D3	P1PEB	1: mask	0: unmask	1
D2	P1PEA	1: mask	0: unmask	1
D1	P0PEB	1: mask	0: unmask	1
D0	P0PEA	1: mask	0: unmask	1

(71) General-purpose input port status register (GPIN) Common register

The GPIN register indicates the signal level of each general-purpose input pin. Each bit is available when each general-purpose I/O pin is input mode.

Register Name	Address	Access	Default	Function
GPIN_RO	0190 H	R	**Note**	Read-only



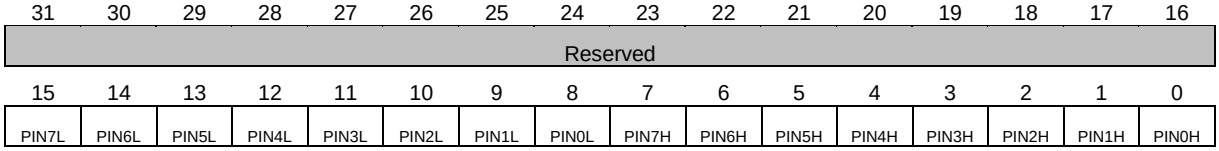
Bit	Field	Function	Default
D31-D16	Reserved	Reserved	0
D15	PIN7L	Inverts and indicates the input level of the PIO7 pin. 1: Low 0: High	**Note**
D14	PIN6L	Inverts and indicates the input level of the PIO6 pin. 1: Low 0: High	
D13	PIN5L	Inverts and indicates the input level of the PIO5 pin. 1: Low 0: High	
D12	PIN4L	Inverts and indicates the input level of the PIO4 pin. 1: Low 0: High	
D11	PIN3L	Inverts and indicates the input level of the PIO3 pin. 1: Low 0: High	
D10	PIN2L	Inverts and indicates the input level of the PIO2 pin. 1: Low 0: High	
D9	PIN1L	Inverts and indicates the input level of the PIO1 pin. 1: Low 0: High	
D8	PIN0L	Inverts and indicates the input level of the PIO0 pin. 1: Low 0: High	
D7	PIN7H	Indicates the input level of the PIO7 pin. 1: High 0: Low	
D6	PIN6H	Indicates the input level of the PIO6 pin. 1: High 0: Low	
D5	PIN5H	Indicates the input level of the PIO5 pin. 1: High 0: Low	
D4	PIN4H	Indicates the input level of the PIO4 pin. 1: High 0: Low	
D3	PIN3H	Indicates the input level of the PIO3 pin. 1: High 0: Low	
D2	PIN2H	Indicates the input level of the PIO2 pin. 1: High 0: Low	
D1	PIN1H	Indicates the input level of the PIO1 pin. 1: High 0: Low	
D0	PIN0H	Indicates the input level of the PIO0 pin. 1: High 0: Low	

Note: the default value of this register is depends on input level of corresponding PIO pins

(72) General-purpose input port status Mask register (GPIN_M) Common register

The GPIN_M register is mask register of GPIN register.

Register Name	Address	Access	Default	Function
GPIN_M	0194 H	R/W	0000FFFF H	Mask register

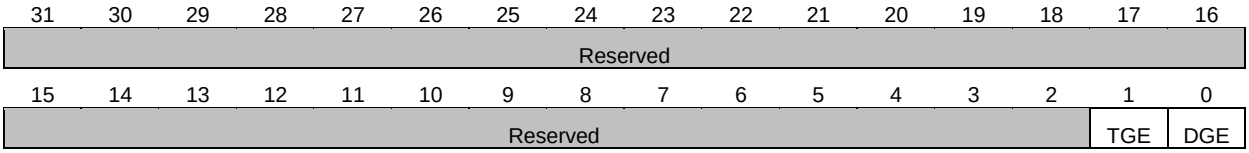


Bit	Field	Function	Default
D31-D16	Reserved	Reserved	0
D15	PIN7L	1: mask 0: unmask	1
D14	PIN6L	1: mask 0: unmask	1
D13	PIN5L	1: mask 0: unmask	1
D12	PIN4L	1: mask 0: unmask	1
D11	PIN3L	1: mask 0: unmask	1
D10	PIN2L	1: mask 0: unmask	1
D9	PIN1L	1: mask 0: unmask	1
D8	PIN0L	1: mask 0: unmask	1
D7	PIN7H	1: mask 0: unmask	1
D6	PIN6H	1: mask 0: unmask	1
D5	PIN5H	1: mask 0: unmask	1
D4	PIN4H	1: mask 0: unmask	1
D3	PIN3H	1: mask 0: unmask	1
D2	PIN2H	1: mask 0: unmask	1
D1	PIN1H	1: mask 0: unmask	1
D0	PIN0H	1: mask 0: unmask	1

(73) General event register (GEV) Common register

The GEV register indicates the causes of the general event.

Register Name	Address	Access	Default	Function
GEV_RO	01A0 H	R	00000000 H	Read-only

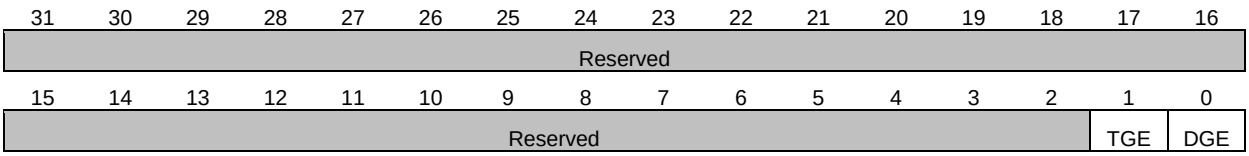


Bit	Field	Function	Default
D31-D2	Reserved	Reserved	0
D1	TGE	1: Indicates that the bits of the TGE register are set. 0: TGE register is all 0.	0
D0	DGE	1: Indicates that the bits of the DGE register are set. 0: DGE register is all 0.	0

(74) General event Mask register (GEV_M) Common register

The GEV_M register is mask register of GEV register.

Register Name	Address	Access	Default	Function
GEV_M	01A4 H	R/W	00000003 H	Mask register

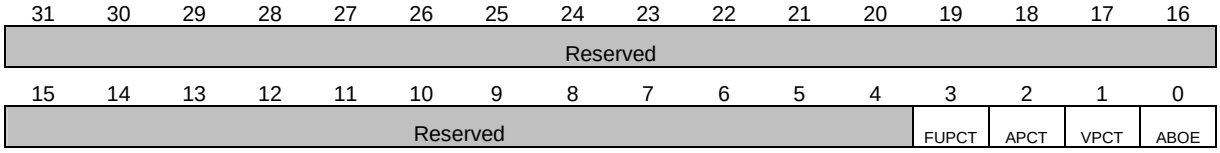


Bit	Field	Function	Default
D31-D2	Reserved	Reserved	0
D1	TGE	1: mask 0: unmask	1
D0	DGE	1: mask 0: unmask	1

(75) Transmit ATM/POS layer event detection registers (DAPET)

The DAPET registers indicate whether the occurrence of each event was detected.

Register Name	Address				Access	Default	Function
	Port0:	Port1:	Port2:	Port3:			
DAPET_RWC	01B0 H	05B0 H	09B0 H	0DB0 H	R/WC	00000000 H	Read-only / Write clear
DAPET_RC	01B4 H	05B4 H	09B4 H	0DB4 H	RC	00000000 H	Read clear

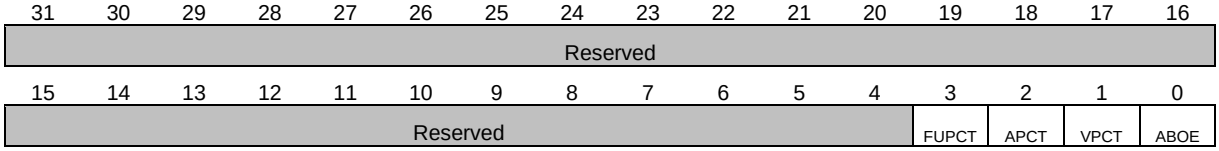


Bit	Field	Function	Default
D31-D4	Reserved	Reserved	All 0
D3	FUPCT	1: Detects occurrence of an overflow in transmit FIFO underflow packet counter. 0: Does not detect.	0
D2	APCT	1: Detects occurrence of an overflow in transmit abort packet counter. 0: Does not detect.	0
D1	VPCT	1: Detects occurrence of an overflow in transmit valid cell/packet counter. 0: Does not detect.	0
D0	ABOE	1: Detects occurrence of transmit abort packet due to a transmit FIFO underflow. 0: Does not detect.	0

(76) Transmit ATM/POS layer event detection Read Clear Enable registers (DAPET_RCE)

The DAPET registers is read clear enable register of DAPET_RC register.

Register Name	Address				Access	Default	Function
	Port0:	Port1:	Port2:	Port3:			
DAPET_RCE	01B8 H	05B8 H	09B8 H	0DB8 H	R/W	0000007F H	Read clear enable

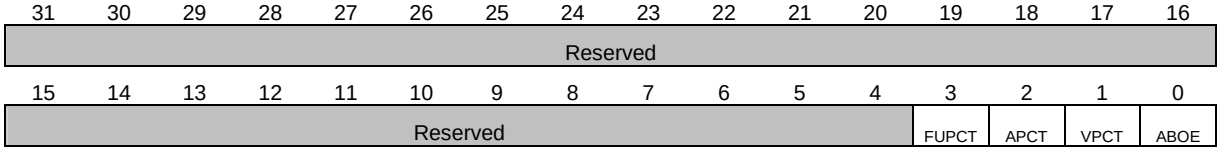


Bit	Field	Function	Default
D31-D4	Reserved	Set to 0.	All 0
D3	FUPCT	1: enable 0: disable	1
D2	APCT	1: enable 0: disable	1
D1	VPCT	1: enable 0: disable	1
D0	ABOE	1: enable 0: disable	1

(77) Transmit ATM/POS layer event detection Mask registers (DAPET_M)

The DAPET register is mask register of the DAPET register.

Register Name	Address				Access	Default	Function
	Port0:	Port1:	Port2:	Port3:			
DAPET_M	01BC H	05BC H	09BC H	0DBC H	R/W	0000007F h	Mask register.

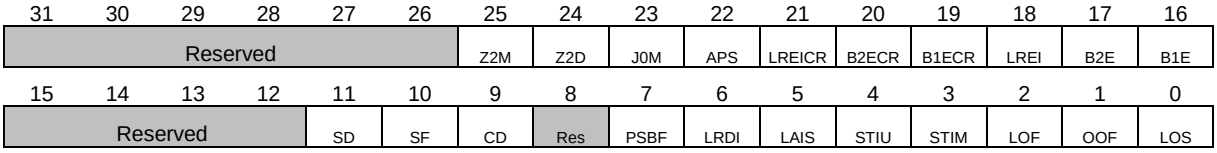


Bit	Field	Function	Default
D31-D7	Reserved	Set to 0.	All 0
D3	FUPCT	1: mask 0: unmask	1
D2	APCT	1: mask 0: unmask	1
D1	VPCT	1: mask 0: unmask	1
D0	ABOE	1: mask 0: unmask	1

(78) Receive section and line layer event detection registers (DSLER)

The DSLER registers indicate whether the occurrence of each event was detected.

Register Name	Address				Access	Default	Function
	Port0:	Port1:	Port2:	Port3:			
DSLER_RWC	01C0 H	05C0 H	09C0 H	0DC0 H	R/WC	**Note**	Read-only / Write clear
DSLER_RC	01C4 H	05C4 H	09C4 H	0DC4 H	RC	**Note**	Read clear



Bit	Field	Function	Default
D31-D26	Reserved	Reserved	0
D25	Z2M	1: Bits 7 to 8 of 1st Z2 byte has been received. 0: Not detected.	0
D24	Z2D	1: Bits 6 to 7 of 1st Z2 byte has been received. 0: Not detected.	0
D23	J0M	1: Storing J0 message has been completed. 0: Not completed.	0
D22	APS	1: APS signal has been received. 0: Not detected.	0
D21	LREICR	1: Detects occurrence of an overflow in Line REI counter. 0: Does not detect.	0
D20	B2ECR	1: Detects occurrence of an overflow in B2 error counter. 0: Does not detect.	0
D19	B1ECR	1: Detects occurrence of an overflow in B1 error counter. 0: Does not detect.	0
D18	LREI	1: Detects Line REI. 0: Does not detect.	0
D17	B2E	1: Detects B2 error. 0: Does not detect.	0
D16	B1E	1: Detects B1 error. 0: Does not detect.	0
D15-D12	Reserved	Reserved	0
D11	SD	1: Detects occurrence of SD event. 0: Does not detect.	0
D10	SF	1: Detects occurrence of SF event. 0: Does not detect.	0
D9	CD	1: Detects low level of CD pin input. 0: Does not detect.	**Note**
D8	Reserved	Reserved	**Note**
D7	PSBF	1: Detects occurrence of PSBF event. 0: Does not detect.	0
D6	LRDI	1: Detects occurrence of Line RDI event. 0: Does not detect.	0
D5	LAIS	1: Detects occurrence of Line AIS event. 0: Does not detect.	1
D4	STIU	1: Detects occurrence of Section TIU event. 0: Does not detect.	0
D3	STIM	1: Detects occurrence of Section TIM event. 0: Does not detect.	0
D2	LOF	1: Detects occurrence of LOF event. 0: Does not detect.	1
D1	OOF	1: Detects occurrence of OOF event. 0: Does not detect.	1
D0	LOS	1: Detects occurrence of LOS event. 0: Does not detect.	0

Note: the default value of this register is depends on input level of the CD pin.

(79) Receive section and line layer event detection Read clear Enable registers (DSLER_RCE)

The DSLER registers is read clear enable register of the DSLER_RC register.

Register Name	Address				Access	Default	Function
	Port0:	Port1:	Port2:	Port3:			
DSLER_RCE	01C8 H	05C8 H	09C8 H	0DC8 H	R/W	3FF0FFF H	Read clear enable

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved						Z2M	Z2D	J0M	APS	LREICR	B2ECR	B1ECR	LREI	B2E	B1E

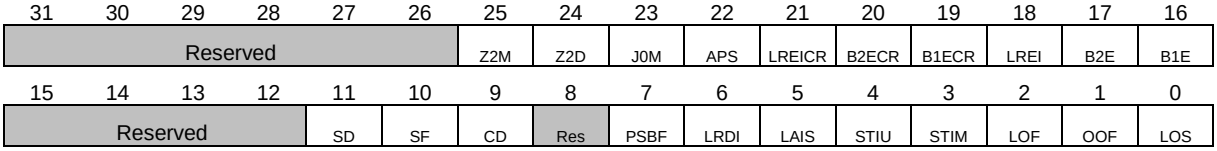
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved				SD	SF	CD	Res	PSBF	LRDI	LAIS	STIU	STIM	LOF	OOF	LOS

Bit	Field	Function	Default
D31-D26	Reserved	Reserved	All 0
D25	Z2M	1: Enable 0: Disable	1
D24	Z2D	1: Enable 0: Disable	1
D23	J0M	1: Enable 0: Disable	1
D22	APS	1: Enable 0: Disable	1
D21	LREICR	1: Enable 0: Disable	1
D20	B2ECR	1: Enable 0: Disable	1
D19	B1ECR	1: Enable 0: Disable	1
D18	LREI	1: Enable 0: Disable	1
D17	B2E	1: Enable 0: Disable	1
D16	B1E	1: Enable 0: Disable	1
D15-D12	Reserved	Reserved	All 0
D11	SD	1: Enable 0: Disable	1
D10	SF	1: Enable 0: Disable	1
D9	CD	1: Enable 0: Disable	1
D8	Reserved	Reserved	1
D7	PSBF	1: Enable 0: Disable	1
D6	LRDI	1: Enable 0: Disable	1
D5	LAIS	1: Enable 0: Disable	1
D4	STIU	1: Enable 0: Disable	1
D3	STIM	1: Enable 0: Disable	1
D2	LOF	1: Enable 0: Disable	1
D1	OOF	1: Enable 0: Disable	1
D0	LOS	1: Enable 0: Disable	1

(80) Receive section and line layer event detection Mask registers (DSLER_M)

The DSLER_M registers is mask register of DSLER register.

Register Name	Address				Access	Default	Function
	Port0:	Port1:	Port2:	Port3:			
DSLER_M	01CC H	05CC H	09CC H	0DCC H	R/W	3FF0FFF H	Mask register

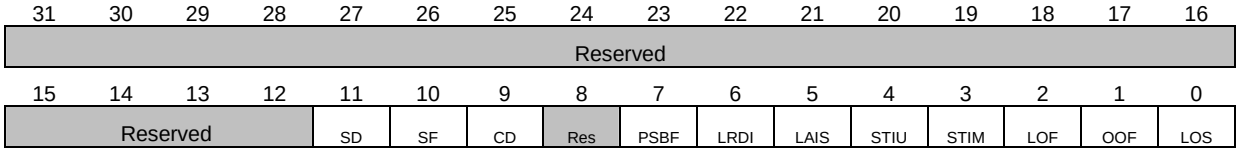


Bit	Field	Function		Default
D31-D26	Reserved	Reserved		All 0
D25	Z2M	1: Mask	0: Unmask	1
D24	Z2D	1: Mask	0: Unmask	1
D23	J0M	1: Mask	0: Unmask	1
D22	APS	1: Mask	0: Unmask	1
D21	LREICR	1: Mask	0: Unmask	1
D20	B2ECR	1: Mask	0: Unmask	1
D19	B1ECR	1: Mask	0: Unmask	1
D18	LREI	1: Mask	0: Unmask	1
D17	B2E	1: Mask	0: Unmask	1
D16	B1E	1: Mask	0: Unmask	1
D15-D12	Reserved	Reserved		All 0
D11	SD	1: Mask	0: Unmask	1
D10	SF	1: Mask	0: Unmask	1
D9	CD	1: Mask	0: Unmask	1
D8	Reserved	Set to 1.		1
D7	PSBF	1: Mask	0: Unmask	1
D6	LRDI	1: Mask	0: Unmask	1
D5	LAIS	1: Mask	0: Unmask	1
D4	STIU	1: Mask	0: Unmask	1
D3	STIM	1: Mask	0: Unmask	1
D2	LOF	1: Mask	0: Unmask	1
D1	OOF	1: Mask	0: Unmask	1
D0	LOS	1: Mask	0: Unmask	1

(81) Receive section and line layer event termination registers (TSLER)

This register indicates that an event has terminated.

Register Name	Address				Access	Default	Function
	Port0:	Port1:	Port2:	Port3:			
TSLER_RWC	01D0 H	05D0 H	09D0 H	0DD0 H	R/WC	**Note**	Read-only / Write clear
TSLER_RC	01D4 H	05D4 H	09D4 H	0DD4 H	RC	**Note**	Read clear



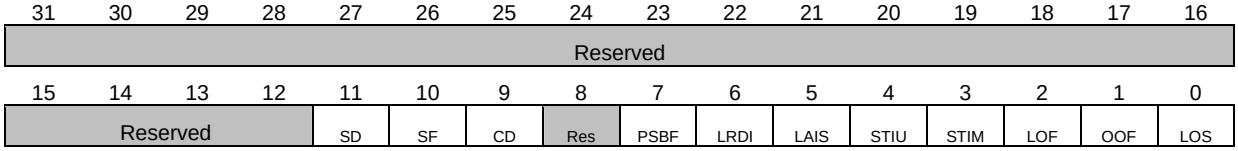
Bit	Field	Function	Default
D31-D12	Reserved	Reserved	All 0
D11	SD	1: Detects termination of SD event. 0: Does not detect.	0
D10	SF	1: Detects termination of SF event. 0: Does not detect.	0
D9	CD	1: Detects high level of CD pin input. 0: Does not detect.	**Note**
D8	Reserved	Reserved	**Note**
D7	PSBF	1: Detects termination of PSBF event. 0: Does not detect.	0
D6	LRDI	1: Detects termination of Line RDI event. 0: Does not detect.	0
D5	LAIS	1: Detects termination of Line AIS event. 0: Does not detect.	0
D4	STIU	1: Detects termination of Section TIU event. 0: Does not detect.	0
D3	STIM	1: Detects termination of Section TIM event. 0: Does not detect.	0
D2	LOF	1: Detects termination of LOF event. 0: Does not detect.	0
D1	OOF	1: Detects termination of OOF event. 0: Does not detect.	0
D0	LOS	1: Detects termination of LOS event. 0: Does not detect.	0

Note: the default value of this register is depends on the input level of the CD pin.

(82) Receive section and line layer event termination Read clear Enable registers (TSLER_RCE)

This register is read clear enable register of the TSLER_RC register.

Register Name	Address				Access	Default	Function
	Port0:	Port1:	Port2:	Port3:			
TSLER_RCE	01D8	05D8	09D8	0DD8	R/W	00000FFF h	Read clear enable

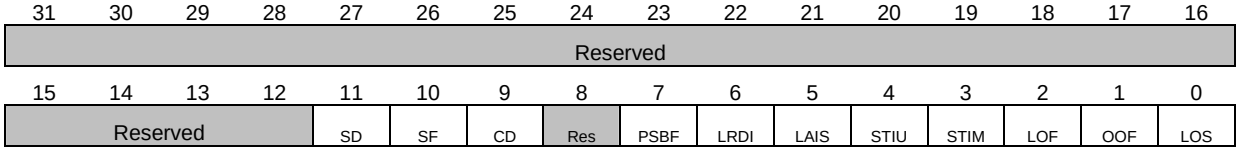


Bit	Field	Function	Default
D31-D12	Reserved	Set to 0.	All 0
D11	SD	1: enable 0: disable	1
D10	SF	1: enable 0: disable	1
D9	CD	1: enable 0: disable	1
D8	Reserved	Reserved	1
D7	PSBF	1: enable 0: disable	1
D6	LRDI	1: enable 0: disable	1
D5	LAIS	1: enable 0: disable	1
D4	STIU	1: enable 0: disable	1
D3	STIM	1: enable 0: disable	1
D2	LOF	1: enable 0: disable	1
D1	OOF	1: enable 0: disable	1
D0	LOS	1: enable 0: disable	1

(83) Receive section and line layer event termination Mask registers (TSLER_M)

This register is mask register of the TSLER register.

Register Name	Address				Access	Default	Function
	Port0:	Port1:	Port2:	Port3:			
TSLER_M	01DC	05DC	09DC	0DDC	R/W	00000FFFh	Mask register

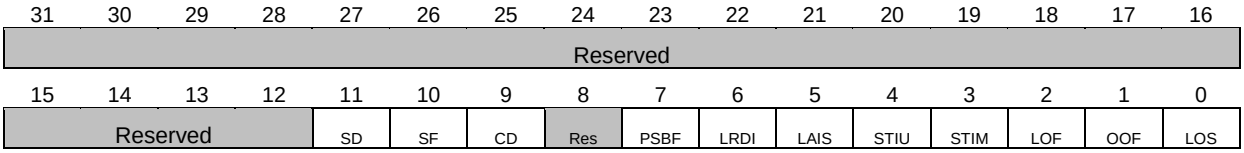


Bit	Field	Function	Default
D31-D12	Reserved	Reserved	All 0
D11	SD	1: mask 0: unmask	1
D10	SF	1: mask 0: unmask	1
D9	CD	1: mask 0: unmask	1
D8	Reserved	Set to 1.	1
D7	PSBF	1: mask 0: unmask	1
D6	LRDI	1: mask 0: unmask	1
D5	LAIS	1: mask 0: unmask	1
D4	STIU	1: mask 0: unmask	1
D3	STIM	1: mask 0: unmask	1
D2	LOF	1: mask 0: unmask	1
D1	OOF	1: mask 0: unmask	1
D0	LOS	1: mask 0: unmask	1

(84) Receive section and line layer event status register (SSLER)

This register indicates the current status of each event.

Register Name	Address				Access	Default	Function
	Port0:	Port1:	Port2:	Port3:			
SSLER	01F0	05F0	09F0	0DF0	R	**Note**	Read-only



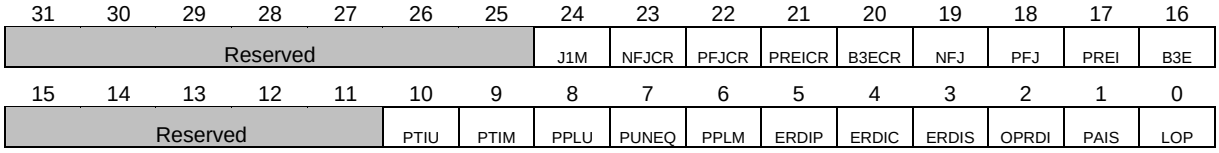
Bit	Field	Function		Default
D31-D12	Reserved	Reserved		All 0
D11	SD	1: SD event in progress	0: SD event is not detected.	0
D10	SF	1: SF event in progress	0: SF event is not detected.	0
D9	CD	1: The CD input is low.	0: The CD input is high.	**Note**
D8	Reserved	Reserved		**Note**
D7	PSBF	1: PSBF event in progress	0: PSBF event is not detected.	0
D6	LRDI	1: Line RDI event in progress	0: Line RDI event is not detected.	0
D5	LAIS	1: Line AIS event in progress	0: Line AIS event is not detected.	1
D4	STIU	1: Section TIU event in progress	0: Section TIU event is not detected.	0
D3	STIM	1: Section TIM event in progress	0: Section TIM event is not detected.	0
D2	LOF	1: LOF event in progress	0: LOF event is not detected.	1
D1	OOF	1: OOF event in progress	0: OOF event is not detected.	1
D0	LOS	1: LOS event in progress	0: LOS event is not detected.	0

Note: the default value of this register is depends on input level of the CD pin.

(85) Receive pointer and path layer event detection registers (DPPER)

The DPPER registers indicate whether the occurrence of each event was detected.

Register Name	Address				Access	Default	Function
	Port0:	Port1:	Port2:	Port3:			
DPPER_RWC	0200 H	0600 H	0A00 H	0E00 H	R/WC	00000002 h	Read-only / Write clear
DPPER_RC	0204 H	0604 H	0A04 H	0E04 H	RC	00000002 h	Read clear



Bit	Field	Function	Default
D31-D25	Reserved	Reserved	All 0
D24	J1M	1: Storing J1 message has been completed. 0: Not completed.	0
D23	NFJCR	1: Detects occurrence of an overflow in Negative FJ counter. 0: Dose not detect	0
D22	PFJCR	1: Detects occurrence of an overflow in Positive FJ counter. 0: Dose not detect	0
D21	PREICR	1: Detects occurrence of an overflow in Path REI counter. 0: Does not detect.	0
D20	B3ECR	1: Detects occurrence of an overflow in B3 error counter. 0: Does not detect.	0
D19	NFJ	1: Detects Negative Frequency Justification 0: Dose not detect	0
D18	PFJ	1: Detects Positive Frequency Justification 0: Dose not detect	0
D17	PREI	1: Detects Path REI. 0: Does not detect.	0
D16	B3E	1: Detects B3 error. 0: Does not detect.	0
D15-D11	Reserved	Reserved	All 0
D10	PTIU	1: Detects occurrence of Path TIU event. 0: Does not detect.	0
D9	PTIM	1: Detects occurrence of Path TIM event. 0: Does not detect.	0
D8	PPLU	1: Detects occurrence of Path PLU event. 0: Does not detect.	0
D7	PUNEQ	1: Detects occurrence of Path UNEQ event. 0: Does not detect.	0
D6	PPLM	1: Detects occurrence of Path PLM event. 0: Does not detect.	0
D5	ERDIP	1: Detects occurrence of Enhanced Path RDI Payload defect event. 0: Does not detect.	0
D4	ERDIC	1: Detects occurrence of Enhanced Path RDI Connectivity defect event. 0: Does not detect.	0
D3	ERDIS	1: Detects occurrence of Enhanced Path RDI Server defect event. 0: Does not detect.	0
D2	OPRDI	1: Detects occurrence of One-bit Path RDI event. 0: Does not detect.	0
D1	PAIS	1: Detects occurrence of Path AIS event. 0: Does not detect.	1
D0	LOP	1: Detects occurrence of LOP event. 0: Does not detect.	0

(86) Receive pointer and path layer event detection Read clear Enable registers (DPPER _RCE)

The DPPER registers is read clear enable register of the DPPER_RC register.

Register Name	Address				Access	Default	Function
	Port0:	Port1:	Port2:	Port3:			
DPPER_RCE	0208	0608	0A08	0E08	R/W	01FF07FF h	Read clear enable

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved							J1M	NFJCR	PFJCR	PREICR	B3ECR	NFJ	PFJ	PREI	B3E

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved					PTIU	PTIM	PPLU	PUNEQ	PPLM	ERDIP	ERDIC	ERDIS	OPRDI	PAIS	LOP

Bit	Field	Function		Default
D31-D25	Reserved	Reserved		All 0
D24	J1M	1: Enable	0: Disable	1
D23	NFJCR	1: Enable	0: Disable	1
D22	PFJCR	1: Enable	0: Disable	1
D21	PREICR	1: Enable	0: Disable	1
D20	B3ECR	1: Enable	0: Disable	1
D19	NFJ	1: Enable	0: Disable	1
D18	PFJ	1: Enable	0: Disable	1
D17	PREI	1: Enable	0: Disable	1
D16	B3E	1: Enable	0: Disable	1
D15-D11	Reserved	Reserved		All 0
D10	PTIU	1: Enable	0: Disable	1
D9	PTIM	1: Enable	0: Disable	1
D8	PPLU	1: Enable	0: Disable	1
D7	PUNEQ	1: Enable	0: Disable	1
D6	PPLM	1: Enable	0: Disable	1
D5	ERDIP	1: Enable	0: Disable	1
D4	ERDIC	1: Enable	0: Disable	1
D3	ERDIS	1: Enable	0: Disable	1
D2	OPRDI	1: Enable	0: Disable	1
D1	PAIS	1: Enable	0: Disable	1
D0	LOP	1: Enable	0: Disable	1

(87) Receive pointer and path layer event detection Mask registers (DPPER _M)

The DPPER registers is mask register of the MPPER register.

Register Name	Address				Access	Default	Function
	Port0:	Port1:	Port2:	Port3:			
DPPER_M	020C	060C	0A0C	0E0C	R/W	01FF07FF h	Mask register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved							J1M	NFJCR	PFJCR	PREICR	B3ECR	NFJ	PFJ	PREI	B3E

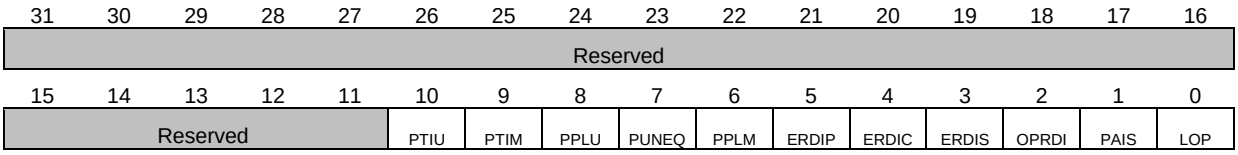
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved					PTIU	PTIM	PPLU	PUNEQ	PPLM	ERDIP	ERDIC	ERDIS	OPRDI	PAIS	LOP

Bit	Field	Function		Default
D31-D25	Reserved	Reserved		All 0
D24	J1M	1: mask	0: unmask	1
D23	NFJCR	1: mask	0: unmask	1
D22	PFJCR	1: mask	0: unmask	1
D21	PREICR	1: mask	0: unmask	1
D20	B3ECR	1: mask	0: unmask	1
D19	NFJ	1: mask	0: unmask	1
D18	PFJ	1: mask	0: unmask	1
D17	PREI	1: mask	0: unmask	1
D16	B3E	1: mask	0: unmask	1
D15-D11	Reserved	Reserved		All 0
D10	PTIU	1: mask	0: unmask	1
D9	PTIM	1: mask	0: unmask	1
D8	PPLU	1: mask	0: unmask	1
D7	PUNEQ	1: mask	0: unmask	1
D6	PPLM	1: mask	0: unmask	1
D5	ERDIP	1: mask	0: unmask	1
D4	ERDIC	1: mask	0: unmask	1
D3	ERDIS	1: mask	0: unmask	1
D2	OPRDI	1: mask	0: unmask	1
D1	PAIS	1: mask	0: unmask	1
D0	LOP	1: mask	0: unmask	1

(88) Receive pointer and path layer event termination registers (TPPER)

This register indicates that an event has terminated.

Register Name	Address				Access	Default	Function
	Port0:	Port1:	Port2:	Port3:			
TPPER_RWC	0210 H	0610 H	0A10 H	0E10 H	R/WC	00000000 H	Read-only / Write clear
TPPER_RC	0214 H	0614 H	0A14 H	0E14 H	RC	00000000 H	Read clear

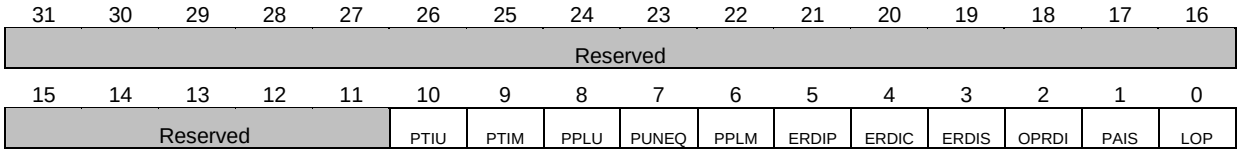


Bit	Field	Function	Default
D31-D11	Reserved	Reserved	0
D10	PTIU	1: Detects termination of Path TIU event. 0: Does not detect.	0
D9	PTIM	1: Detects termination of Path TIM event. 0: Does not detect.	0
D8	PPLU	1: Detects termination of Path PLU event. 0: Does not detect.	0
D7	PUNEQ	1: Detects termination of Path UNEQ event. 0: Does not detect.	0
D6	PPLM	1: Detects termination of Path PLM event. 0: Does not detect.	0
D5	ERDIP	1: Detects termination of Enhanced Path RDI Payload defect event. 0: Does not detect.	0
D4	ERDIC	1: Detects termination of Enhanced Path RDI Connectivity defect event. 0: Does not detect.	0
D3	ERDIS	1: Detects termination of Enhanced Path RDI Server defect event. 0: Does not detect.	0
D2	OPRDI	1: Detects termination of One-bit Path RDI event. 0: Does not detect.	0
D1	PAIS	1: Detects termination of Path AIS event. 0: Does not detect.	0
D0	LOP	1: Detects termination of LOP event. 0: Does not detect.	0

(89) Receive pointer and path layer event termination Read clear Enable registers (TPPER _RCE)

This register is read clear enable register of TPPER_RC register.

Register Name	Address				Access	Default	Function
	Port0:	Port1:	Port2:	Port3:			
TPPER_RCE	0218 H	0618 H	0A18 H	0E18 H	R/W	000007FF H	Read clear enable

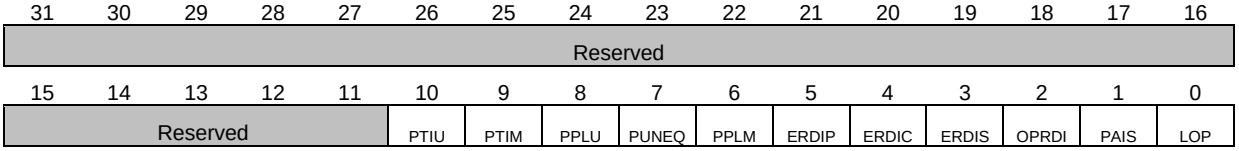


Bit	Field	Function	Default
D31-D11	Reserved	Set to 0.	0
D10	PTIU	1: Enable 0: Disable	1
D9	PTIM	1: Enable 0: Disable	1
D8	PPLU	1: Enable 0: Disable	1
D7	PUNEQ	1: Enable 0: Disable	1
D6	PPLM	1: Enable 0: Disable	1
D5	ERDIP	1: Enable 0: Disable	1
D4	ERDIC	1: Enable 0: Disable	1
D3	ERDIS	1: Enable 0: Disable	1
D2	OPRDI	1: Enable 0: Disable	1
D1	PAIS	1: Enable 0: Disable	1
D0	LOP	1: Enable 0: Disable	1

(90) Receive pointer and path layer event termination Mask registers (TPPER _M)

This register is mask register of TPPER register.

Register Name	Address				Access	Default	Function
	Port0:	Port1:	Port2:	Port3:			
TPPER_M	021C H	061C H	0A1C H	0E1C H	R/W	000007FF H	Mask register



Bit	Field	Function	Default
D31-D11	Reserved	Reserved	All 0
D10	PTIU	1: Mask 0: Unmask	1
D9	PTIM	1: Mask 0: Unmask	1
D8	PPLU	1: Mask 0: Unmask	1
D7	PUNEQ	1: Mask 0: Unmask	1
D6	PPLM	1: Mask 0: Unmask	1
D5	ERDIP	1: Mask 0: Unmask	1
D4	ERDIC	1: Mask 0: Unmask	1
D3	ERDIS	1: Mask 0: Unmask	1
D2	OPRDI	1: Mask 0: Unmask	1
D1	PAIS	1: Mask 0: Unmask	1
D0	LOP	1: Mask 0: Unmask	1

(91) Receive pointer and path layer event status register (SPPER)

This register indicates the current status of each event.

Register Name	Address				Access	Default	Function
	Port0:	Port1:	Port2:	Port3:			
SPPER	0230 H	0630 H	0A30 H	0E30 H	R	00000002 H	Read-only

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

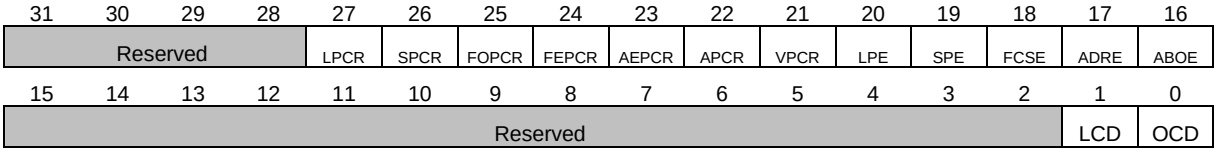
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved					PTIU	PTIM	PPLU	PUNEQ	PPLM	ERDIP	ERDIC	ERDIS	OPRDI	PAIS	LOP

Bit	Field	Function	Default
D31-D11	Reserved	Reserved	All 0
D10	PTIU	1: Path TIU event in progress 0: Path TIU event is not detected.	0
D9	PTIM	1: Path TIM event in progress 0: Path TIM event is not detected.	0
D8	PPLU	1: Path PLU event in progress 0: Path PLU event is not detected.	0
D7	PUNEQ	1: Path UNEQ event in progress 0: Path UNEQ event is not detected.	0
D6	PPLM	1: Path PLM event in progress 0: Path PLM event is not detected.	0
D5	ERDIP	1: Enhanced Path RDI Payload defect event in progress 0: Enhanced Path RDI Payload defect event is not detected.	0
D4	ERDIC	1: Enhanced Path RDI Connectivity defect event in progress 0: Enhanced Path RDI Connectivity defect event is not detected.	0
D3	ERDIS	1: Enhanced Path RDI Server defect event in progress 0: Enhanced Path RDI Server defect event is not detected.	0
D2	OPRDI	1: One-bit Path RDI event in progress 0: One-bit Path RDI event is not detected.	0
D1	PAIS	1: Path AIS event in progress 0: Path AIS event is not detected.	1
D0	LOP	1: LOP event in progress 0: LOP event is not detected.	0

(92) Receive ATM/POS layer event detection registers (DAPER)

The DAPER registers indicate whether the occurrence of each event was detected.

Register Name	Address				Access	Default	Function
	Port0:	Port1:	Port2:	Port3:			
DAPER_RWC	0240 H	0640 H	0A40 H	0E40 H	R/WC	00000003 H	Read-only / Write clear
DAPER_RC	0244 H	0644 H	0A44 H	0E44 H	RC	00000003 H	Read clear



Bit	Field	Function	Default
D31-D26	Reserved	Reserved.	0
D27	LPCR	1: Detects occurrence of an overflow in receive long packet counter. 0: Does not detect.	0
D26	SPCR	1: Detects occurrence of an overflow in receive short packet counter. 0: Does not detect.	0
D25	FOPCR	1: Detects occurrence of an overflow in receive FIFO overflow cell/packet counter. 0: Does not detect.	0
D24	FEPCR	1: Detects occurrence of an overflow in receive HEC error drop cell and FCS error packet counter. 0: Does not detect.	0
D23	AEPCR	1: Detects occurrence of an overflow in receive HEC error correct cell and address error packet counter. 0: Does not detect.	0
D22	APCR	1: Detects occurrence of an overflow in receive idle cell and abort packet counter. 0: Does not detect.	0
D21	VPCR	1: Detects occurrence of an overflow in receive valid cell/packet counter. 0: Does not detect.	0
D20	LPE	1: Detects occurrence of receive long packet. 0: Does not detect.	0
D19	SPE	1: Detects occurrence of receive short packet. 0: Does not detect.	0
D18	FCSE	1: Detects occurrence of receive FCS error. 0: Does not detect.	0
D17	ADRE	1: Detects occurrence of receive address error. 0: Does not detect.	0
D16	ABOE	1: Detects occurrence of receive abort packet. 0: Does not detect.	0
D15-D2	Reserved	Reserved.	0
D1	LCD	1: Detects occurrence of LCD event. 0: Does not detect.	1
D0	OCD	1: Detects occurrence of OCD event. 0: Does not detect.	1

(93) Receive ATM/POS layer event detection Read clear Enable registers (DAPER _RCE)

The DAPER_RCE register is read clear enable register of the DAPER_RC register.

Register Name	Address				Access	Default	Function
	Port0:	Port1:	Port2:	Port3:			
DAPER_RCE	0248 H	0648 H	0A48 H	0E48 H	R/W	7FFF0003 H	Read clear enable

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved				LPCR	SPCR	FOPCR	FEPCR	AEPCR	APCR	VPCR	LPE	SPE	FCSE	ADRE	ABOE

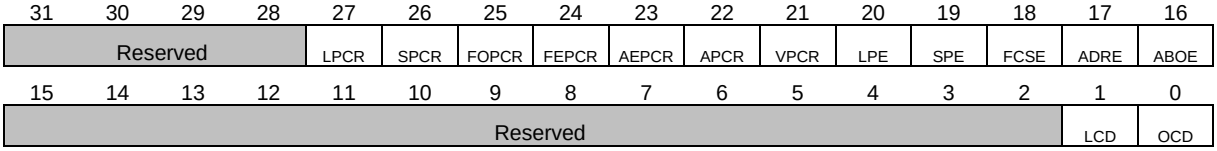
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved														LCD	OCD

Bit	Field	Function	Default
D31-D26	Reserved	Reserved.	All 0
D27	LPCR	1: Enable 0: Disable	1
D26	SPCR	1: Enable 0: Disable	1
D25	FOPCR	1: Enable 0: Disable	1
D24	FEPCR	1: Enable 0: Disable	1
D23	AEPCR	1: Enable 0: Disable	1
D22	APCR	1: Enable 0: Disable	1
D21	VPCR	1: Enable 0: Disable	1
D20	LPE	1: Enable 0: Disable	1
D19	SPE	1: Enable 0: Disable	1
D18	FCSE	1: Enable 0: Disable	1
D17	ADRE	1: Enable 0: Disable	1
D16	ABOE	1: Enable 0: Disable	1
D15-D2	Reserved	Reserved.	All 0
D1	LCD	1: Enable 0: Disable	1
D0	OCD	1: Enable 0: Disable	1

(94) Receive ATM/POS layer event detection Mask registers (DAPER _M)

The DAPER_M is mask register of the DAPER register.

Register Name	Address				Access	Default	Function
	Port0:	Port1:	Port2:	Port3:			
DAPER_M	024C H	064C H	0A4C H	0E4C H	R/W	7FFF0003 H	Mask register

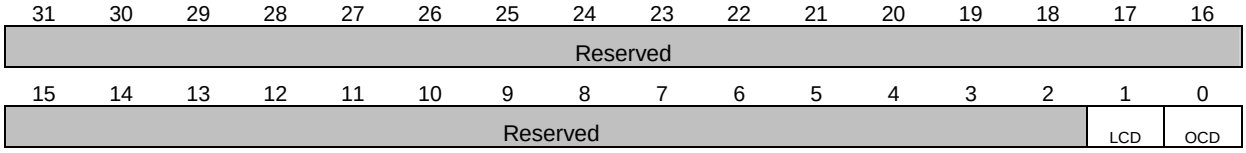


Bit	Field	Function	Default
D31-D26	Reserved	Set to 0.	All 0
D27	LPCR	1: Mask 0: Unmask	1
D26	SPCR	1: Mask 0: Unmask	1
D25	FOPCR	1: Mask 0: Unmask	1
D24	FEPCR	1: Mask 0: Unmask	1
D23	AEPCR	1: Mask 0: Unmask	1
D22	APCR	1: Mask 0: Unmask	1
D21	VPCR	1: Mask 0: Unmask	1
D20	LPE	1: Mask 0: Unmask	1
D19	SPE	1: Mask 0: Unmask	1
D18	FCSE	1: Mask 0: Unmask	1
D17	ADRE	1: Mask 0: Unmask	1
D16	ABOE	1: Mask 0: Unmask	1
D15-D2	Reserved	Set to 0.	All 0
D1	LCD	1: Mask 0: Unmask	1
D0	OCD	1: Mask 0: Unmask	1

(95) Receive ATM/POS layer event termination registers (TAPER)

This register indicates that an event has terminated.

Register Name	Address				Access	Default	Function
	Port0:	Port1:	Port2:	Port3:			
TAPER_RWC	0250 H	0650 H	0A50 H	0E50 H	R/WC	00000000 H	Read-only / Write clear
TAPER_RC	0254 H	0654 H	0A54 H	0E54 H	RC	00000000 H	Read clear

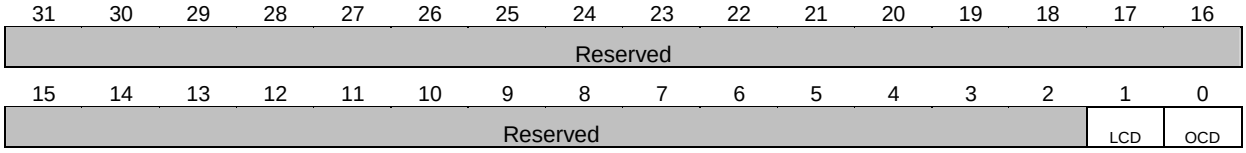


Bit	Field	Function	Default
D31-D2	Reserved	Reserved	All 0
D1	LCD	1: Detects termination of LCD event. 0: Does not detect.	0
D0	OCD	1: Detects termination of OCD event. 0: Does not detect.	0

(96) Receive ATM/POS layer event termination Read clear Enable registers (TAPER _RCE)

This register is read clear enable register of the TAPER_RC register.

Register Name	Address				Access	Default	Function
	Port0:	Port1:	Port2:	Port3:			
TAPER_RCE	0258 H	0658 H	0A58 H	0E58 H	R/W	00000003 H	Read clear enable

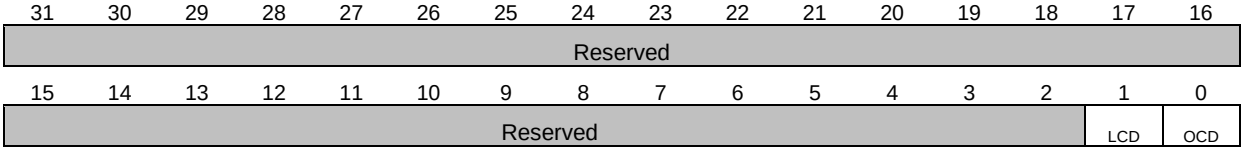


Bit	Field	Function	Default
D31-D2	Reserved	Set to 0.	All 0
D1	LCD	1: Enable 0:Disable	1
D0	OCD	1: Enable 0:Disable	1

(97) Receive ATM/POS layer event termination Mask registers (TAPER _M)

This register is mask register of TAPER register.

Register Name	Address				Access	Default	Function
	Port0:	Port1:	Port2:	Port3:			
TAPER_M	025C H	065C H	0A5C H	0E5C H	R/W	00000003 H	Mask register

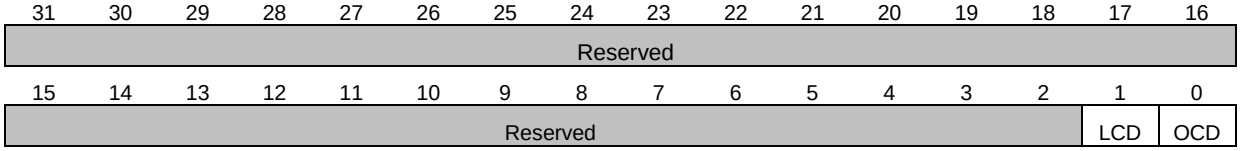


Bit	Field	Function	Default
D31-D2	Reserved	Set to 0.	All 0
D1	LCD	1: Mask 0:Unmask	1
D0	OCD	1: Mask 0:Unmask	1

(98) Receive ATM/POS layer event status registers (SAPER)

This register indicates the current status of each event.

Register Name	Address				Access	Default	Function
	Port0:	Port1:	Port2:	Port3:			
SAPER	0270 H	0670 H	0A70 H	0E70 H	R	00000003 H	Read-only

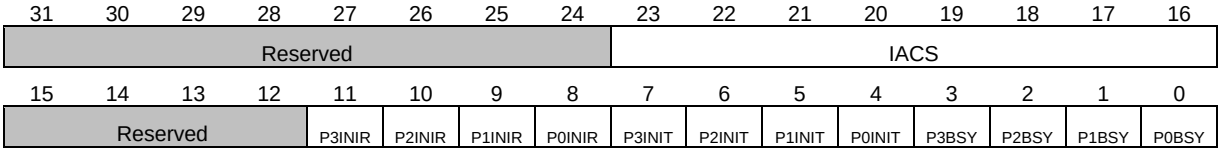


Bit	Field	Function	Default
D31-D2	Reserved	Reserved	All 0
D1	LCD	1: LCD event in progress 0: LCD event is not detected.	1
D0	OCD	1: OCD event in progress 0: OCD event is not detected.	1

(99) General event detection register (DGE) Common register

The DGE register indicates the causes of the general event.

Register Name	Address	Access	Default	Function
DGE_RWC	0280 H	R/WC	00000FF0 H	Read-only / Write clear
DGE_RC	0284 H	RC	00000FF0 H	Read clear



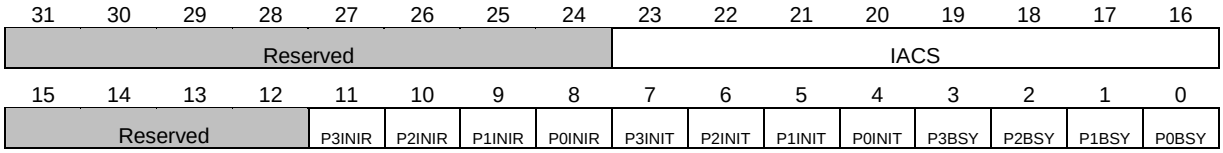
Bit	Field	Function	Default
D31-D17	Reserved	Reserved	All 0
D16	IACS	1: Detects an illegal access to undefined address. 0: Does not detect.	0
D15-D12	Reserved	Reserved	All 0
D11	P3INIR	1: Detects that the receive function of port3 is initialized due to port reset. 0: Does not detect.	1
D10	P2INIR	1: Detects that the receive function of port2 is initialized due to port reset. 0: Does not detect.	1
D9	P1INIR	1: Detects that the receive function of port1 is initialized due to port reset. 0: Does not detect.	1
D8	P0INIR	1: Detects that the receive function of port0 is initialized due to port reset. 0: Does not detect.	1
D7	P3INIT	1: Detects that the transmit function of port3 is initialized due to port reset. 0: Does not detect.	1
D6	P2INIT	1: Detects that the transmit function of port2 is initialized due to port reset. 0: Does not detect.	1
D5	P1INIT	1: Detects that the transmit function of port1 is initialized due to port reset. 0: Does not detect.	1
D4	P0INIT	1: Detects that the transmit function of port0 is initialized due to port reset. 0: Does not detect.	1
D3	P3BSY	1: Detects that the receive function of port3 is busy due to port enable. 0: Does not detect.	0
D2	P2BSY	1: Detects that the receive function of port2 is busy due to port enable. 0: Does not detect.	0
D1	P1BSY	1: Detects that the receive function of port1 is busy due to port enable. 0: Does not detect.	0
D0	P0BSY	1: Detects that the receive function of port0 is busy due to port enable. 0: Does not detect.	0

Note: the default value of this register is depends on General event.

(100) General event detection Read clear Enable register (DGE _RCE) Common register

The DGE register is read clear enable register of DGE_RC register.

Register Name	Address	Access	Default	Function
DGE_RCE	0288 H	R/W	00010FFF H	Read clear enable

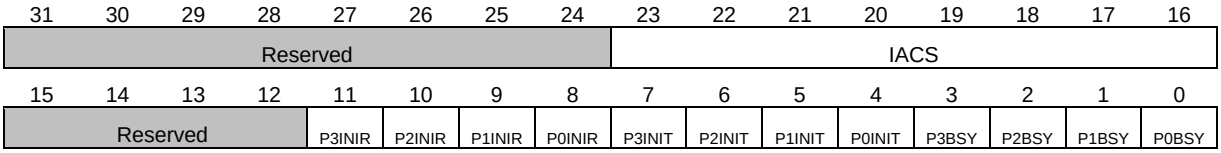


Bit	Field	Function	Default
D31-D17	Reserved	Set to 0.	0
D16	IACS	1: Enable 0:Disable	1
D15-D12	Reserved	Set to 0.	0
D11	P3INIR	1: Enable 0:Disable	1
D10	P2INIR	1: Enable 0:Disable	1
D9	P1INIR	1: Enable 0:Disable	1
D8	P0INIR	1: Enable 0:Disable	1
D7	P3INIT	1: Enable 0:Disable	1
D6	P2INIT	1: Enable 0:Disable	1
D5	P1INIT	1: Enable 0:Disable	1
D4	P0INIT	1: Enable 0:Disable	1
D3	P3BSY	1: Enable 0:Disable	1
D2	P2BSY	1: Enable 0:Disable	1
D1	P1BSY	1: Enable 0:Disable	1
D0	P0BSY	1: Enable 0:Disable	1

(101) General event detection Mask register (DGE _M) Common register

The DGE register is mask register of DGE register.

Register Name	Address	Access	Default	Function
DGE_M	028C H	R/W	00010FFF H	Mask register

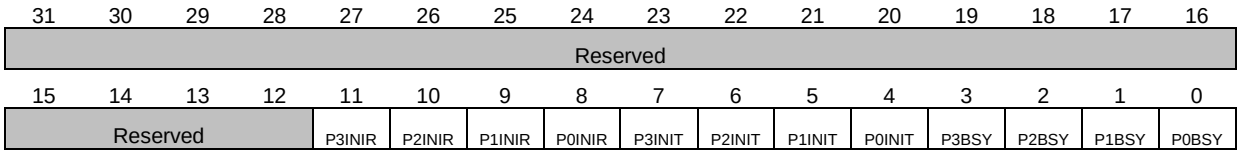


Bit	Field	Function	Default
D31-D17	Reserved	Set to 0.	0
D16	IACS	1: Mask 0: Unmask	1
D15-D12	Reserved	1: Mask 0: Unmask	1
D11	P3INIR	Set to 0.	0
D10	P2INIR	1: Mask 0: Unmask	1
D9	P1INIR	1: Mask 0: Unmask	1
D8	P0INIR	1: Mask 0: Unmask	1
D7	P3INIT	1: Mask 0: Unmask	1
D6	P2INIT	1: Mask 0: Unmask	1
D5	P1INIT	1: Mask 0: Unmask	1
D4	P0INIT	1: Mask 0: Unmask	1
D3	P3BSY	1: Mask 0: Unmask	1
D2	P2BSY	1: Mask 0: Unmask	1
D1	P1BSY	1: Mask 0: Unmask	1
D0	P0BSY	1: Mask 0: Unmask	1

(102) General event termination register (TGE) Common register

The TGE register indicates the causes of the general event.

Register Name	Address	Access	Default	Function
TGE_RWC	0290	R/WC	00000000 H	Read-only / Write clear
TGE_RC	0294	RC	00000000 H	Read clear

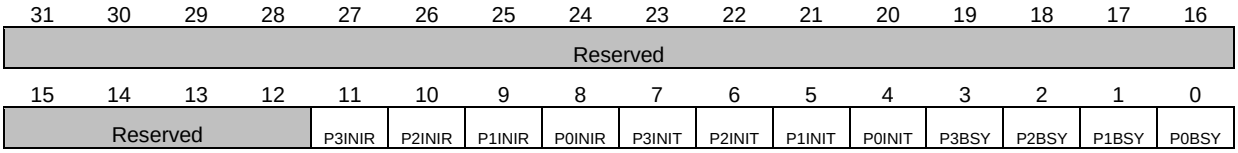


Bit	Field	Function	Default
D31-D12	Reserved	Reserved	All 0
D11	P3INIR	1: Detects that the initialization of the receive function of port3 is completed. 0: Does not detect.	0
D10	P2INIR	1: Detects that the initialization of the receive function of port2 is completed. 0: Does not detect.	0
D9	P1INIR	1: Detects that the initialization of the receive function of port1 is completed. 0: Does not detect.	0
D8	P0INIR	1: Detects that the initialization of the receive function of port0 is completed. 0: Does not detect.	0
D7	P3INIT	1: Detects that the initialization of the transmit function of port3 is completed. 0: Does not detect.	0
D6	P2INIT	1: Detects that the initialization of the transmit function of port2 is completed. 0: Does not detect.	0
D5	P1INIT	1: Detects that the initialization of the transmit function of port1 is completed. 0: Does not detect.	0
D4	P0INIT	1: Detects that the initialization of the transmit function of port0 is completed. 0: Does not detect.	0
D3	P3BSY	1: Detects that the receive function of port3 is not busy due to port disable. 0: Does not detect.	0
D2	P2BSY	1: Detects that the receive function of port2 is not busy due to port disable. 0: Does not detect.	0
D1	P1BSY	1: Detects that the receive function of port1 is not busy due to port disable. 0: Does not detect.	0
D0	P0BSY	1: Detects that the receive function of port0 is not busy due to port disable. 0: Does not detect.	0

(103) General event termination Read Clear Enable register (TGE_RCE) Common register

The TGE register is read clear enable register of TGE_RC register.

Register Name	Address	Access	Default	Function
TGE_RCE	0298 H	R/W	00000FFF H	Read clear enable

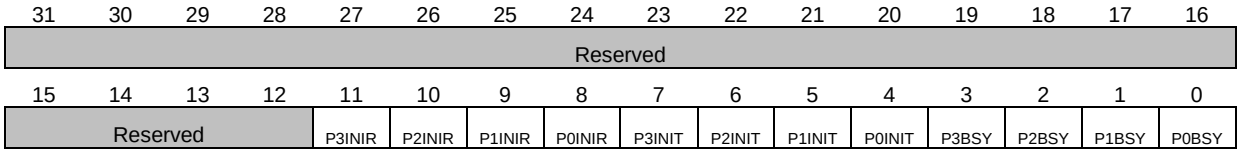


Bit	Field	Function	Default
D31-D12	Reserved	Set to 0.	0
D11	P3INIR	1: Enable 0:Disable	1
D10	P2INIR	1: Enable 0:Disable	1
D9	P1INIR	1: Enable 0:Disable	1
D8	P0INIR	1: Enable 0:Disable	1
D7	P3INIT	1: Enable 0:Disable	1
D6	P2INIT	1: Enable 0:Disable	1
D5	P1INIT	1: Enable 0:Disable	1
D4	P0INIT	1: Enable 0:Disable	1
D3	P3BSY	1: Enable 0:Disable	1
D2	P2BSY	1: Enable 0:Disable	1
D1	P1BSY	1: Enable 0:Disable	1
D0	P0BSY	1: Enable 0:Disable	1

(104) General event termination Mask register (TGE_M) Common register

The TGE register is mask register of TGE register.

Register Name	Address	Access	Default	Function
TGE_M	029C	R/W	00000FFF	Mask register

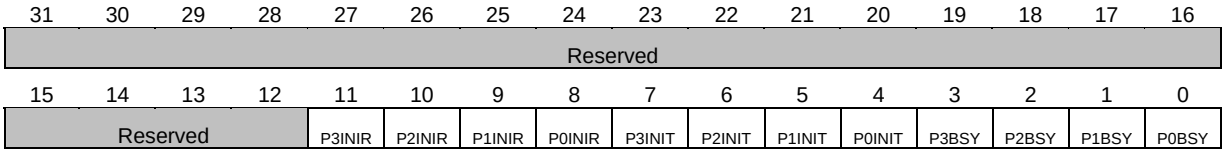


Bit	Field	Function	Default
D31-D12	Reserved	Set to 0.	0
D11	P3INIR	1: Mask 0: Unmask	1
D10	P2INIR	1: Mask 0: Unmask	1
D9	P1INIR	1: Mask 0: Unmask	1
D8	P0INIR	1: Mask 0: Unmask	1
D7	P3INIT	1: Mask 0: Unmask	1
D6	P2INIT	1: Mask 0: Unmask	1
D5	P1INIT	1: Mask 0: Unmask	1
D4	P0INIT	1: Mask 0: Unmask	1
D3	P3BSY	1: Mask 0: Unmask	1
D2	P2BSY	1: Mask 0: Unmask	1
D1	P1BSY	1: Mask 0: Unmask	1
D0	P0BSY	1: Mask 0: Unmask	1

(105) General event status register (SGE) Common register

The SGE register indicates the causes of the general event.

Register Name	Address	Access	Default	Function
SGE	02A0 H	R	00000FF0 H	Read-only

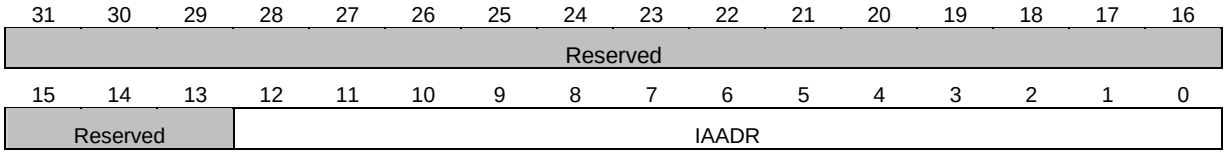


Bit	Field	Function	Default
D31-D12	Reserved	Reserved	0
D11	P3INIR	1: The receive function of port3 is under initialization. 0: The receive function of port3 is not under initialization.	1
D10	P2INIR	1: The receive function of port2 is under initialization. 0: The receive function of port2 is not under initialization.	1
D9	P1INIR	1: The receive function of port1 is under initialization. 0: The receive function of port1 is not under initialization.	1
D8	P0INIR	1: The receive function of port0 is under initialization. 0: The receive function of port0 is not under initialization.	1
D7	P3INIT	1: The transmit function of port3 is under initialization. 0: The transmit function of port3 is not under initialization.	1
D6	P2INIT	1: The transmit function of port2 is under initialization. 0: The transmit function of port2 is not under initialization.	1
D5	P1INIT	1: The transmit function of port1 is under initialization. 0: The transmit function of port1 is not under initialization.	1
D4	P0INIT	1: The transmit function of port0 is under initialization. 0: The transmit function of port0 is not under initialization.	1
D3	P3BSY	1: The receive function of port3 is busy. 0: The receive function of port3 is not busy.	0
D2	P2BSY	1: The receive function of port2 is busy. 0: The receive function of port2 is not busy.	0
D1	P1BSY	1: The receive function of port1 is busy. 0: The receive function of port1 is not busy.	0
D0	P0BSY	1: The receive function of port0 is busy. 0: The receive function of port0 is not busy.	0

(106) Illegal access address register (IAADR) Common register

The IAADR register indicates the address of the illegal access.

Register Name	Address	Access	Default
IAADR	02A4 H	R	00000000 H

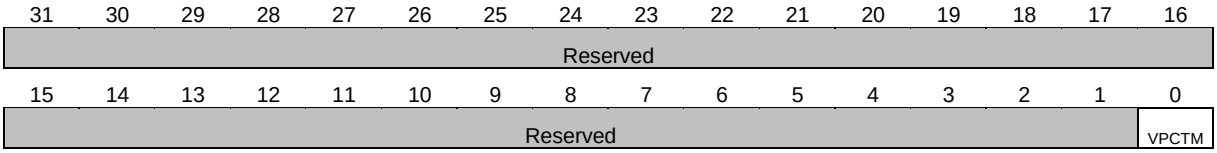


Bit	Field	Function	Default
D31-D13	Reserved	Reserved	All 0
D12-D0	IAADR	Indicates the address of the illegal access.	0000 H

(107) Transmit counter mode register (MDCNTT)

The MDCNTT register sets the modes related to operation of the performance monitoring counter.

Register Name	Address				Access	Default
	Port0:	Port1:	Port2:	Port3:		
MDCNTT	02C0 H	06C0 H	0AC0 H	0EC0 H	R/W	00000000 H

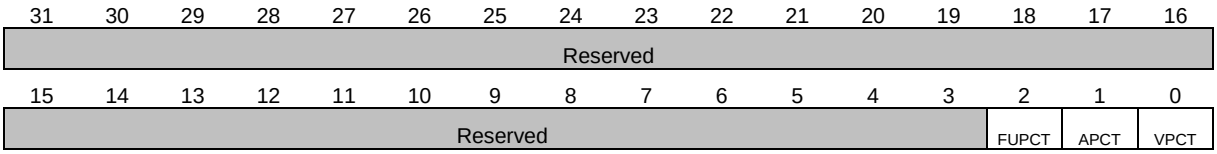


Bit	Field	Function	Default
D31-D1	Reserved	Set to 0.	0
D0	VPCTM	Selects the number of the valid packets or bytes counted by transmit valid packet counter. 1: Number of bytes 0: Number of packets	0

(108) Transmit counter sampling register (CSMPT)

This register specifies a command that saves the counter value of the performance monitoring counter to the corresponding load register.

Register Name	Address				Access	Default
	Port0:	Port1:	Port2:	Port3:		
CSMPT	02C4 H	06C4 H	0AC4 H	0EC4 H	R/W	00000000 H



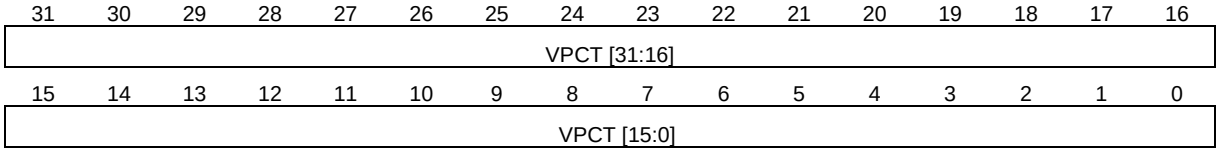
Bit	Field	Function	Default
D31-D3	Reserved	Set to 0.	0
D2	FUPCT	1: Loads the transmit FIFO underflow packet counter. 0: Indicates completion of loading.	0
D1	APCT	1: Loads the transmit abort packet counter. 0: Indicates completion of loading.	0
D0	VPCT	ATM mode: 1: Loads the valid transmit cell counter. 0: Indicates completion of loading. POS mode: 1: Loads the valid transmit packet counter. 0: Indicates completion of loading.	0

(109) Transmit valid cell/packet counter load register (VPCT)

ATM mode:
This register reads the transmit valid cell counter value.

POS mode:
This register reads the transmit valid packet counter value. This count is selected from the number of valid packets or bytes for POS mode.

Register Name	Address				Access	Default
	Port0:	Port1:	Port2:	Port3:		
VPCT	02C8 H	06C8 H	0AC8 H	0EC8 H	R	00000000 H

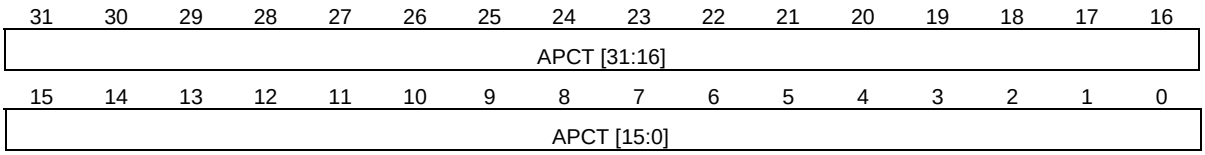


Bit	Field	Function	Default
D31-D0	VPCT	Transmit valid cell/packet counter.	0

(110) Transmit abort packet counter load register (APCT)

POS mode:
This register reads the transmit abort packet counter value.

Register Name	Address				Access	Default
	Port0:	Port1:	Port2:	Port3:		
APCT	02CC H	06CC H	0ACC H	0ECC H	R	00000000 H



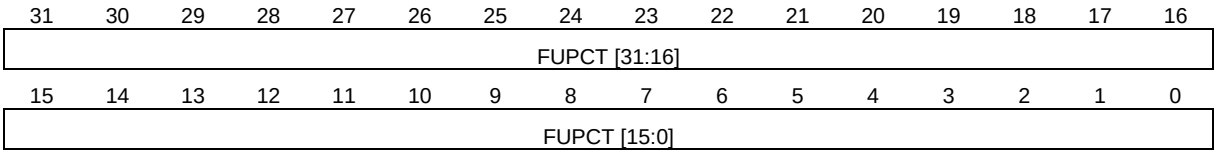
Bit	Field	Function	Default
D31-D0	APCT	Transmit abort packet counter.	0

(111) Transmit FIFO underflow packet counter load register (FUPCT)

POS mode:

This register reads the transmit FIFO underflow packet counter value.

Register Name	Address				Access	Default
	Port0:	Port1:	Port2:	Port3:		
FUPCT	02D0 H	06D0 H	0AD0 H	0ED0 H	R	00000000 H

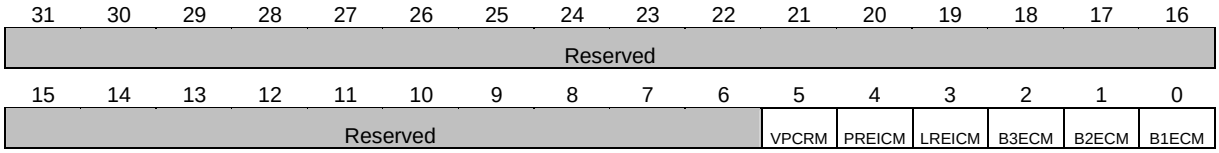


Bit	Field	Function	Default
D31-D0	FUPCT	Transmit FIFO underflow packet counter.	0

(112) Receive counter mode register (MDCNTR)

The MDCNTR register sets the modes related to operation of the performance-monitoring counter.

Register Name	Address				Access	Default
	Port0:	Port1:	Port2:	Port3:		
MDCNTR	02D4 H	06D4 H	0AD4 H	0ED4 H	R/W	00000000 H

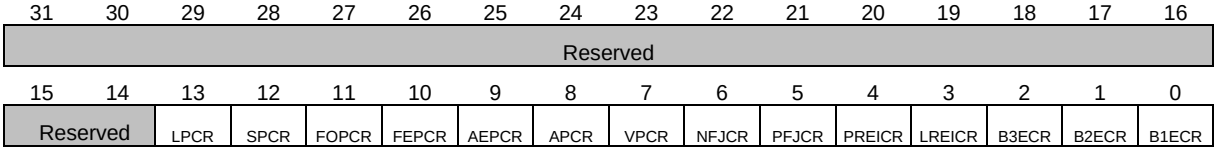


Bit	Field	Function	Default
D31-D6	Reserved	Set to 0.	0
D5	VPCRM	Selects the number of the valid packets or bytes counted by receive valid packet counter. 1: Number of bytes 0: Number of packets	0
D4	PREICRM	Selects the number of the error bits or frames counted by Path REI counter. 1: Number of error frames 0: Number of error bits	0
D3	LREICRM	Selects the number of the error bits or frames counted by Line REI counter. 1: Number of error frames 0: Number of error bits	0
D2	B3ECRM	Selects the number of the error bits or frames counted by B3 error counter. 1: Number of error frames 0: Number of error bits	0
D1	B2ECRM	Selects the number of the error bits or frames counted by B2 error counter. 1: Number of error frames 0: Number of error bits	0
D0	B1ECRM	Selects the number of the error bits or frames counted by B1 error counter. 1: Number of error frames 0: Number of error bits	0

(113) Receive counter sampling register (CSMPR)

This register specifies a command that saves the counter value of the performance monitoring counter to the corresponding load register.

Register Name	Address				Access	Default
	Port0:	Port1:	Port2:	Port3:		
CSMPR	02D8 H	06D8 H	0AD8 H	0ED8 H	R/W	00000000 H



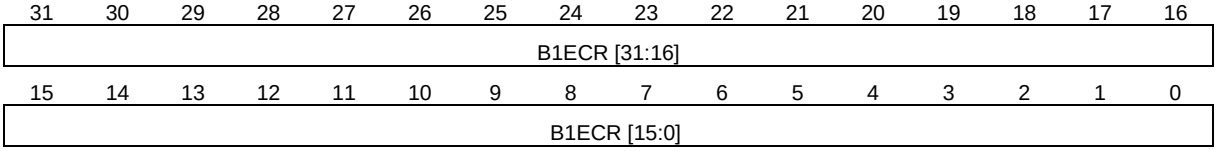
Bit	Field	Function	Default
D31-D14	Reserved	Set to 0.	0
D13	LPCR	1: Loads the receive long packet counter. 0: Indicates completion of loading.	0
D12	SPCR	1: Loads the receive short packet counter. 0: Indicates completion of loading.	0
D11	FOPCR	ATM mode: 1: Loads the receive FIFO overflow cell counter. 0: Indicates completion of loading. POS mode: 1: Loads the receive FIFO overflow packet counter. 0: Indicates completion of loading.	0
D10	FEPCR	ATM mode: 1: Loads the HEC error drop cell counter. 0: Indicates completion of loading. POS mode: 1: Loads the receive FCS error packet counter. 0: Indicates completion of loading.	0
D9	AEPCR	ATM mode: 1: Loads the HEC error correct cell counter. 0: Indicates completion of loading. POS mode: 1: Loads the receive address error packet counter. 0: Indicates completion of loading.	0
D8	APCR	ATM mode: 1: Loads the receive idle cell counter. 0: Indicates completion of loading. POS mode: 1: Loads the receive abort packet counter. 0: Indicates completion of loading.	0
D7	VPCR	ATM mode: 1: Loads the valid receive cell counter. 0: Indicates completion of loading. POS mode: 1: Loads the valid receive packet counter. 0: Indicates completion of loading.	0
D6	NFJCR	1: Loads the Negative Frequency Justification counter 0: Indicates completion of loading.	
D5	PFJCR	1: Loads the Positive Frequency Justification counter 0: Indicates completion of loading.	

D4	PREICR	1: Loads the path REI counter. 0: Indicates completion of loading.	0
D3	LREICR	1: Loads the line REI counter. 0: Indicates completion of loading.	0
D2	B3ECR	1: Loads the B3 error counter. 0: Indicates completion of loading.	0
D1	B2ECR	1: Loads the B2 error counter. 0: Indicates completion of loading.	0
D0	B1ECR	1: Loads the B1 error counter. 0: Indicates completion of loading.	0

(114) B1 error counter load register (B1ECR)

This register reads the B1 error counter value. B1 error count is selected from the number of error bits or frames.

Register Name	Address				Access	Default
	Port0:	Port1:	Port2:	Port3:		
B1ECR	02DC H	06DC H	0ADC H	0EDC H	R	00000000 H

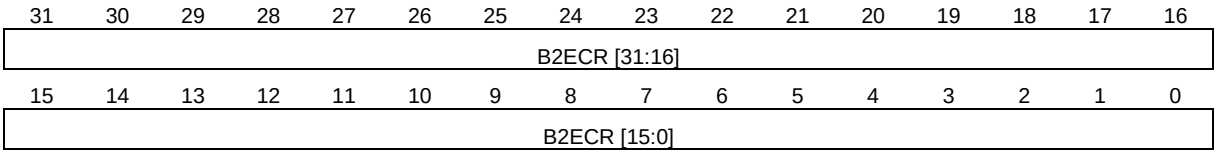


Bit	Field	Function	Default
D31-D0	B1ECR	B1 error counter.	0

(115) B2 error counter load register (B2ECR)

This register reads the B2 error counter value. B2 error count is selected from the number of error bits or frames.

Register Name	Address				Access	Default
	Port0:	Port1:	Port2:	Port3:		
B2ECR	02E0 H	06E0 H	0AE0 H	0EE0 H	R	00000000H

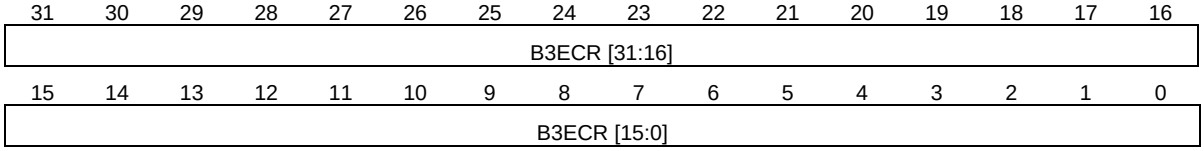


Bit	Field	Function	Default
D31-D0	B2ECR	B2 error counter.	0

(116) B3 error counter load register (B3ECR)

This register reads the B3 error counter value. B3 error count is selected from the number of error bits or frames.

Register Name	Address				Access	Default
	Port0:	Port1:	Port2:	Port3:		
B3ECR	02E4 H	06E4 H	0AE4 H	0EE4 H	R	00000000 H

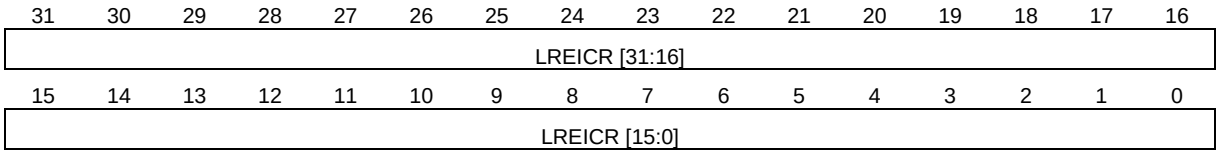


Bit	Field	Function	Default
D31-D0	B3ECR	B3 error counter.	0

(117) Line REI counter load register (LREICR)

This register reads the Line REI counter value. Line REI count is selected from the number of error bits or frames.

Register Name	Address				Access	Default
	Port0:	Port1:	Port2:	Port3:		
LREICR	02E8 H	06E8 H	0AE8 H	0EE8 H	R	00000000 H

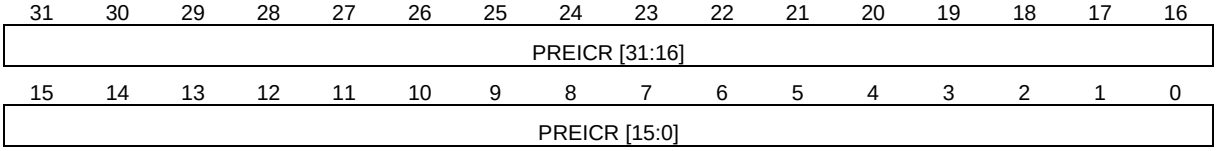


Bit	Field	Function	Default
D31-D0	LREICR	Line REI counter.	0

(118) Path REI counter load register (PREICR)

This register reads the Path REI counter value. Path REI count is selected from the number of error bits or frames.

Register Name	Address				Access	Default
	Port0:	Port1:	Port2:	Port3:		
PREICR	02EC H	06EC H	0AEC H	0EEC H	R	00000000 H

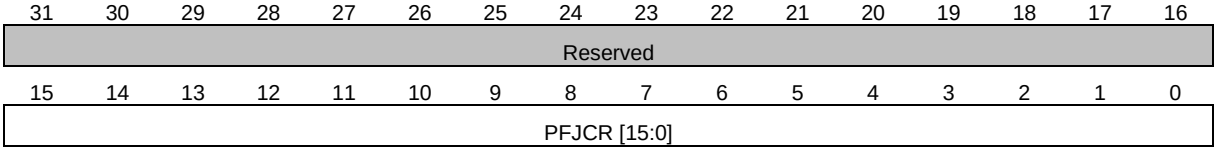


Bit	Field	Function	Default
D31-D0	PREICR	Path REI counter.	0

(119) Positive Frequency Justification counter load register (PFJCR)

This register reads the Positive Frequency Justification counter value.

Register Name	Address				Access	Default
	Port0:	Port1:	Port2:	Port3:		
PFJCR	02F0 H	06F0 H	0AF0 H	0EF0 H	R	00000000H

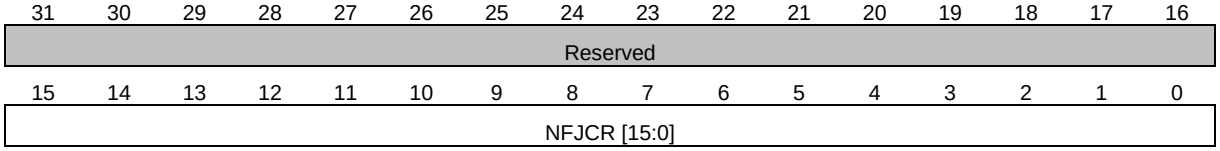


Bit	Field	Function	Default
D31-D16	Reserved		0
D15-D0	PFJCR	Positive Frequency Justification counter.	0

(120) Negative Frequency Justification counter load register (NFJCR)

This register reads the Negative Frequency Justification counter value.

Register Name	Address				Access	Default
	Port0:	Port1:	Port2:	Port3:		
NFJCR	02F4 H	06F4 H	0AF4 H	0EF4 H	R	00000000 H



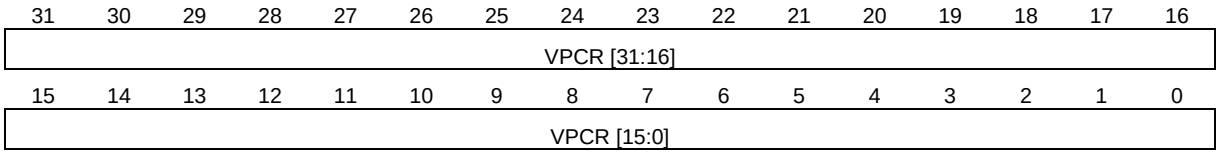
Bit	Field	Function	Default
D31-D16	Reserved		0
D15-D0	NFJCR	Negative Frequency Justification counter.	0

(121) Receive valid cell/packet counter load register (VPCR)

ATM mode:
This register reads the receive valid cell counter value.

POS mode:
This register reads the receive valid packet counter value. This count is selected from the number of valid packets or bytes for POS mode.

Register Name	Address				Access	Default
	Port0:	Port1:	Port2:	Port3:		
VPCR	02F8 H	06F8 H	0AF8 H	0EF8 H	R	00000000 H



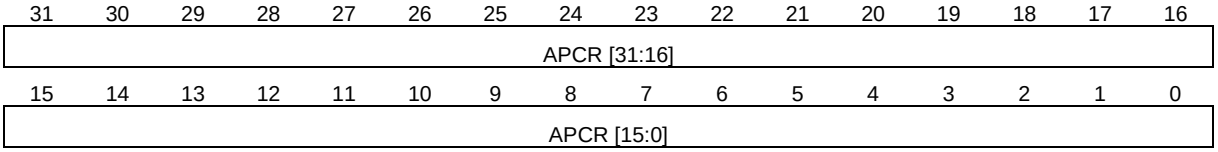
Bit	Field	Function	Default
D31-D0	VPCR	Receive valid cell/packet counter.	0

(122) Receive idle cell and abort packet counter load register (APCR)

ATM mode:
This register reads the receive idle cell counter value.

POS mode:
This register reads the receive abort packet counter value.

Register Name	Address				Access	Default
	Port0:	Port1:	Port2:	Port3:		
APCR	02FC H	06FC H	0AFC H	0EFC H	R	00000000 H



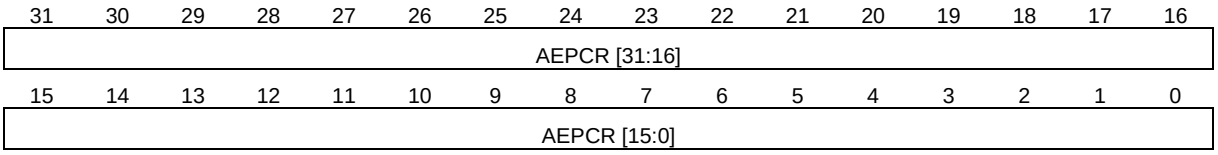
Bit	Field	Function	Default
D31-D0	APCR	Receive idle cell and abort packet counter.	0

(123) Receive HEC error correct cell and address error packet counter load register (AEPCR)

ATM mode:
This register reads the receive HEC error correct cell counter value.

POS mode:
This register reads the receive address error packet counter value.

Register Name	Address				Access	Default
	Port0:	Port1:	Port2:	Port3:		
AEPCR	0300 H	0700 H	0B00 H	0F00 H	R	00000000 H



Bit	Field	Function	Default
D31-D0	AEPCR	Receive HEC error correct cell and address error packet counter.	0

(124) Receive HEC error drop cell and FCS error packet counter load register (FEPCR)

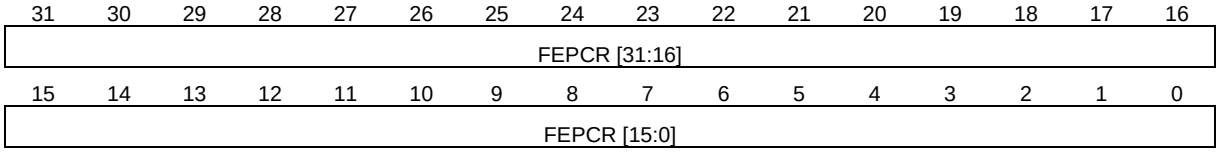
ATM mode:

This register reads the receive HEC error drop cell counter value.

POS mode:

This register reads the receive FCS error packet counter value.

Register Name	Address				Access	Default
	Port0:	Port1:	Port2:	Port3:		
FEPCR	0304	0704	0B04	0F04	R	00000000H



Bit	Field	Function	Default
D31-D0	FEPCR	Receive HEC error drop cell and FCS error packet counter.	0

(125) Receive FIFO overflow cell/packet counter load register (FOPCR)

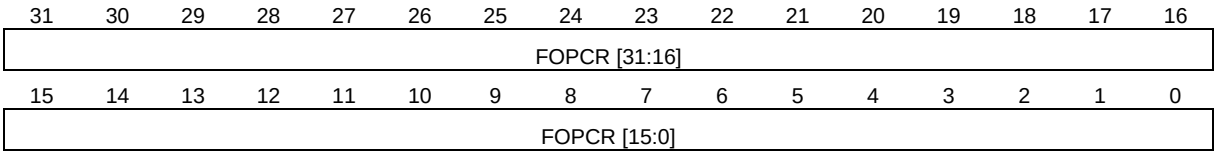
ATM mode:

This register reads the receive FIFO overflow cell counter value.

POS mode:

This register reads the receive FIFO overflow packet counter value.

Register Name	Address				Access	Default
	Port0:	Port1:	Port2:	Port3:		
FOPCR	0308 H	0708 H	0B08 H	0F08 H	R	00000000 H



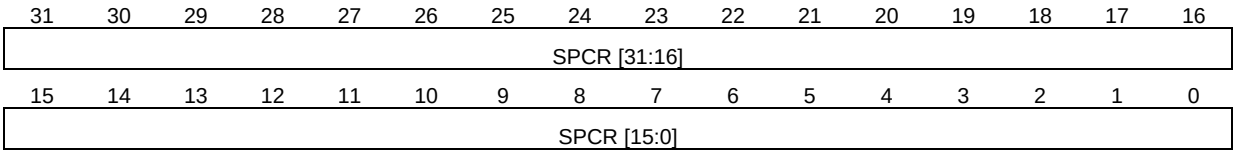
Bit	Field	Function	Default
D31-D0	FOPCR	Receive FIFO overflow cell/packet counter.	0

(126) Receive short packet counter load register (SPCR)

POS mode:

This register reads the receive short packet counter value.

Register Name	Address				Access	Default
	Port0:	Port1:	Port2:	Port3:		
SPCR	030C H	070C H	0B0C H	0F0C H	R	00000000 H



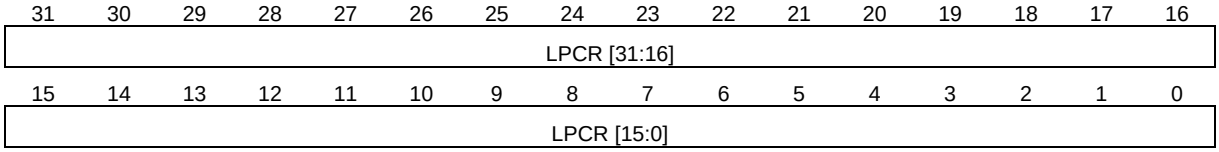
Bit	Field	Function	Default
D31-D0	SPCR	Receive short packet counter.	0

(127) Receive long packet counter load register (LPCR)

POS mode:

This register reads the receive long packet counter value.

Register Name	Address				Access	Default
	Port0:	Port1:	Port2:	Port3:		
LPCR	0310 H	0710 H	0B10 H	0F10 H	R	00000000 H

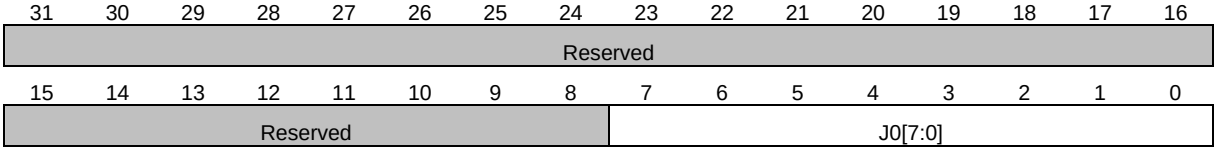


Bit	Field	Function	Default
D31-D0	LPCR	Receive long packet counter.	0

(128) Transmit J0 insert register (J0T)

The J0T register sets the transmit J0 byte.

Register Name	Address				Access	Default
	Port0:	Port1:	Port2:	Port3:		
J0T	0320 H	0720 H	0B20 H	0F20 H	R/W	00000001 H

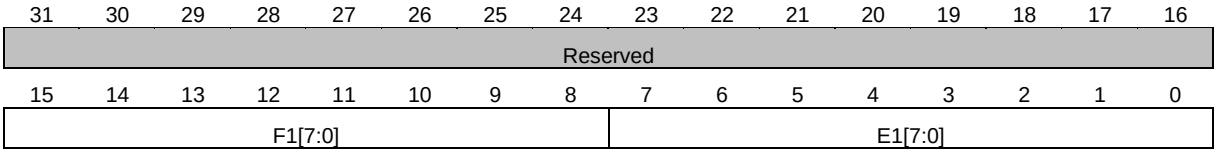


Bit	Field	Function	Default
D31-D8	Reserved	Set to 0.	0
D7-D0	J0[7:0]	Sets the data to be inserted at the position of the J0 byte of a transmit frame.	01H

(129) Transmit E1 and F1 insert register (E1F1T)

The E1F1T register sets the transmit E1 byte.

Register Name	Address				Access	Default
	Port0:	Port1:	Port2:	Port3:		
E1F1T	0324 H	0724 H	0B24 H	0F24 H	R/W	00000000H

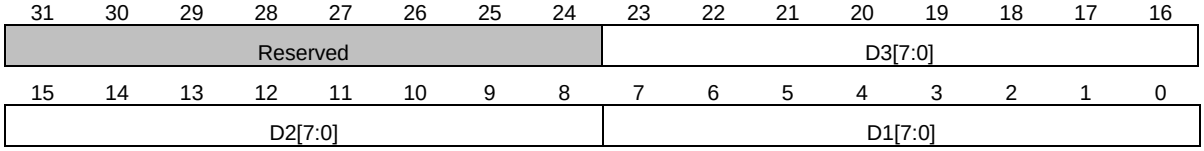


Bit	Field	Function	Default
D31-D16	Reserved	Set to 0.	0
D15-D8	F1[7:0]	Sets the data to be inserted at the position of the F1 byte of a transmit frame.	0
D7-D0	E1[7:0]	Sets the data to be inserted at the position of the E1 byte of a transmit frame.	0

(130) Transmit Section DCC insert register (SDCCT)

The SDCCT register sets the transmit D1 through D3 byte.

Register Name	Address				Access	Default
	Port0:	Port1:	Port2:	Port3:		
SDCCT	0328 H	0728 H	0B28 H	0F28 H	R/W	00000000 H

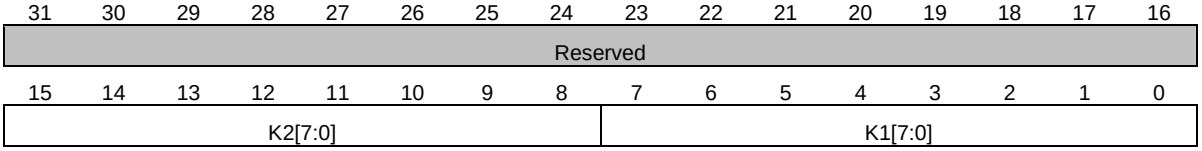


Bit	Field	Function	Default
D31-D24	Reserved	Set to 0.	0
D23-D16	D3[7:0]	Sets the data to be inserted at the position of the D3 byte of a transmit frame.	0
D15-D8	D2[7:0]	Sets the data to be inserted at the position of the D2 byte of a transmit frame.	0
D7-D0	D1[7:0]	Sets the data to be inserted at the position of the D1 byte of a transmit frame.	0

(131) Transmit K1 and K2 insert register (K12T)

The K12T register sets the K1 and K2 bytes to be stored into a transmit frame.

Register Name	Address				Access	Default
	Port0:	Port1:	Port2:	Port3:		
K12T	032C H	072C H	0B2C H	0F2C H	R/W	00000000 H

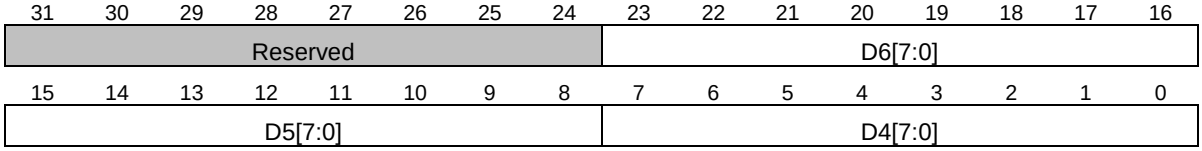


Bit	Field	Function	Default
D31-D16	Reserved	Set to 0.	0
D15-D8	K2[7:0]	Sets the data to be inserted at the position of the K2 byte of a transmit frame. Bits 6 to 8 of the K2 byte are used when the μPD98413 transmits alarm Line AIS or Line RDI. When the μPD98413 transmits alarm Line AIS or Line RDI, transmission of an alarm is take precedence over the setting of K2[7:0] of this register. When the μPD98413 does not transmit alarm Line AIS or Line RDI, the values of K2[7:0] of this register are transmitted.	0
D7-D0	K1[7:0]	Sets the data to be inserted at the position of the K1 byte of a transmit frame.	0

(132) Transmit Line DCC insert register 1 (LDCCT1)

The LDCCT1 register sets the transmit D4 through D5 bytes.

Register Name	Address				Access	Default
	Port0:	Port1:	Port2:	Port3:		
LDCCT1	0330 H	0730 H	0B30 H	0F30 H	R/W	00000000 H

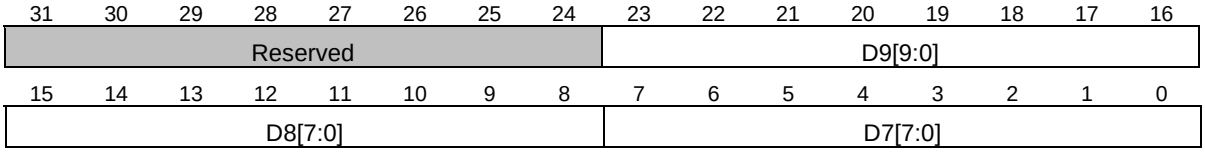


Bit	Field	Function	Default
D31-D24	Reserved	Set to 0.	0
D23-D16	D6[7:0]	Sets the data to be inserted at the position of the D6 byte of a transmit frame.	0
D15-D8	D5[7:0]	Sets the data to be inserted at the position of the D5 byte of a transmit frame.	0
D7-D0	D4[7:0]	Sets the data to be inserted at the position of the D4 byte of a transmit frame.	0

(133) Transmit Line DCC insert register 2 (LDCCT2)

The LDCCT2 register sets the transmit D7 through D9 bytes.

Register Name	Address				Access	Default
	Port0:	Port1:	Port2:	Port3:		
LDCCT2	0334 H	0734 H	0B34 H	0F34 H	R/W	00000000 H

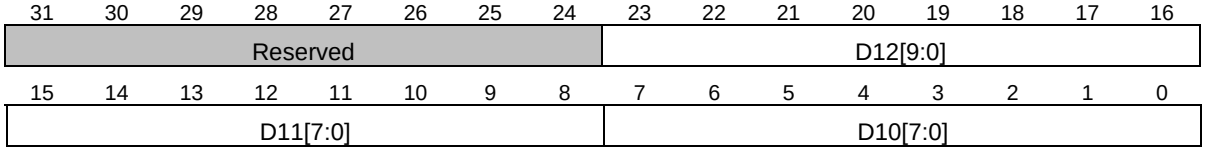


Bit	Field	Function	Default
D31-D24	Reserved	Set to 0.	0
D23-D16	D9[7:0]	Sets the data to be inserted at the position of the D9 byte of a transmit frame.	0
D15-D8	D8[7:0]	Sets the data to be inserted at the position of the D8 byte of a transmit frame.	0
D7-D0	D7[7:0]	Sets the data to be inserted at the position of the D7 byte of a transmit frame.	0

(134) Transmit Line DCC insert register 3 (LDCCT3)

The LDCCT3 register sets the transmit D10 through D12 bytes.

Register Name	Address				Access	Default
	Port0:	Port1:	Port2:	Port3:		
LDCCT3	0338 H	0738 H	0B38 H	0F38 H	R/W	00000000H

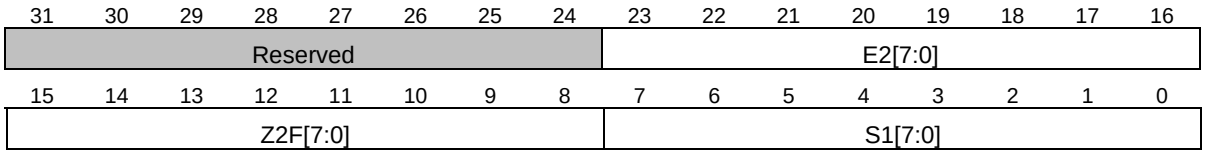


Bit	Field	Function	Default
D31-D24	Reserved	Set to 0.	0
D23-D16	D12[7:0]	Sets the data to be inserted at the position of the D12 byte of a transmit frame.	0
D15-D8	D11[7:0]	Sets the data to be inserted at the position of the D11 byte of a transmit frame.	0
D7-D0	D10[7:0]	Sets the data to be inserted at the position of the D10 byte of a transmit frame.	0

(135) Transmit S1, 1st Z2 and E2 insert register (S1Z2E2T)

The S1Z2E2T register sets the transmit S1, 1st Z2 and E2 byte.

Register Name	Address				Access	Default
	Port0:	Port1:	Port2:	Port3:		
S1Z2E2T	033C H	073C H	0B3C H	0F3C H	R/W	00000000 H

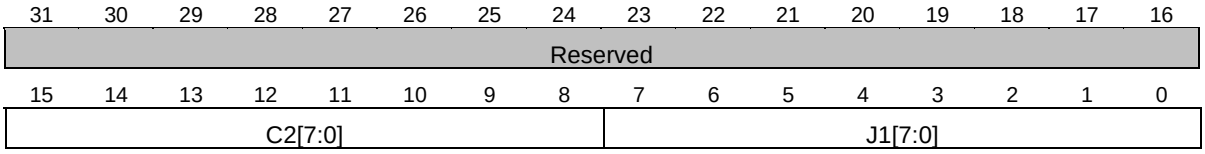


Bit	Field	Function	Default
D31-D24	Reserved	Set to 0.	0
D23-D16	E2[7:0]	Sets the data to be inserted at the position of the E2 byte of a transmit frame.	0
D15-D8	Z2F[7:0]	Sets the data to be inserted at the position of the 1st Z2 byte of a transmit frame.	0
D7-D0	S1[7:0]	Sets the data to be inserted at the position of the S1 byte of a transmit frame.	0

(136) Transmit J1 and C2 insert register (J1C2T)

The J1C2T register sets the transmit J1 and C2 byte.

Register Name	Address				Access	Default
	Port0:	Port1:	Port2:	Port3:		
J1C2T	0340 H	0740 H	0B40 H	0F40 H	R/W	00001300 H

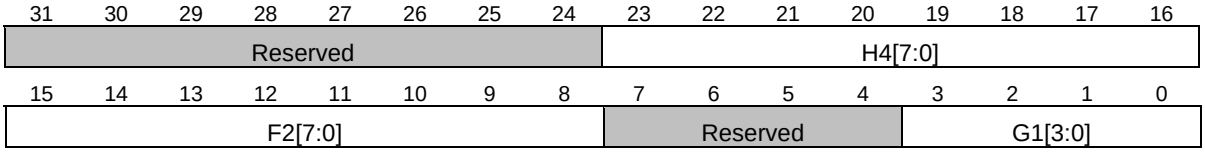


Bit	Field	Function	Default
D31-D16	Reserved	Set to 0.	0
D15-D8	C2[7:0]	Sets the data to be inserted at the position of the C2 byte of a transmit frame.	13H
D7-D0	J1[7:0]	Sets the data to be inserted at the position of the J1 byte of a transmit frame.	0

(137) Transmit G1, F2 and H4 insert register (G1F2H4T)

The G1F2H4T register sets the transmit G1, F2 and H4 byte.

Register Name	Address				Access	Default
	Port0:	Port1:	Port2:	Port3:		
G1F2H4T	0344 H	0744 H	0B44 H	0F44 H	R/W	00000000 H

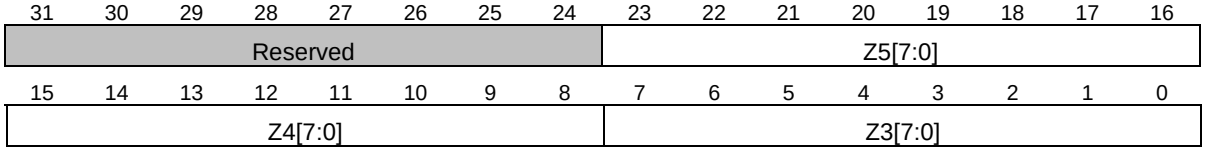


Bit	Field	Function	Default
D31-D24	Reserved	Set to 0.	0
D23-D16	H4[7:0]	Sets the data to be inserted at the position of the H4 byte of a transmit frame.	0
D15-D8	F2[7:0]	Sets the data to be inserted at the position of the F2 byte of a transmit frame.	0
D7-D4	Reserved	Set to 0.	0
D3-D0	G1[3:0]	Set the data to be inserted at the position of the G1 byte (bits 5 to 8) of a transmit frame. The μPD98413 overwrites bits 5 to 7 when it transmits Path RDI because of command execution or automatic loopback.	0

(138) Transmit Z3 through Z5 insert register (Z345T)

The Z345T register sets the transmit Z3 through Z5 bytes.

Register Name	Address				Access	Default
	Port0:	Port1:	Port2:	Port3:		
Z345T	0348 H	0748 H	0B48 H	0F48 H	R/W	00000000H

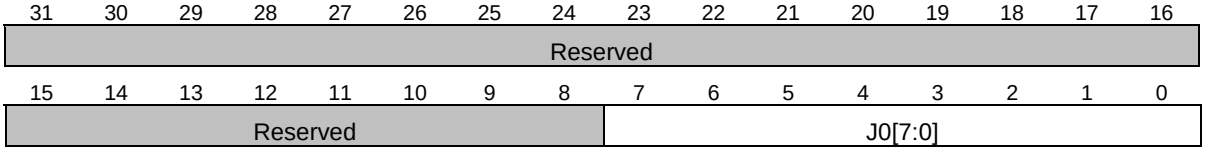


Bit	Field	Function	Default
D31-D24	Reserved	Set to 0.	0
D23-D16	Z5[7:0]	Sets the data to be inserted at the position of the Z5 byte of a transmit frame.	0
D15-D8	Z4[7:0]	Sets the data to be inserted at the position of the Z4 byte of a transmit frame.	0
D7-D0	Z3[7:0]	Sets the data to be inserted at the position of the Z3 byte of a transmit frame.	0

(139) Receive J0 drop register (J0R)

The J0R register is used for storing the receive J0 byte.

Register Name	Address				Access	Default
	Port0:	Port1:	Port2:	Port3:		
J0R	0360 H	0760 H	0B60 H	0F60 H	R	00000000 H

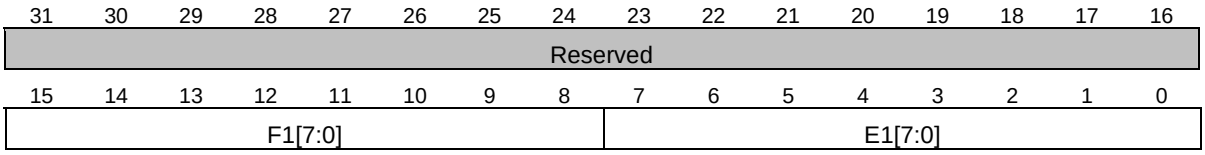


Bit	Field	Function	Default
D31-D8	Reserved		0
D7-D0	J0[7:0]	Stores the receive J0 byte. This field is updated each time a frame is received.	0

(140) Receive E1 and F1 drop register (E1F1R)

The E1F1R register is used for storing the receive E1 and F1 bytes.

Register Name	Address				Access	Default
	Port0:	Port1:	Port2:	Port3:		
E1F1R	0364 H	0764 H	0B64 H	0F64 H	R	00000000 H

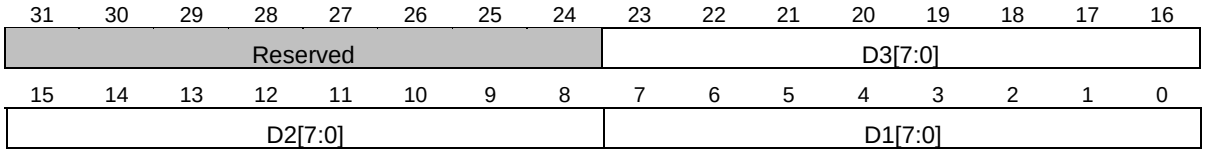


Bit	Field	Function	Default
D31-D16	Reserved		0
D15-D8	F1[7:0]	Stores the receive F1 byte. This field is updated each time a frame is received.	0
D7-D0	E1[7:0]	Stores the receive E1 byte. This field is updated each time a frame is received.	0

(141) Receive Section DCC drop register (SDCCR)

The SDCCR register is used for storing the receive D1 through D3 bytes.

Register Name	Address				Access	Default
	Port0:	Port1:	Port2:	Port3:		
SDCCR	0368 H	0768 H	0B68 H	0F68 H	R	00000000 H

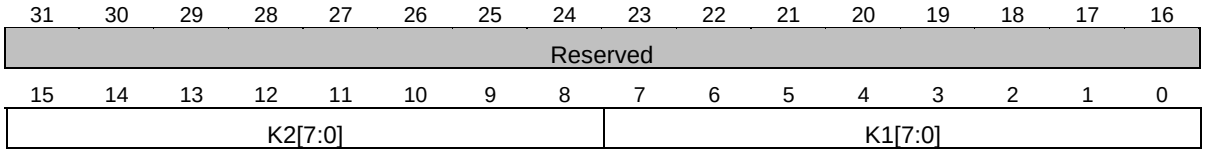


Bit	Field	Function	Default
D31-D24	Reserved		0
D23-D16	D3[7:0]	Stores the receive D3 byte. This field is updated each time a frame is received.	0
D15-D8	D2[7:0]	Stores the receive D2 byte. This field is updated each time a frame is received.	0
D7-D0	D1[7:0]	Stores the receive D1 byte. This field is updated each time a frame is received.	0

(142) Receive K1 and K2 drop register (K12R)

The K12R register is used for storing the receive K1 and K2 bytes.

Register Name	Address				Access	Default
	Port0:	Port1:	Port2:	Port3:		
K12R	036C H	076C H	0B6C H	0F6C H	R	00000000 H



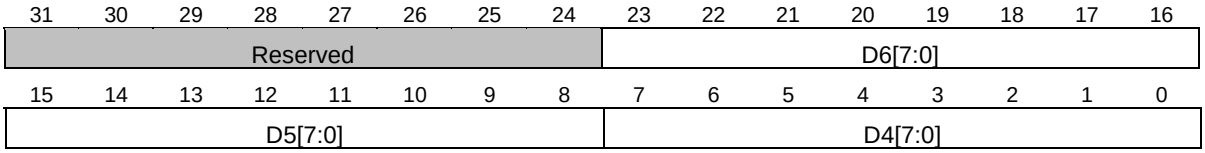
Bit	Field	Function	Default
D31-D16	Reserved		0
D15-D8	K2[7:0]	The receive K2 byte is stored.	0
D7-D0	K1[7:0]	The receive K1 byte is stored.	0

This register is updated when three contiguous frames containing the same K1 and K2 bytes are received after the contents of the register are changed.

(143) Receive Line DCC drop register 1 (LDCCR1)

The LDCCR1 register is used for storing the receive D4 through D6 bytes.

Register Name	Address				Access	Default
	Port0:	Port1:	Port2:	Port3:		
LDCCR1	0370 H	0770 H	0B70 H	0F70 H	R	00000000 H

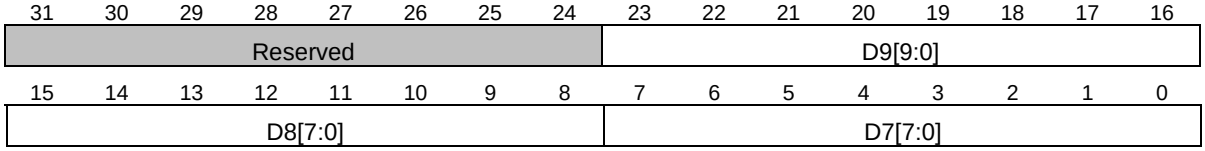


Bit	Field	Function	Default
D31-D24	Reserved		0
D23-D16	D6[7:0]	Stores the receive D6 byte. This field is updated each time a frame is received.	0
D15-D8	D5[7:0]	Stores the receive D5 byte. This field is updated each time a frame is received.	0
D7-D0	D4[7:0]	Stores the receive D4 byte. This field is updated each time a frame is received.	0

(144) Receive Line DCC drop register 2 (LDCCR2)

The LDCCR2 register is used for storing the receive D7 through D9 bytes.

Register Name	Address				Access	Default
	Port0:	Port1:	Port2:	Port3:		
LDCCR2	0374 H	0774 H	0B74 H	0F74 H	R	00000000 H

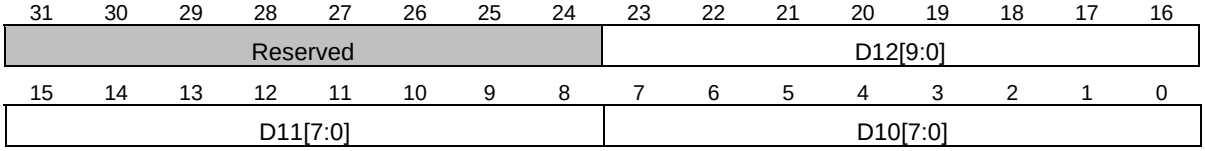


Bit	Field	Function	Default
D31-D24	Reserved		0
D23-D16	D9[7:0]	Stores the receive D9 byte. This field is updated each time a frame is received.	0
D15-D8	D8[7:0]	Stores the receive D8 byte. This field is updated each time a frame is received.	0
D7-D0	D7[7:0]	Stores the receive D7 byte. This field is updated each time a frame is received.	0

(145) Receive Line DCC drop register 3 (LDCCR3)

The LDCCR3 register is used for storing the receive D10 through D12 bytes.

Register Name	Address				Access	Default
	Port0:	Port1:	Port2:	Port3:		
LDCCR3	0378 H	0778 H	0B78 H	0F78 H	R	00000000 H

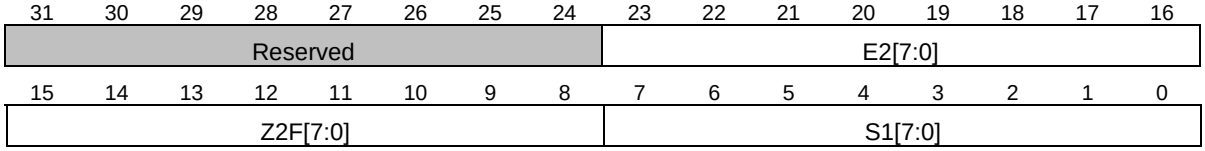


Bit	Field	Function	Default
D31-D24	Reserved		0
D23-D16	D12[7:0]	Stores the receive D12 byte. This field is updated each time a frame is received.	0
D15-D8	D11[7:0]	Stores the receive D11 byte. This field is updated each time a frame is received.	0
D7-D0	D10[7:0]	Stores the receive D10 byte. This field is updated each time a frame is received.	0

(146) Receive S1, 1st Z2 and E2 drop register (S1Z2E2R)

The S1Z2E2R register is used for storing the receive S1, 1st Z2 and E2 byte.

Register Name	Address				Access	Default
	Port0:	Port1:	Port2:	Port3:		
S1Z2E2R	037C H	077C H	0B7C H	0F7C H	R	00000000 H

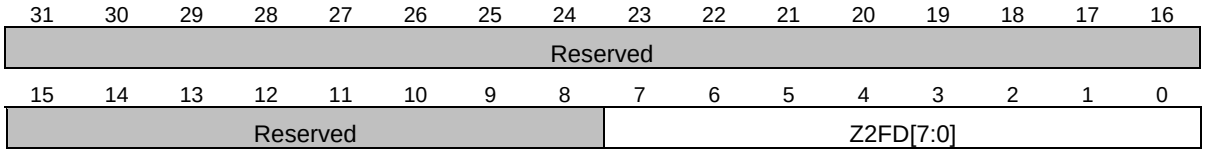


Bit	Field	Function	Default
D31-D24	Reserved		0
D23-D16	E2[7:0]	Stores the receive E2 byte. This field is updated each time a frame is received.	0
D15-D8	Z2F[7:0]	Stores the receive 1st Z2 byte. This field is updated each time a frame is received.	0
D7-D0	S1[7:0]	Stores the receive S1 byte. This field is updated each time a frame is received.	0

(147) Receive 1st Z2 drop register 1 (Z2FDR)

The Z2FDR register is used for storing the receive 1st Z2 byte.

Register Name	Address				Access	Default
	Port0:	Port1:	Port2:	Port3:		
Z2FDR	0380 H	0780 H	0B80 H	0F80 H	R	00000000 H

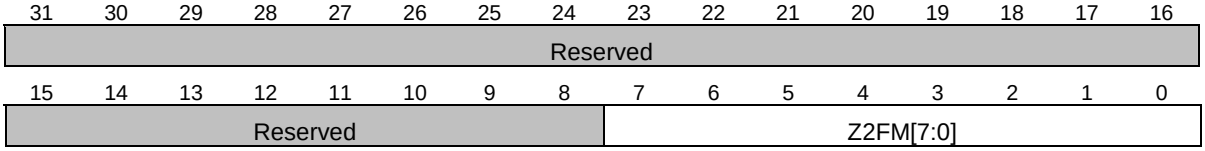


Bit	Field	Function	Default
D31-D8	Reserved		0
D7-D0	Z2FD[7:0]	Stores the receive 1st Z2 byte. This field is updated when six contiguous frames containing the same bit 6-7 of 1st Z2 byte are received after the contents of the register are changed.	0

(148) Receive 1st Z2 drop register 2 (Z2FMR)

The Z2FMR register is used for storing the receive 1st Z2 byte.

Register Name	Address				Access	Default
	Port0:	Port1:	Port2:	Port3:		
Z2FMR	0384 H	0784 H	0B84 H	0F84 H	R	00000000 H

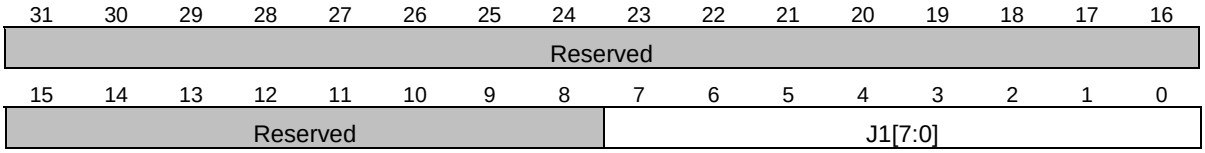


Bit	Field	Function	Default
D31-D8	Reserved		0
D7-D0	Z2FM[7:0]	Stores the receive 1st Z2 byte. This field is updated when 12 contiguous frames containing the same bit 7-8 of 1st Z2 byte are received after the contents of the register are changed.	0

(149) Receive J1 drop register (J1R)

The J1R register is used for storing the receive J1 byte.

Register Name	Address				Access	Default
	Port0:	Port1:	Port2:	Port3:		
J1R	0388 H	0788 H	0B88 H	0F88 H	R	00000000 H

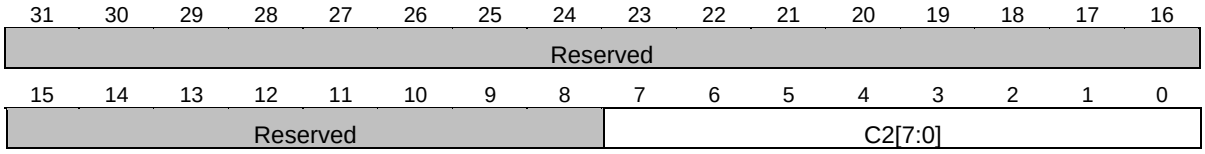


Bit	Field	Function	Default
D31-D8	Reserved		0
D7-D0	J1[7:0]	Stores the receive J1 byte. This field is updated each time a frame is received.	0

(150) Receive C2 drop register (C2R)

The C2R register is used for storing the receive C2 byte.

Register Name	Address				Access	Default
	Port0:	Port1:	Port2:	Port3:		
C2R	038C H	078C H	0B8C H	0F8C H	R	00000000 H



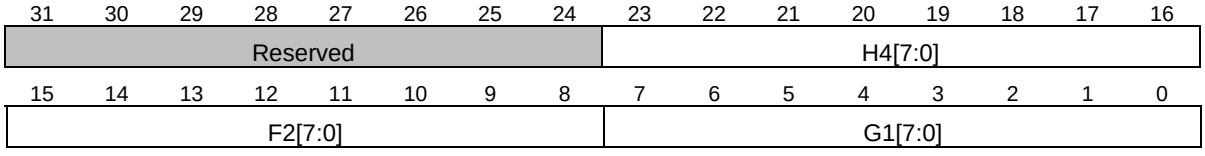
Bit	Field	Function	Default
D31-D8	Reserved		0
D7-D0	C2[7:0]	Stores the receive C2 byte. This field is updated when three or five contiguous frames containing the same C2 byte are received after the contents of the register are changed.	0

Note: This register is updated if the same value is received in three or five time consecutive.

(151) Receive G1, F2 and H4 drop register (G1F2H4R)

The G1F2H4R register is used for storing the receive G1, F2 and H4 byte.

Register Name	Address				Access	Default
	Port0:	Port1:	Port2:	Port3:		
G1F2H4R	0390 H	0790 H	0B90 H	0F90 H	R	00000000 H

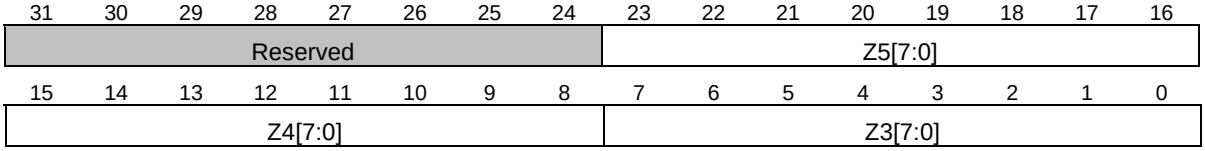


Bit	Field	Function	Default
D31-D24	Reserved		0
D23-D16	H4[7:0]	Stores the receive H4 byte. This field is updated each time a frame is received.	0
D15-D8	F2[7:0]	Stores the receive F2 byte. This field is updated each time a frame is received.	0
D7-D0	G1[7:0]	Stores the receive G1 byte. This field is updated each time a frame is received.	0

(152) Receive Z3 through Z5 drop register (Z345R)

The Z345R register is used for storing the receive Z3 through Z5 byte.

Register Name	Address				Access	Default
	Port0:	Port1:	Port2:	Port3:		
Z345R	0394 H	0794 H	0B94 H	0F94 H	R	00000000 H



Bit	Field	Function	Default
D31-D24	Reserved		0
D23-D16	Z5[7:0]	Stores the receive Z5 byte. This field is updated each time a frame is received.	0
D15-D8	Z4[7:0]	Stores the receive Z4 byte. This field is updated each time a frame is received.	0
D7-D0	Z3[7:0]	Stores the receive Z3 byte. This field is updated each time a frame is received.	0

[MEMO]

CHAPTER 6 JTAG BOUNDARY SCAN

The μPD98413 has a JTAG boundary scan circuit.

Caution: Some pins do not support the JTAG, as shown in the table.

Type	Name of Pin Which Does Not to Support JTAG	Number of Pins
PECL-level pins	T.B.D	T.B.D
ohters	T.B.D	T.B.D
T.B.D	T.B.D	T.B.D

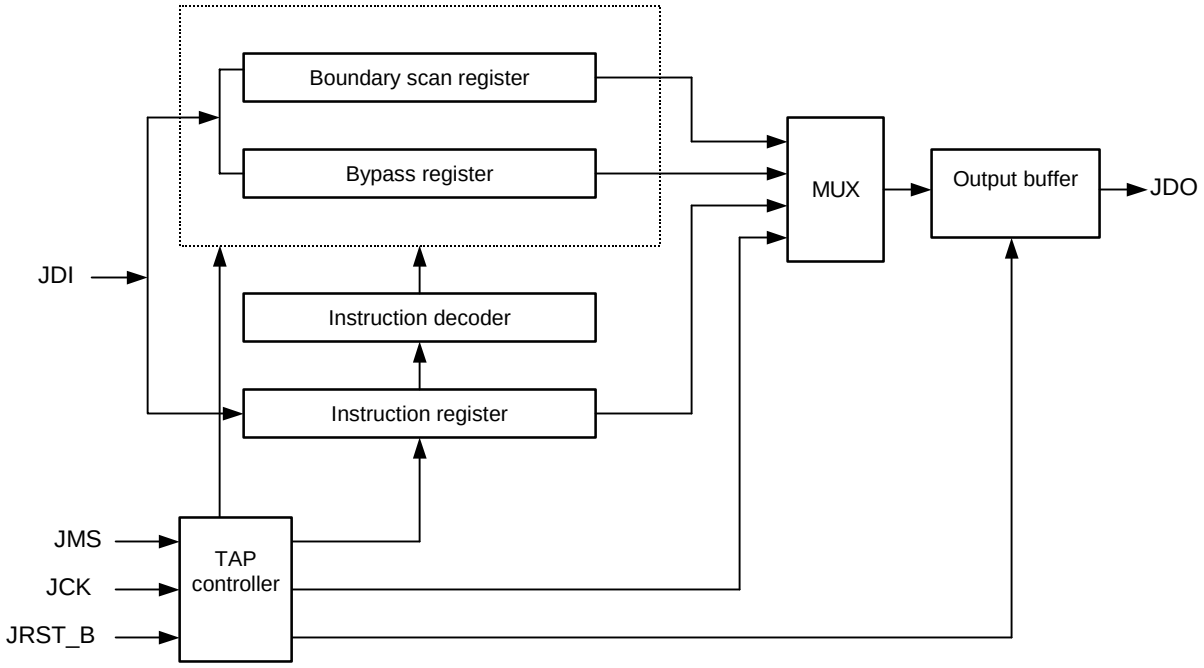
6.1 Features

- Conforms to IEEE1149.1 JTAG Boundary Scan Standard.
- Three registers dedicated to boundary scan
  - Instruction register
  - Bypass register
  - Boundary scan register
- Three instructions supported
  - BYPASS instruction
  - EXTEST instruction
  - SAMPLE/PRELOAD instruction
- Five pins dedicated to boundary scan
  - JCK (JTAG Clock)
  - JMS (JTAG Mode Select)
  - JDI (JTAG Data Input)
  - JDO (JTAG Data Output)
  - JRST_B (JTAG Reset)

6.2 Internal Configuration of Boundary Scan Circuit

Figure 6-1 shows the block diagram of the internal JTAG boundary scan circuit of the μPD98413.

Figure 6-1. Block Diagram of Boundary Scan Circuit



6.2.1 Instruction Register

The instruction register consists of a two-bit shift register and writes instruction data from the JDI pin. The register and instruction are selected by this instruction data.

6.2.2 TAP (Test Access Port) Controller

The TAP controller changes operating state by latching the signal of the JMS pin at the rising edge of the clock input to the JCK pin.

6.2.3 Bypass Register

The bypass register consists of a one-bit shift register connected between the JDI and JDO pins when the TAP controller is in Shift-DR state. If this register is selected while the TAP controller is in Shift-DR state, data is shifted to the JDO pin at the rising edge of the clock input to the JCK pin.

When this register is selected, the operation of the JTAG boundary circuit does not influence on the operation of the μPD98413.

6.2.4 Boundary Scan Register

The boundary scan register is located between an external pin of the mPD98414 and internal logic circuit. When this register is selected, data is latched or loaded by the instruction of the TAP controller.

If this register is selected while the TAP controller is in Shift-DR state, data is output to the JDO pin starting from the LSB at the falling edge of the clock input to the JCK pin.

6.3 Pin Function

6.3.1 JCK (JTAG Clock) Pin

The JCK pin is used to supply a clock signal to the JTAG boundary scan circuit (such as the bypass register, instruction register, and TAP controller. This clock signal is isolated so as not to be supplied to the other internal circuits of the μPD98413.

6.3.2 JMS (JTAG Mode Select) Pin

Input to the JMS pin is latched at the rising edge of the clock input to the JCK pin and defines the operation of the TAP controller.

6.3.3 JDI (JTAG Data Input) Pin

The JDI pin is an input pin that inputs data to the JTAG boundary scan circuit register.

6.3.4 JDO (JTAG Data Output) Pin

The JDO pin is an output pin that outputs data from the JTAG boundary scan circuit. This pin changes its output at the falling edge of the clock input to the JCK pin. This pin is a tristate output pin and is controlled by the TAP controller.

6.3.5 JRST_B (JTAG Reset) Pin

This pin asynchronously initializes the TAP controller. This reset signal sets the μPD98413 in the normal operation mode and the boundary register in non-operation state.

6.4 Operation Description

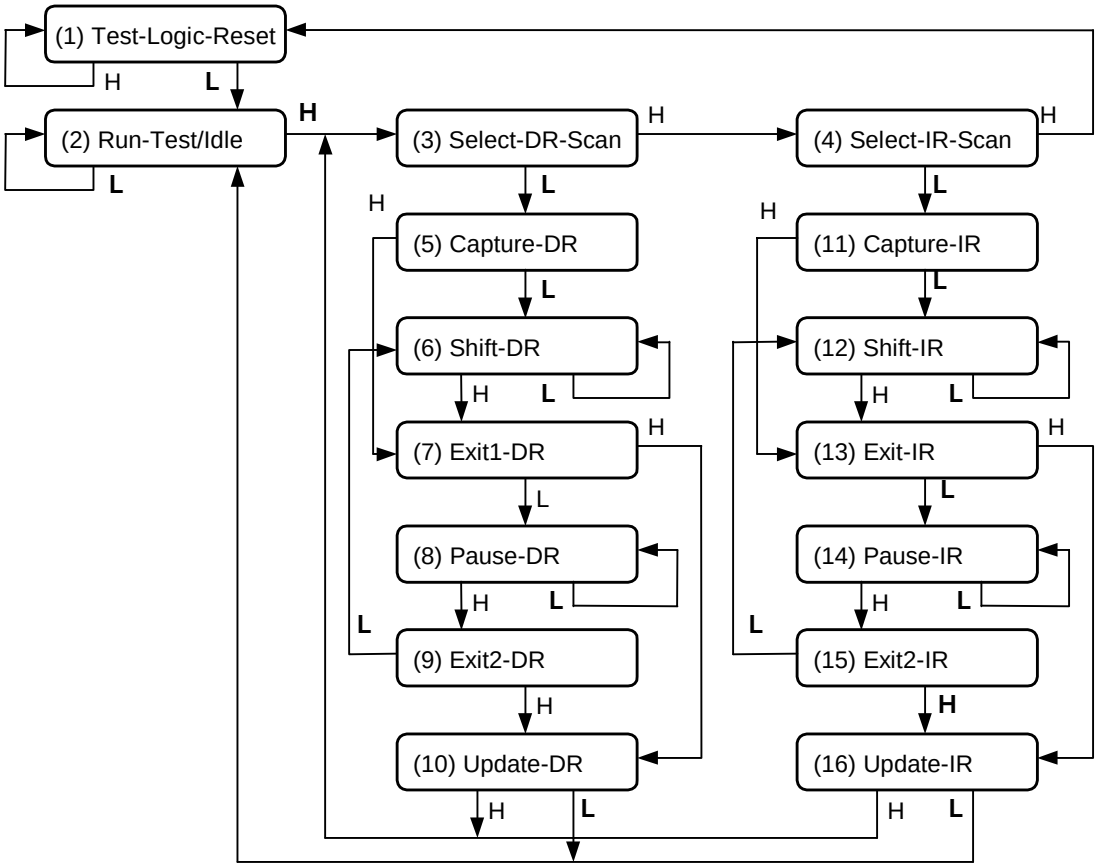
6.4.1 TAP Controller

The TAP controller is a circuit having 16 states synchronized with changes of the JMS and JCK pins. Its operation is specified by IEEE Standard 1149.1.

6.4.2 TAP Controller State

Figure 6-2 shows the state transition of the TAP controller. The state of the TAP controller is determined depending on the state of the JMS pin signal input at the rising edge of the clock input to the JCK pin. The operations of the instruction register, boundary scan register, and bypass register change at the rising or falling edge of the clock input to the JCK pin. (See Figure 6-3).

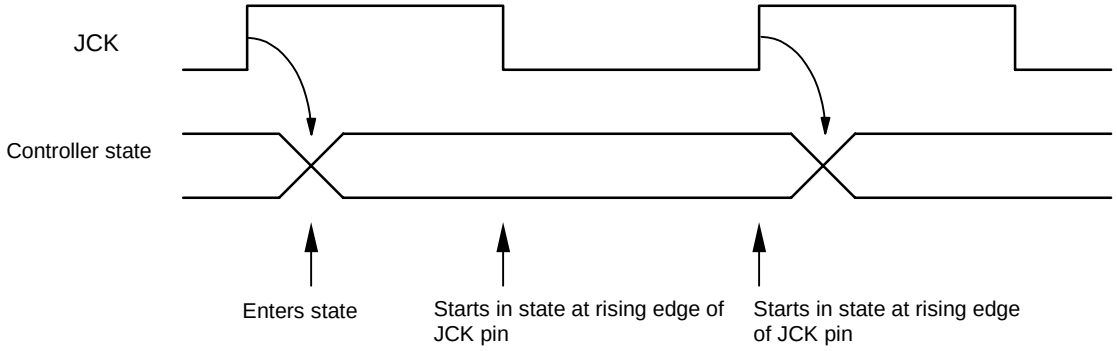
Figure 6-2. State Transition of TAP Controller



Remarks 1. "H" and "L" of the arrows indicating state transition in the above figure indicate the state of the JMS pin at the rising edge of the clock input to the JCK pin.

2. Numbers in ( ) in the above figure correspond to the explanation below.

Figure 6-3. Operation Timing in Controller State



(1) Test-Logic-Reset

The JTAG boundary scan circuit performs no operation on the mPD98414. Therefore, it does not affect the system logic of the mPD98414. This is because the bypass instruction is stored to the instruction register and executed on initialization. The TAP controller enters the Test-Logic-Reset state if the JMS pin signal holds the high level for the duration of at least five rising edges of the JCK pin signal, regardless of the current state of the controller. The TAP controller holds this state for the duration in which the JMS pin signal high.

If the TAP controller must be in the Test-Logic-Reset state, the controller returns to the original Test-Logic-Reset state even if a low-level signal is input once to the JMS pin by mistake (due to, for example, the influence of the external interface), if the JMS pin signal holds its high level status for the duration of three rising edges of the JCK pin signal.

The operation of the test logic does not hinder the logic operation of the mPD98414 due to the above error.

When the TAP controller exits from the Test-Logic-Reset state, the controller enters the Run-Test/Idle state. In this state, no operation is performed because the current instruction is set by the operation of the bypass register. The logic operation of the JTAG boundary scan circuit is inactive even in the Select-DR-Scan and Select-IR-Scan states.

(2) Run-Test/Idle

The TAP controller is in this state during scan operation (in Select-DR-Scan or Select-IR-Scan state). Once the controller has entered this state and if the JMS pin signal holds the low level, the controller remains in this state.

The controller enters the Select-DR-Scan state if the JMS pin signal holds high level at one rising edge of the JCK pin signal.

All the test data registers (boundary register and bypass register) selected by the current instruction hold the previous status (Idle). While the TAP controller is in this state, the instruction does not change.

(3) Select-DR-Scan

This is a temporary boundary scan state. The boundary scan register and bypass register selected by the current instruction hold the previous state.

If the JMS signal is held low at the rising edge of the JCK pin signal while the TAP controller is in this state, the controller enters the Capture-DR state, and scan sequence to the selected registers is started.

If the JMS signal is held high at the rising edge of the JCK pin signal, the TAP controller enters the Select-IR-Scan state. While the controller is in this state, the instruction does not change.

(4) Select-IR-Scan

This is a temporary boundary scan state. The boundary scan register and bypass register selected by the current instruction hold the previous state.

If the JMS signal is held low at the rising edge of the JCK pin signal while the TAP controller is in this state, the controller enters the Capture-IR state, and scan sequence to the selected registers is started.

If the JMS signal is held high at the rising edge of the JCK pin signal, the TAP controller enters the Test-Logic-Reset state. While the controller is in this state, the instruction does not change.

(5) Capture-DR

In this controller state, data is loaded to the boundary scan register selected by the current instruction in parallel at the rising edge of the JCK pin signal (in this case, data is input from the input pin of each device to the corresponding boundary scan register). While the TAP controller is in this state, the instruction does not change.

If the TAP controller is in this state at the rising edge of the JCK pin signal, the controller enters the following state:

- If the JMS pin signal is held high: Exit1-DR state
- If the JMS pin signal is held low: Shift-DR state

(6) Shift-DR

In this controller state, JDI and JDO are connected (at either of the boundary scan register of bypass register) by the current instruction. The shift data is shifted one state at a time toward the serial output direction at each rising edge of the JCK pin signal.

The boundary scan register or bypass register selected by the current instruction holds the previous status without change if the controller is not on the serial bus (not in the Shift-DR state). While the controller is in this state, the instruction does not change.

If the TAP controller is in this state at the rising edge of the JCK pin signal, the controller enters the following state:

- If the JMS pin signal is held high: Exit1-DR state
- If the JMS pin signal is held low: Shift-DR state

(7) Exit1-DR

This is a temporary controller state. If the JMS pin signal is held high at the rising edge of the JCK pin signal with the TAP controller in this state, the controller enters the Update-DR state. This ends the scan process.

If the JMS pin signal is held low at the rising edge of the JCK pin signal, the TAP controller enters the Pause-DR state.

Both the bypass register and boundary scan register selected by the current instruction hold the previous status without change. While the TAP controller is in this state, the instruction does not change.

(8) Pause-DR

In this controller state, shifting between JDI and JDO connected by either the bypass register or boundary scan register is temporarily stopped. These registers selected by the current instruction hold the previous state without change.

The TAP controller remains in this state while the JMS pin signal is low. If the JMS pin signal is held high at the rising edge of the JCK pin signal, the TAP controller enters the Exit2-DR state. While the TAP controller is in this state, the instruction does not change.

(9) Exit2-DR

This is a temporary controller state. If the JMS pin signal is held high at the rising edge of the JCK pin signal with the TAP controller in this state, the controller enters the Update-DR state. This ends the scan process.

If the JMS pin signal is held low at the rising edge of the JCK pin signal, the TAP controller enters the Shift-DR state.

Both the bypass register and boundary scan register selected by the current instruction hold the previous status without change. While the TAP controller is in this state, the instruction does not change.

(10) Update-DR

The boundary scan register has a parallel output latch to prevent changes in parallel output (while shifted to the shift register path concatenated) by certain instructions (for example, EXTEST instruction).

In the Update-DR controller state, data is latched from the shift register to the parallel output latch of this register at the falling edge of the JCK pin signal.

The data retained latched to the parallel output latch changes depending on this controller state (the data does not change with the other controller states).

The previous states of all the shift register of the boundary scan register selected by the current instruction are retained.

While the TAP controller is in this state, the instruction does not change.

If the JMS pin signal is held high at the rising edge of the JCK pin signal with the TAP controller in this state, the controller enters the Select-DR-Scan state.

If the JMS signal is held low at the rising edge of the JCK pin signal, the TAP controller enters the Run-Test/Idle state.

(11) Capture-IR

In this controller state, the shift register loads the pattern of a fixed logic value [01 (binary)] to the instruction register at the rising edge of the JCK pin signal.

The previous states of both the bypass register and boundary scan register selected by the current instruction are retained without change.

While the TAP controller is in this state, the instruction does not change.

If the JMS pin signal is held high at the rising edge of the JCK pin signal while the controller is in this state, the controller enters the Exit1-IR state.

If the JMS pin signal is held low at the rising edge of the JCK pin signal, the TAP controller enters the Shift-IR state.

(12) Shift-IR

In this controller state, JDI and JDO are connected by the shift register in the instruction register. The shift data is shift one state toward the serial output direction at each rising edge of the JCK pin signal.

The boundary scan register or bypass register selected by the current instruction holds the previous state without change.

While the TAP controller is in this state, the instruction does not change.

If the JMS pin signal is held high at the rising edge of the JCK pin signal with the TAP controller in this state, the controller enters the Exit1-IR state. If the JMS pin signal is held low, the controller remains the Shift-IR state.

(13) Exit1-IR

This is a temporary controller state. If the JMS pin signal is held high at the rising edge of the JCK pin signal, the TAP controller enters the Update-IR state. This ends the scan process.

If the JMS pin signal is held low at the rising edge of the JCK pin, the TAP controller enters the Pause-IR state.

Both the bypass register and boundary scan register selected by the current instruction retain their states without change.

While the TAP controller is in this state, the instruction does not change.

(14) Pause-IR

In this controller state, shift of the instruction register is temporarily stopped. The bypass register and boundary scan register selected by the current instruction hold the previous state without change.

While the TAP controller is in this state, the instruction does not change. The instruction register holds the current state.

While the JMS pin signal is low, the TAP controller remains in this state. If the JMS pin signal is held high at the rising edge of the JCK pin signal, the TAP controller enters the Exit2-IR state.

(15) Exit2-IR

This is a temporary controller state. If the JMS pin signal is held high at the rising edge of the JCK pin signal, the TAP controller enters the Update-IR state. This ends the scan process.

If the JMS pin signal is held low at the rising edge of the JCK pin signal, the TAP controller enters the Shift-IR state.

Both the bypass register and boundary scan register selected by the current instruction retain their states without change.

While the TAP controller is in this state, or while the instruction register holds the current state, the instruction does not change.

(16) Update-IR

In this controller state, the instruction shifted to the instruction register is latched to the parallel output latch from the shift register path at the falling edge of the JCK pin signal. Once a new instruction has been latched, it is used as the current instruction.

The bypass register or boundary scan register selected by the current instruction holds the previous state.

If the JMS pin signal is held high at the rising edge of the JCK pin signal while the TAP controller is in this state, the TAP controller enters the Select-DR-Scan state.

If the JMS pin signal is held low at the rising edge of the JCK pin signal, the TAP controller enters the Run-Test/Idle state.

The Pause-DR controller state in (8) and Pause-IR controller state in (14) temporarily stop shifting of data in the bypass register, boundary scan register, or instruction register.

6.5 TAP Controller Operation

The TAP controller operates as follows.
The state of the controller is changed by either of (1) and (2) below.

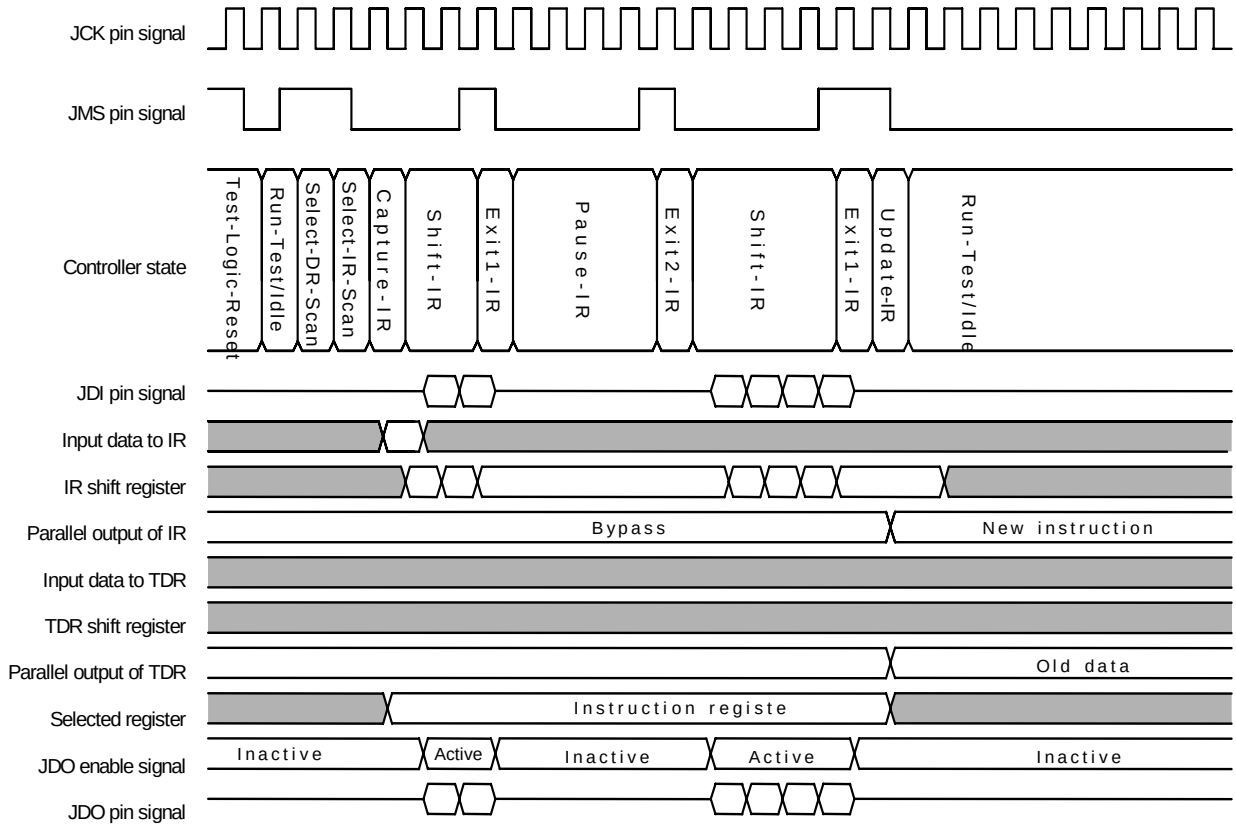
(1) Rising edge of JCK pin signal
(2) JRST_B pin input

The TAP controller generates signals that control the operations of the bypass register, boundary scan register, and instruction register defined by the IEEE1149.1 JTAG Boundary Scan Standard (see Figures 6-4 and 6-5).
The JDO pin output buffer and the peripheral circuit that selects a register whose contents are to be output to the JDO pin are controlled as shown in Table 6-1. The JDO pin defined in this table changes at the falling edge of the JCK pin signal after it has entered each state.

Table 6-1. Operation in Each Controller State

Controller State	Selected Register to Be Driven to JDO Pin	JDO Pin Driver
Test-Logic-Reset	Undefined	High impedance
Run-Test/Idle		
Select-DR-Scan		
Select-IR-Scan		
Capture-IR		
Shift-IR	Instruction register	Active
Exit1-IR	Undefined	High impedance
Pause-IR		
Exit2-IR		
Update-IR		
Capture-DR		
Shift-DR	Data register (boundary scan register, bypass register)	Active
Exit1-DR	Undefined	High impedance
Pause-DR		
Exit2-DR		
Update-DR		

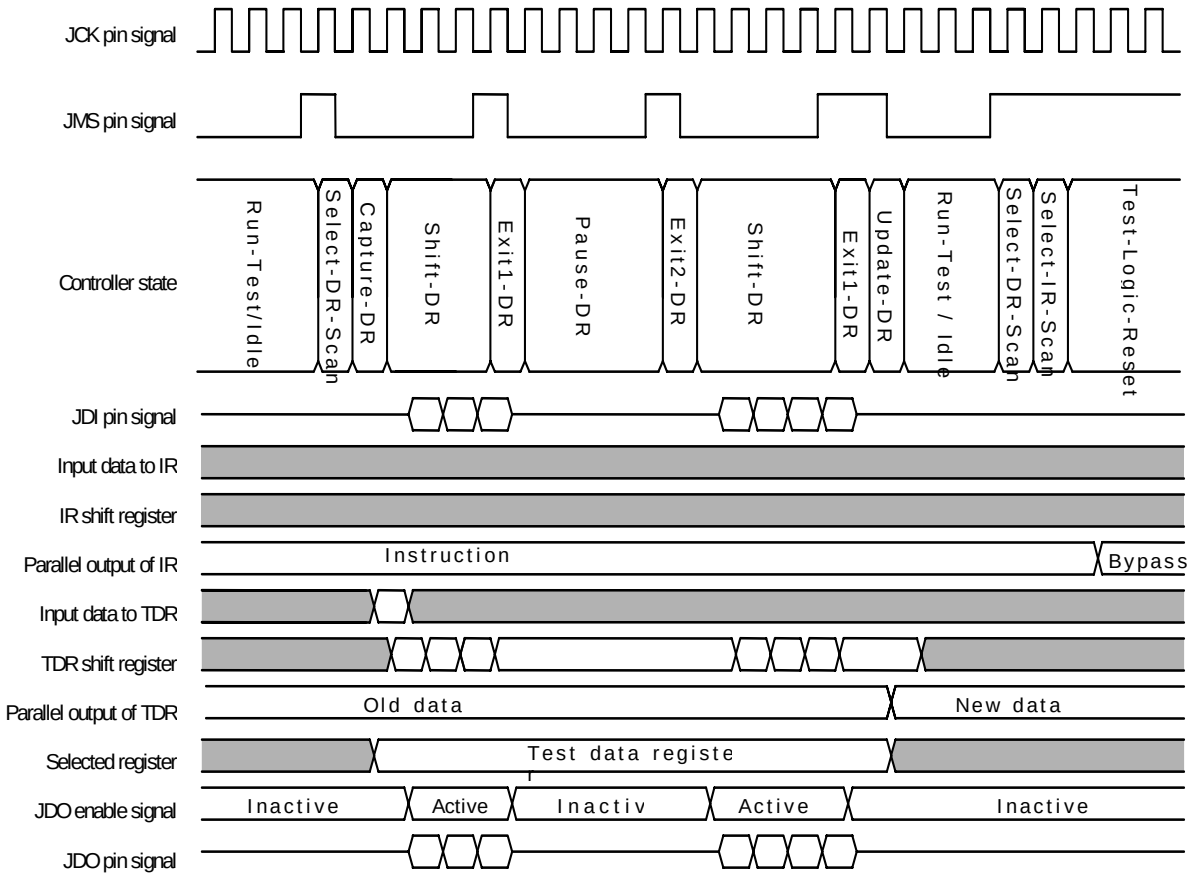
Figure 6-4. Operation of Test Logic (Instruction Scan)



Note TDR (Test Data Register): Boundary scan register and bypass register

Remark ▭ : Don't care or undefined

Figure 6-5. Operation of Test Logic (Data Scan)



Note TDR (Test Data Register): Boundary scan register and bypass register

Remark : Don't care or undefined

6.6 Initializing TAP Controller

The TAP controller is initialized as follows:

(1) The TAP controller is not initialized by the operation of system input such as system reset.

(2) The TAP controller enters the Test-Logic-Reset controller state at the fifth rising edge of the JCK pin signal (while the JMS pin signal is held high).

(3) The TAP controller asynchronously enters the Test-Logic-Reset state when the JRST_B signal is input.

6.7 Instruction Register

This register is defined as follows (see Section 6.2).

(1) The instruction shifted and input to the instruction register is latched so that it changes only in the Update-IR and Test-Logic-Reset controller states.

(2) Data is not inverted since it has been serially input to the instruction register until it is serially output.

(3) A fixed binary pattern data "01" (with LSB (Least Significant Bit) being "1") is loaded to this register cell in the Capture-IR controller state.

(4) A fixed binary pattern data "01" (with LSB (Least Significant Bit) being "1") is loaded to this register cell in the Test-Logic-Reset controller state.

(5) While this register is read, data is output from the JDO pin, starting from the LSB to the MSB, at each falling edge of the JCK pin signal.

The JTAG boundary scan circuit of the mPD98414 can support only the following three instructions depending on the data set to the instruction register.

- BYPASS instruction
- EXTEST instruction
- SAMPLE/PRELOAD instruction

Instruction Register		Supported Instruction
D1	D0	
0	0	EXTEST instruction
0	1	SAMPLE/PRELOAD instruction
1	0	Unused (BYPASS instruction)
1	1	BYPASS instruction

6.7.1 BYPASS Instruction

This instruction is specified by instruction data "11" or "10". This instruction is used to select only the bypass register (to access between the JDI and JDO pins serially) in the Shift-DR controller state.

While this instruction is selected, the operation of the JTAG boundary scan circuit does not affect the operation of the mPD98414.

This bypass instruction is selected while the TAP controller is in the Test-Logic-Reset state.

6.7.2 EXTEST Instruction

This instruction is specified by instruction data "00". In the Shift-DR controller state, this instruction is used to select the boundary scan register of serial access between the JDI and JDO instructions.

• While this instruction is selected:

The states of all the signals driven from the system output pins are completely defined by the data shifted to the boundary scan register. In the Update-DR controller state, the states of all the signals are changed only by the falling edge of the JCK pin signal.

The states of all the signals input from the system input pins are loaded to the boundary scan register at the rising edge of the JCK pin signal while the TAP controller is in the Capture-DR state.

6.7.3 SAMPLE/PRELOAD Instruction

This instruction is specified by instruction data "01". This instruction can execute two functions, SAMPLE and PRELOAD, with a single instruction.

6.7.4 Boundary Scan Data Bit Definition

NEC can supply the BSDL (Boundary Scan Description Language) file for the mPD98414 upon request.

[MEMO]