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Renesas Electronics Corporation

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TTL

General Information

1. Outline

A decrease of storage time-by SBD and a progress of process technology have made a great improvement in the figure of merit (product of speed and power dissipation) of TTL's. The HD74LS series has the same speed as the standard TTL, and the power dissipation of this series has been reduced to improve the figure of merit. As a result the propagation delay time is 10 ns per gate, and the power dissipation is 2 mW. Figure 1 shows a basic gate circuit for HD74LS series. Most of inputs ore provided not with the multiemitter structure but with the diode structure by SBD. The diode structure provides over twice the breakdown voltage compared with the multiemitter structure, so that unused terminal con be connected directly to V_{CC} terminal. When the number of inputs becomes larger, the speed (especially t_{PLH}) sometimes decreases because the capacities in substrate on anode side of diode increase. (For the internal gate in MSI's, the multiemitter structure is used)

A low power dissipation, however, requires a large resistance, which occupies a large area in an usual IC technology. The HD74LS series employs the ion implantation technology by which an efficient resistance/area rate can be achieved at the large resistance part, resulting in a higher degree of integration. Thus, low power shottky TTL's will give full performance in MSI and LSI uses.

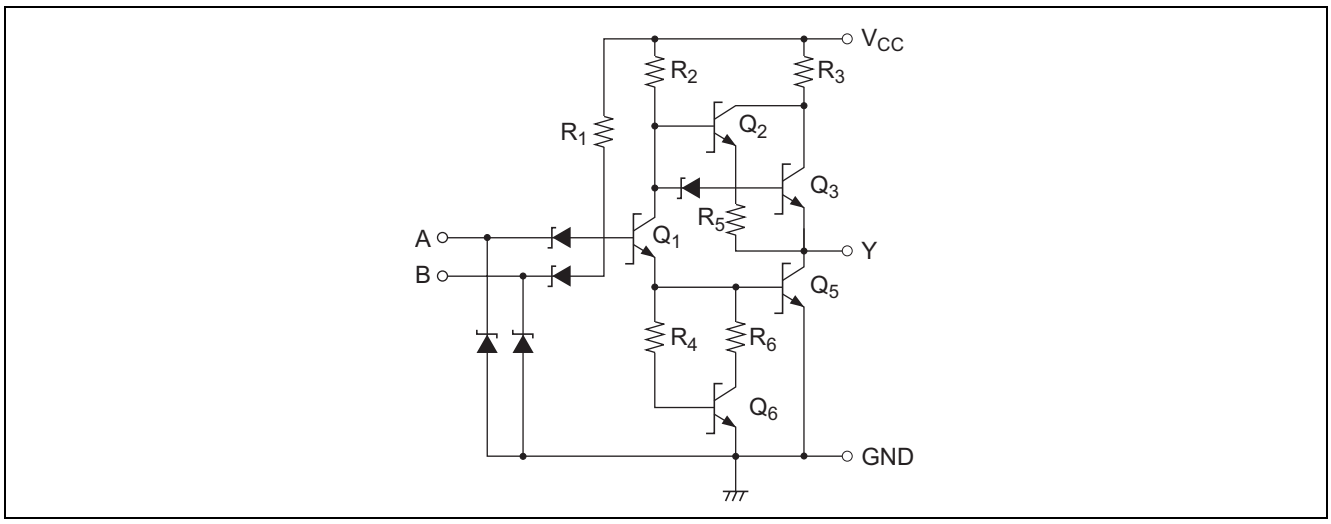

Figure 1 Basic gate

2. Features

The low power dissipation SBD TTL HD74LS series features as follows.

- Wide operating temperature range: –20 to +75°C
- High reliability
- Both ceramic and plastic packages available
- Both packages provide the same characteristics.
- Compatibility:
  HD74LS series are fully compatible with SN74LS series on pin assignment, functions and characteristics.

3. Symbol, Terms, and Definitions

3.1 Explanation of Electrical Characteristics and Recommended Operating Conditions

(1) DC Characteristics

Symbols	Terms	Definitions
V_{IH}	High-level input voltage	An input voltage within the more positive (less negative) of the two ranges of values used to represent the binary variables.
V_{OH}	High-level output voltage	The voltage at an output terminal with input conditions applied that according to the product specification will establish a high level at the output.
V_{IK}	Input clamp voltage	An input voltage in a region of relatively low differential resistance that serves to limit the input voltage swing.
V_{IL}	Low-level input voltage	An input voltage within the less positive (more negative) of the two ranges of values used to represent the binary variables.
V_{OL}	Low-level output voltage	The voltage at an output terminal with input conditions applied that according to the product specification will establish a low level at the output.
V_T^-	Negative-going threshold voltage	The voltage level at a transition-operated input that causes operation of the logic element according to specification as the input voltage falls from a level above the positive-going threshold voltage, V_T^+
$V_{O(off)}$	Off-state output voltage	The voltage at an output terminal with input conditions applied that according to the product specification will cause the output switching element to be in the off state.
$V_{O(on)}$	On-state output voltage	The voltage at an output terminal with input conditions applied that according to the product specification will cause the outputs switching element to be in the on state.
V^+	Positive-going threshold voltage	The voltage level at a transition-operated input that causes operation of the logic element according to specification as the input voltage rises from a level below the negative-going threshold voltage, V_T^-
I_{IH}	High-level input current	The current into an input when a high-level voltage is applied to that input.
I_{OH}	High-level output current	The current into an output with input conditions applied that according to the product specifications will establish a high level at the output.
I_{IL}	Low-level input current	The current into an input when a low-level voltage is applied to that input.
I_{OL}	Low-level output current	The current into an output with input conditions applied that according to the product specifications will establish a low level at the output.
$I_{O(off)}$	Off-state output current	The current flowing into an output with input conditions applied that according to the product specification will cause the output switching element to be in the off state.
I_{OZ}	Off-state (high-impedance-state) output current (of a three-state output)	The current into an output having three-state capability with input conditions applied that according to the product specification will establish the high-impedance state at the output.

(1) DC Characteristics (cont)

Symbols	Terms	Definitions
I_{OS}	Short-circuit output current	The current into an output when that output is short-circuited to ground (or other specified potential) with input conditions applied to establish the output logic level farthest from potential (or other specified potential)
I_{CC}	Supply current	The current into the V_{CC} supply terminal of an integrated circuit.

(2) AC Characteristics

Symbols	Terms	Definitions
f_{max}	Maximum clock frequency	The highest rate at which the clock input of a bistable circuit can be drive through its required sequence while maintaining stable transition of logic level at the output with input conditions established that should cause changes of output logic level in accordance with the specification.
t_{TLH}	Transition time, low-to-high-level	The time between a specified low-level voltage and a specified high-level voltage on a waveform that is changing from the defined low level to the defined high level.
t_{THL}	Transition time, high-to-low-level	The time between a specified high-level voltage and a specified low-level voltage on a waveform that is changing from the defined high level to the defined low level.
t_{PLH}	Propagation delay time, low-to-high-level	The time between the specified reference points on the input and output voltage waveforms with the output changing from the defined low level to the defined high level.
t_{PHL}	Propagation delay time, high-to-low-level	The time between the specified reference points on the input and output voltage waveforms with the output changing from the defined high level to the defined low level.
t_{ZH}	Output enable time (of a three-state output) to high level	The propagation delay time between the specified reference points on the input and output voltage waveforms with the three-state output changing from a high-impedance (off) state to the defined high level.
t_{ZL}	Output enable time (of a three-state output) to low level	The propagation delay time between the specified reference points on the input and output voltage waveforms with the three-state output changing from a high-impedance (off) state to the defined low level.
t_{HZ}	Output disable time (of a three-state output) to high level	The propagation delay time between the specified reference points on the input and output voltage waveforms with the three-state output changing from the defined high-level to a high-impedance (off) state.
t_{LZ}	Output disable time (of a three-state output) to low level	The propagation delay time between the specified reference points on the input and output voltage waveforms with the three-state output changing from the defined low-level to a high-impedance (off) state.
t_w	Pulse width	The time interval between specified reference points on the leading and trailing edges of the pulse waveform.
t_h	Hold time	The interval during which a signal is retained at a specified input terminal after an active transition occurs at another specified input terminal.
t_{su}	Setup time	The time interval between the application of a signal that is maintained at a specified input terminal and a consecutive active transition at another specified input terminal..

(2) AC Characteristics (cont)

Symbols	Terms	Definitions
$t_{release}$	Release time	The time interval between the releases from a specified input terminal of data intended to be recognized and the occurrence of an active transition at another specified input terminal..

3.2 Definitions of Symbol

Symbols	Definitions
H	High level (steady state)
L	Low level (steady state)
↑	Transition from low to high level
↓	Transition from high to low level
×	Irrelevant (any input, including transitions)
Z	Off (high-impedance) state of a 3-state output
a.....h	The level of steady-state inputs at inputs A through H respectively
Qo	Level of Q before the indicated steady-state input conditions are established
$\overline{Qo}$	Complement of Q_O or level of $\overline{Q}$ before the indicated steady-state input conditions are established.
Qn	Level of Q before the most recent active transition indicated ↑ or ↓
	One high-level pulse
	One low-level pulse
TOGGLE	Each output changes to the complement of its previous level on each active transition indicated by ↑ or ↓

Revision Record

Rev.	Date	Description	
		Page	Summary
1.00	Jul.09.04	—	First edition issued

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