
IDT[®]
Tsi310[™] Device Differences

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About this Document

This document describes the functional and physical changes that were implemented in the Revision A version of the Tsi310, part number Tsi310A-133CE. It is intended for Tsi310 designers who are using the Tsi310A-133CE device, and would like to understand the design differences between the Tsi310A-133CE and the Tsi310-133CE.

1. Device Errata Changes

The Tsi310 was modified to fix one device errata. The fix was implemented by only revising the metal layers; the base layers were not modified. The following errata is fixed in the Revision A device:

- Errata 2: PCI/X transaction ordering may not be followed

Note: For more information about this errata, see the *Tsi310 Device Errata* document.

2. Functional Changes

The following functional revisions were made to the netlist:

- Changes to fix errata 2: A logic change was implemented to prevent single dataphase read completions (Memory Read DWORD, I/O Read, or Configuration Type 1 Read) from passing Posted Writes.
- Additional functional changes: A logic change was made so that the bridge will not respond to any cycles besides Type 0 configuration cycles (including Type 1 configuration cycles) when in the D3 hot state. Not responding to a transaction causes a master-abort (that is, the Tsi310 will not assert DEVSEL#).

3. Other Changes

Other changes to the Tsi310 include the following:

- The PCI Revision ID Register at offset 0x08 was incremented to read 0x03 (previously it read 0x02). Please note that the Tsi310A part number, Tsi310A-133CE, corresponds with PCI Revision ID number, 0x03.
- The Version field of the JTAG ID Register was incremented to read 0x3 (previously it read 0x2).
- An alternative package substrate is used in the Tsi310A-133CE. The new substrate has identical form, function, quality, and reliability characteristics as the previous version.



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