Tsi110™ Design Notes

80E5000_DN001_02

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About this Document

This document describes design notes for the Tsi110.

Revision History

80E5000_DN001_02, Formal, October 2009

This document was rebranded as IDT. It does not include any technical changes.

80E5000_DN001_01, Formal, February 2009

This is the first version of the *Tsi110 Design Notes*. There is no new Tsi110 information in this document since the design note information used to reside in the *Tsi110 Device Errata*.

Part Numbers

Part Number	Frequency	Temperature	Package	Pin Count
Tsi110-167CL	167 MHz	Commercial	BGA	1023
Tsi110-167CLY	167 MHz	Commercial	BGA (RoHS)	1023

Design Notes

Design Note	Applicability
	Tsi110-167CL/CLY
"[DN1] Converting PCIXCAP to PCI_PCIXCAP[1:0]"	✓
"[DN2] Recovery from internal PCI timeouts"	✓
"[DN3] Byte swapping for Ethernet Controller"	✓
"[DN4] Boot vector mapping to HLP address"	✓
"[DN5] PCI_CLK and CG_REF clock frequency restrictions"	✓

[DN1] Converting PCIXCAP to PCI_PCIXCAP[1:0]

The *PCI-X Addendum to PCI Local Bus Specification (Revision 1.0a)* provides a recommendation for converting the 3-level PCIXCAP signal to two binary signals. These signals are active low and are named "133 MHz" and "PCIX." If "133 MHz" and "PCIX" are mapped to PCI_PCIXCAP[1] and PCI_PCIXCAP[0] respectively, the sense must be inverted. That is, instead of being active low, active high logic must be used for "133 MHz" and "PCIX."

[DN2] Recovery from internal PCI timeouts

As a target, the PCI/X Interface contains a timer for timing out Switch Fabric requests that are initiated by devices on its PCI/X bus. A timeout on a Switch Fabric access indicates a serious system problem because an access was unable to complete.

If the PCI/X Interface experiences a Switch Fabric timeout error it asserts the following bits in the PFAB_CSR register: TEA, RESP_TIMOUT, and INVLD_RESP. The PCI/X Interface, however, is unable to recover from the error and a software reset must performed by setting MISC_CSR[SOFT_RESET] and PFAB_CSR[SW_RST].

[DN3] Byte swapping for Ethernet Controller

To ensure proper operation of the Ethernet Controller, use one of the following byte swapping configurations.

Hardware cache coherency not used

When hardware cache coherency is not used (that is, the Ethernet Controller accesses memory directly through the Switch Fabric), byte swapping and word swapping must be configured in the following way:

- For buffer descriptors – Byte and word swapping must be enabled so that the Processor Interface and Ethernet Controller have a consistent view of the buffer descriptors.
- For data – No swapping must be enabled so that data is maintained in “network” order.

Hardware cache coherency used

When hardware cache coherency is used (that is, the Ethernet Controller accesses memory through the Processor Bus Master, or PBM), byte swapping and word swapping must be configured in the following way:

- For buffer descriptors – Word swapping must be enabled. Byte swapping must be disabled to account for the byte swapping performed by the Processor Interface.
- For data – Byte swapping must be enabled to cancel the byte swapping performed by the Processor Interface.

From the Processor Interface’s description in the *Tsi110 User Manual*, it indicates that the Ethernet Controller’s configuration for byte and word swap could be the same because the upper address bits could be used to communicate the required swapping to the PBM. However, the Ethernet Controller does not provide control of the full 64-bit internal address space; therefore, it cannot control the Processor Interface’s byte swapping.

[DN4] Boot vector mapping to HLP address

Immediately after a device reset, Tsi110’s BARs are not enabled; however, the following are exceptions:

1. The processor’s PB_OCN_BAR1 has the BOOT bit set which enables this BAR with default address mapping.
2. The HLP’s base address for chip selects 0 and 1 are enabled.

With this configuration, the processor’s boot vector, 0x0_FFF0_0100, is mapped to access the HLP’s chip select 0 using a 24-bit address of 0x00_0100.

The Tsi110 provides a power-up strap to change this default behavior. The PWRUP_PB_BVS strap can be used to change the address mapping so that the HLP’s chip select 0 presents a 24-bit address of 0xF0_0100. In addition, in the Tsi110 power-up straps may be used to change the HLP’s configuration so that a latched 32-bit address is presented: 0x0FF0_0100 (for more information, see the PWRUP_HLP_LATCH signal).

[DN5] PCI_CLK and CG_REF clock frequency restrictions

The Tsi110 uses the CG_REF clock input to generate an internal Switch Fabric clock called OCN clock. The OCN clock frequency, T_{F_OCN}[1], has the same frequency as CG_REF when the Clock Generator is bypassed (that is, $T_{F_OCN} = T_{F_NOPLL}$), and four times the frequency of CG_REF when the Clock Generator is enabled (that is, $T_{F_OCN} = 4 * T_{F_CG}$).

The Tsi110 requires that the PCI_CLK frequency, T_{F_PCI}, always be less than or equal to T_{F_OCN}. Under most cases, this requirement is met by default:

- If Tsi110's CG_PCI_CLKO outputs (or buffered versions of CG_PCI_CLKO) provide the PCI/X bus clock, this requirement is met under all conditions.
- If T_{F_PCI} is 25, 33, 50, 66 or 100MHz, this requirement is met.

The requirement that T_{F_PCI} be less than or equal to T_{F_OCN} can only be violated if PCI_CLK is not driven by CG_PCI_CLKO and T_{F_PCI} is greater than T_{F_OCN}. This requirement may appear to be met but is actually violated under very specific conditions. If both the OCN clock and the PCI/X bus clock are nominally 133MHz but are driven from independent clock sources, the PCI clock may be marginally faster than the OCN clock due to inaccuracies in the clock sources. Enabling spread spectrum on PCI_CLK, in the Clock Generator, or both, increases the amount of the violation.

Care must be taken to ensure that at all times (that is, including the maximum frequency deviations due to accuracy, age, jitter, spread spectrum, and noise), T_{F_OCN} is greater than or equal to T_{F_PCI}. Violating this requirement may degrade PCI/X Interface performance, lead to deadlock, or both.

1. T_{F_NOPLL}, T_{F_CG}, and T_{F_PCI} are specified in the "Electrical Characteristics" section of the *Tsi110 Hardware Manual*. T_{F_OCN} is not specified in the Hardware Manual because it is derived from T_{F_NOPLL} and T_{F_CG}.