Tsi109™/Tsi110™ Device Differences

80E5000_AN001_02

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1. Tsi109/Tsi110 Device Differences

This document summarizes the differences between the Tsi109 and Tsi110. Topics discussed include the following:

Revision History

80E5000_AN001_02, Formal, October 2009

This version of the document was rebranded as IDT. It does not include any technical changes.

80E5000_AN001_01, Formal, February 2007

This is the first version of the *Tsi109/Tsi110 Device Differences*.

1.1 Functional Differences

Table 1: Functional Differences

Function/Feature	Tsi109	Tsi110
Processor Interface		
200-MHz operation	✓	
167-MHz operation	✓	✓
Dual processor support	✓	
MPX support	✓	
60x support	✓	✓
Address and data parity generation	✓	
Memory Interface		
DDR2 at 400-MHz operation	✓	

Table 1: Functional Differences *(Continued)*

Function/Feature	Tsi109	Tsi110
DDR2 at 333-MHz operation	✓	✓
ECC support	✓	

1.2 Register Differences

The following table lists the registers and bits that are defined differently for the Tsi109 and Tsi110.

Table 2: Register Differences

Offset	Register	Bit(s)
Processor Interface		
0x000	PB Identification Register	0:15
0x00C	PB Interrupt Status Register	12, 30, 31
0x010	PB Interrupt Enable Register	12, 30, 31
0x014	PB Interrupt Set Register	12, 30, 31
0x018	PB Arbiter Control Register	22, 29:30
0x400	PB Slave Configuration Register	17, 20, 21, 22
0x404	PB Error Log Register	8:9
0xC00	PB Master Configuration Register	3
Memory Interface		
0x000	SDRAM Control Register	4:7
0x00C	SDRAM Refresh Interval Register	16:31
0x010	SDRAM Interrupt Status Register	26, 27
0x014	SDRAM Interrupt Enable Register	26, 27
0x018	SDRAM Interrupt Set Register	26, 27
0x01C	SDRAM Shadow Interrupt Status Register	26, 27

Table 2: Register Differences

Offset	Register	Bit(s)
PCI/X Interface		
0x000	PB Identification Register	31:16
Clock Generator		
0x20C	Clock Generator Clock Control Register	20, 18:16, 14, 6

1.3 Signal/Pinout Differences

Table 3: Signal/Pinout Differences

Pin Number	Pin Name	
	Tsi109	Tsi110
C14	SD_CB[3]	NC
C15	SD_CB[6]	NC
C19	SD_CB[5]	NC
D15	SD_CB[7]	NC
D16	SD_DQS_N[8]	NC
D17	SD_DQS_N[17]	NC
D18	SD_CB[1]	NC
D19	SD_CB[4]	NC
E16	SD_DQS_P[8]	NC
E17	SD_DQS_P[17]	NC
E18	SD_CB[0]	NC
F15	SD_CB[2]	NC
J32	CG_PB_CLKO[2]	NC
L25	PB_AP[4]	RESERVED[21]
N26	PB_HITn[1]	RESERVED[0]
N27	PB_BRn[1]	NC
N30	PB_AP[2]	RESERVED[19]
N32	PB_AP[3]	RESERVED[20]

Table 3: Signal/Pinout Differences *(Continued)*

Pin Number	Pin Name	
	Tsi109	Tsi110
P25	PB_AP[0]	RESERVED[17]
P29	PB_QACKn[1]	NC
R31	PB_AP[1]	RESERVED[18]
R32	PB_HITn[0]	RESERVED[1]
U29	PB_DTI[0]	PB_DBWOn
V28	PB_BGn[1]	NC
W27	PB_DRDYn[1]	RESERVED[2]
W29	PB_DRDYn[0]	RESERVED[3]
W30	PB_DTI[1]	NC
Y29	PB_DBGn[1]	NC
Y32	PB_DTI[2]	NC
AA28	PB_QREQn[1]	NC
AB26	PB_DP[1]	RESERVED[23]
AB27	PB_DP[0]	RESERVED[22]
AB29	PB_DP[2]	RESERVED[24]
AC31	PB_DP[5]	RESERVED[27]
AC32	PB_DP[7]	RESERVED[29]
AD26	PB_DP[3]	RESERVED[25]
AE22	DMAPE_ACK[0]	RESERVED[4]
AE23	DMAPE_DATA[4]	RESERVED[5]
AE27	PB_DP[4]	RESERVED[26]
AE30	PB_DP[6]	RESERVED[28]
AF23	DMAPE_ACK[1]	RIU
AG22	DMAPE_DATA[1]	RESERVED[6]
AH21	DMAPE_DATA[0]	RESER.VED[7]
AH22	DMAPE_DATA[2]	RESERVED[8]
AH23	DMAPE_DATA[6]	RESERVED[9]
AJ22	DMAPE_DATA[3]	RESERVED[10]

Table 3: Signal/Pinout Differences *(Continued)*

Pin Number	Pin Name	
	Tsi109	Tsi110
AJ23	DMAPE_DATA[7]	RESERVED[11]
AK22	DMAPE_CLKO[0]	RESERVED[12]
AL23	DMAPE_EOD	RESERVED[13]
AL24	DMAPE_CLK	RESERVED[14]
AM22	DMAPE_DATA[5]	RESERVED[15]
AM23	DMAPE_CLKO[1]	RESERVED[16]

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