Tsi108™/Tsi109™ Device Differences

80B5000_AN004_06

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Tsi108/Tsi109 Device Differences

This document summarizes the differences between the Tsi108 and Tsi109. For more information on the feature differences between these devices, see the *Tsi108/Tsi109 User Manual*.

The following topics are discussed:

Revision History

80B5000_AN004_06, Formal, October 2009

This document was rebranded as IDT. It does not include any technical changes.

80B5000_AN004_05, Formal, May 2006

This version includes a new section that explains Clock Generator output differences between the Tsi108 and Tsi109 (see "Clock Generator Output — Turn Off Time" on page 11).

80B5000_AN004_04, Formal, November 2005

This version was revised to support the following product name changes: Tsi108A to Tsi109, Tsi108x to Tsi108/Tsi108, and Tsi108 Family to Tsi108/Tsi109. No technical changes were implemented.

80B5000_AN004_03, Formal, September 2005

The following changes were made to this version:

- Added information that explains why certain Tsi108 registers changed in support of the Tsi109 (see the Description column in Table 2 on page 6).
- Added a Tsi108 register change that was omitted previously from this document (see WAMI in Table 2 on page 6.
- Added information that explains the purpose of multiplexed signals that were added in support of the Tsi109 (see the Description column in Table 3 on page 9)

- Added a section that describes key guidelines for migrating board designs that use the Tsi108 to the Tsi109 (see Section 6 on page 10).

80B5000_AN004_02, Formal, July 2005

The following changes were made to this version:

- Added PB_RSR[PB_BVS] as a new Tsi109 field (see Section 2.1 on page 6).
- Added SD_D{0..1}_CTRL[RBC] as a new Tsi109 field (see Section 2.1 on page 6).
- Added a new multiplexed pin called PWRUP_PB_BVS (see Section 3.1 on page 9).
- Added a table that lists the physical differences between the devices (see Section 5 on page 10).
- Moved HLP_B{0..3}_CTRL1[MODE] to the “Modified Tsi108 Fields” section of this document (see Table 2 on page 6). In the previous version of this document, this bit was incorrectly listed as a new Tsi109 field when it is just modified.
- Changed the document title from Tsi108x Device Differences to *Tsi108 Family Device Differences*.

80B5000_AN004_01, Formal, June 2005

This is the first release of the *Tsi108/Tsi109 Device Differences*.

1. Functional Differences

The functional differences between the Tsi108 and Tsi109 are summarized in the following table.

Table 1: Functional Differences

Function/Feature	Tsi108	Tsi109
Processor Interface		
Dual processor support		✓
IBM 60x processor out of order mode (DBWO)		✓
Processor power management		✓
Address and data parity support on the processor bus	✓	✓
Processor to Memory latency (processor clocks)	13	12
Generated processor bus clocks	3	3
Memory Controller		
Memory power savings modes		✓
ECC support for SDRAM devices	✓	✓
Memory preserve mode for SDRAM devices[a]	✓	
PCI/X Interface		
User-selectable option for pre-driving device address during PCI configuration cycles		✓
CompactPCI Hot Swap support	✓	✓
HLP Interface		
Memory bank width set by PWRUP_HLP_WIDTH signal		✓
Latch/Non-latch mode set by PWRUP_HLP_LATCH signal		✓
Ethernet Controller		
Dual Gigabit Ethernet support	✓	✓
Clock Generator		
Interrupt from Clock Generator		✓

a. SDRAM memory preservation is supported by the Tsi109 using “self-refresh mode.”

2. Register Differences

This section discusses the register differences between the Tsi108 and Tsi109.

2.1 Register Changes to Support Tsi109

The following registers were modified to support the Tsi109.

Table 2: Register Changes to Support Tsi109

Register	Bit	Bit Name	Description
Processor Interface			
PB Identification Register (Offset 0x000)	00:15	TUNDRA_DEV_ID	Device ID. Updated to include a Tsi109 value.
PB Reset Control and Status Register (Offset 0x004)	24	PB_BVS	Boot vector select. This new Tsi109 bit allows the device to map the boot vector to one of two HLP addresses.
PB Bus Master Select Register (Offset 0x008)	23	WAMI	Who-am-I. This new Tsi109 bit allows software to determine its processor number in a dual-processor configuration.
PB Interrupt Status Register (Offset 0x00C)	12	PB_WAKE1	Wake processor features. These new Tsi109 bits are used for processor power management.
	13	PB_WAKE0	
PB Interrupt Enable Register (Offset 0x010)	12	PB_WAKE1_EN	
	13	PB_WAKE0_EN	
PB Interrupt Set Register (Offset 0x014)	12	PB_WAKE1_SET	
	13	PB_WAKE0_SET	
PB Power Management Control Register (Offset 0x01C)	0:31	-	This new Tsi109 register is used for processor power management.
PB Slave Configuration Registers (Offset 0x400)	28	SCPU_OPT	Single CPU optimization. This new Tsi109 bit allows the Processor Interface to optimize performance when used with a single processor.

Table 2: Register Changes to Support Tsi109 *(Continued)*

Register	Bit	Bit Name	Description
Memory Controller			
SDRAM Control Register (Offset 0x000)	02	PWR_DWN	Power-down. This new Tsi109 bit enables SDRAM power-down modes.
	03	SELF_RFSH	Self-refresh enable. This new Tsi109 bit enables SDRAM self-refresh mode.
	04:07	SELF_RFSH_DLY	Self-refresh delay. This new Tsi109 field specifies the delay between the last serviced Processor Interface or Switch Fabric request and the Memory Controller placing the SDRAMs into self-refresh mode.
	24	RPW_DISABLE	Reads-pass-writes disable. This new Tsi109 bit allows RPW to be disabled.
	25	PB_SLOWER	Processor Interface path control. This new Tsi109 bit enable the Memory Controller to optimize the asynchronous path to the Processor Interface.
	31	MEM_PRESERVE	Memory preserve. This new Tsi109 bit forces the device to disable memory preserve mode.
SDRAM DIMM Control Register (Offset 0x020, 0x024)	03	RBC	Row-bank-column address mapping select. This new Tsi109 bit controls the mapping of the internal address to the Row, Bank, Column and Rank-select fields of the multiplexed SDRAM address.
	05:07	CLK_DISABLE	SDRAM clock disable. This new Tsi109 field provides a method to tri-state unused SDRAM output clocks.
PCI/X Interface			
PCI ID Register (Offset 0x000)	31:16	DID	Device ID. Updated to include a Tsi109 value.
PCI Miscellaneous Control and Status Register (Offset 0x040)	14	PRE_DRIVE	PCI (2.3) address pre-drive enable for configuration cycles. This new Tsi109 bit enables a PCI configuration address to be driven four PCI_CLK clock cycles before the assertion of PCI_FRAMEn.
	13	SYS32	32-bit PCI select. This new Tsi109 bit can select 32-bit or 64-bit PCI system operation when the Tsi109 is the PCI central resource.

Table 2: Register Changes to Support Tsi109 *(Continued)*

Register	Bit	Bit Name	Description
PCI SERRn Status Register (Offset 0x048)	07	D_TOUT	In the Tsi109, these interrupt status bits can be set even if SERR_EN is not enabled or asserted. In the Tsi108, these interrupt status bits are asserted only if SERR_EN is enabled; in which case, PCI_SERRn is also asserted.
	06	DR_ND	
	05	DW_ND	
	04	PW_MA	
	03	PW_TA	
	02	PW_RETRY	
	01	PW_DPE	
	00	APE	
DMA Controller			
DMA General Control and Status Register (0ffset 0x024, 0x124, 0x224, and 0x324)	24	SOFT_RST	Software reset. This bit is used by the Tsi108 and Tsi109 to reset a DMA channel.
HLP Interface			
HLP_B{0..3}_CTRL0 Register (Offsets 0x008, 018, 028, 038)	01:00	WIDTH	Bank width. This new Tsi109 field indicates whether the HLP bank width is set as 8-, 16-, or 32-bits wide. For the Tsi109, this field is set by the PWRUP_HLP_WIDTH signal.
HLP_B{0..3}_CTRL1 Register (Offsets 0x00C, 01C, 02C, 03C)	31	MODE	Mode of operation (Latch or Non-latch). This bit was updated for Tsi109 so that its reset state is set by the PWRUP_HLP_LATCH signal.
Clock Generator			
Clock Generator Interrupt Status Register (Offset 0x200)	19:16	LOL	Loss of lock. In the Tsi108, these interrupt bits are set but the Clock Generator does not provide an interrupt output to the Interrupt Controller. In the Tsi109, these interrupts can be routed through the Interrupt Controller.
Clock Generator Output Control Register (Offset 0x230)	26:24	PB_PD_EN	Processor bus power-down enable. This new Tsi109 field enables the corresponding Processor Interface output clocks to be held in a static state when the processors are in deep-sleep mode.

Table 2: Register Changes to Support Tsi109 *(Continued)*

Register	Bit	Bit Name	Description
Clock Generator Power-up Option Status Register (Offset 0x234)	9	HLP_LATCH	HLP latch mode. This new Tsi109 bit indicates the status of the HLP latch mode. The latch mode is based on the power-up value of the PWRUP_HLP_LATCH signal.
Clock Generator PVT Control Register (Offset 0x240)	31:0	-	This register is new for the Tsi109; however, it is not used by the Tsi108 or the Tsi109.

3. Signal/Pinout Differences

This section discusses the signal differences between the Tsi108 and Tsi109.

3.1 Signal Changes to Support Tsi109

The following multiplexed signals were added to the Tsi109; they are not used by the Tsi108. Please note, however, there are no pinout differences between the two devices.

Table 3: Signal Changes to Support Tsi109

Signal Name	Note	Pin Number	Description
PWRUP_HLP_LATCH	This signal is multiplexed with HLP_AD[9].	G6	This signal selects the HLP latch mode: Non-latch or Latch.
PWRUP_HLP_WIDTH	These signals are multiplexed with HLP_AD[4:3].	H3, H2	This signal selects the width of the HLP bus: 8-, 16-, or 32-bit.
PWRUP_PB_BVS	This signal is multiplexed with HLP_AD[14]	J7	This signal selects the processor boot vector select.

4. Electrical Differences

There are no electrical differences between the Tsi108 and Tsi109.

5. Physical Differences

The following table lists the physical differences between the Tsi108 and Tsi109.

Table 4: Physical Differences

Physical Difference	Tsi108	Tsi109
Support for Commercial operating temperature range	✓	✓
Support for Industrial operating temperature range		✓
Lead balls	✓	✓
Lead-free balls	✓	✓
Package size: 33 x 33 mm	✓	✓
Ball pitch: 1.0 x 1.0 mm	✓	✓
Ball matrix: 32 x 32	✓	✓
Ball count: 1023	✓	✓

6. Migrating from Tsi108 to Tsi109

This section discusses the power-up differences that must be considered when migrating a board design that uses the Tsi108 to the Tsi109.

6.1 Power-up Considerations

The Tsi109 contains three power-up options that are not available to the Tsi108: PWRUP_HLP_WIDTH, PWRUP_HLP_LATCH, and PWRUP_PB_BVS (see below). If you are migrating a board design from the Tsi108 to the Tsi109, then one of the following methods for managing the power-up differences must be implemented:

1. Pull the power-up signals to the desired state using pull-up or pull-down resistors.
2. Use a serial EEPROM to set the power-up options to a defined state. The EEPROM values will overwrite the initial values that were latched at power-up before any CPU or PCI/X access is accepted by the Tsi108.

6.2 New Tsi109 Power-up Options

The Tsi109 adds the following power-up options (the Tsi108 default value for each power-up option is also listed):

- HLP_AD[4:3] — PWRUP_HLP_WIDTH (Power-up HLP width):
  - 00 = 8-bit bus (Tsi108 default state)
  - 01 = 16-bit bus
  - 10 = 32-bit bus
  - 11 = Reserved for future use

    Note: This option is configured through PWRUP_HLP_WIDTH[WIDTH].
- HLP_AD[9] — PWRUP_HLP_LATCH (HLP latch mode select):
  - 0 = Latch mode
  - 1 = Non-latch mode (Tsi108 default state)

    Note: This option is configured through HLP_B{0..3}_CTRL1[MODE].
- HLP_AD[14] — PWRUP_PB_BVS (Processor boot vector select):
  - 0 = Maps boot vector 0x0_FFF0_0100 to HLP address 0x0_0000_0100 (Tsi108 default state)
  - 1 = Maps boot vector 0x0_FFF0_0100 to HLP address 0x0_0FF0_0100

    Note: This option is configured through PB_RSR[PB_BVS].

6.3 Clock Generator Output — Turn Off Time

The amount of time the Tsi108 Clock Generator and the Tsi109 Clock Generator outputs remain active upon receiving a hardware reset differs. The Tsi108 keeps the output clocks active for approximately 300 cycles upon receiving a hardware reset, while the Tsi109 stops the clock outputs immediately upon hardware reset assertion.

The clock turn off time should not affect most designs because the *Tsi108/Tsi109 User Manual* indicates the removal of the Clock Generator output clocks upon a hardware reset. Designs that use programmable devices that need an input clock to program up while a hardware reset is asserted should take this into consideration.

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