Tsi108™/Tsi109™ Debug Checklist

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About this Document

This document describes some of the common issues that may be encountered when debugging boards configured with the Tsi108 or Tsi109. The following issues are discussed:

1. Voltages/Sequencing

Check the input voltages to the Tsi108/Tsi109 to ensure the Core and I/O voltages are at the proper levels (for more information, see the *Tsi108/Tsi109 User Manual*.

Verify correct power-up sequencing. The Tsi108/Tsi109 has strict voltage sequencing requirements that must be followed (for more information, see the *Tsi108/Tsi109 Hardware Manual*).

2. Clocks

The Tsi108/Tsi109 contains an integrated Clock Generator that allows it to generate independent clocks for the Processor Interface, Memory Controller, PCI/X Interface, and internal logic. These clocks are all generated from a single reference clock input, CG_REF.

2.1 Quality of the Clocks

The various output clocks provided by the Tsi108/Tsi109 are derived from a 33-MHz reference clock input, CG_REF. The design contains various PLLs and dividers that allow the Tsi108/Tsi109 to supply the output clocks at the required frequencies. Since all clocks are derived from the single reference clock input, it is extremely important that CG_REF originate from a clean source. For this reason, make sure the 1.8V output of the crystal oscillator is a clean 33-MHz output.

Once the quality of the input clock is successfully verified, the individual Tsi108/Tsi109 output clocks should be checked to verify proper frequency. The values placed on the Tsi108/Tsi109 CG_PB_SELECT[2:0] and CG_SD_SELECT[2:0] determine the Processor bus and Memory bus output clock frequencies, and whether or not the Processor Interface and Memory Controller run synchronously or asynchronously. CG_PB_SELECT[2:0] and CG_SD_SELECT[2:0] are sampled at power-up and must be terminated correctly for the application.

The PCI/X output clock frequencies are determined by the values placed on Tsi108/Tsi109 PCIX_CAP[1:0] inputs at power-up when the Tsi108/Tsi109 is being used as the PCI/X host. The Tsi108/Tsi109 Clock Generator should not be used when the Tsi108/Tsi109 is configured as an agent on the PCI/X bus (that is, PCI_RSTn is configured as an input). In this case the PCI/X clock input to the Tsi108/Tsi109, PCI_CLK, must be clean and match what is driven on the PCI/X initialization pattern at power-up.

3. Reset

The Tsi108/Tsi109 implements various reset inputs as well as outputs. The application will dictate how the Tsi108/Tsi109 is reset as well as the other devices in the system. The majority of Tsi108/Tsi109 applications use the bridge as the system host where the Tsi108/Tsi109 gets its reset input, OCN_RSTn, and drives the various resets to the Processor and PCI/X agents. (For more information on Tsi108/Tsi109 resets, see the *Tsi108/Tsi109 User Manual*.)

The following items should be checked at power-up:

- Reference Clock input, CG_REF, must be valid and stable before reset is released even if the Clock Generator is not being used to generate the various output clocks since this input provides the internal Switch Fabric clock to the Tsi108/Tsi109.
- For designs that do not use the Tsi108/Tsi109 Clock Generator to provide clocks to the various interfaces, the SD_SYSCLK, PB_SYSCLK, and PCI_CLK inputs must be running and stable before reset is released.
- Power-up options are latched at the negation of reset. Make sure the proper values are being latched at power-up. The status of these power-up straps can be determined by reading the CG_PWRUP_STATUS register.

The Tsi108/Tsi109 clock outputs stop during a reset when the Tsi108/Tsi109 Clock Generator provides the system clocks. The Tsi108 differs from the Tsi109 regarding the output clocks. The Tsi108 keeps the output clocks running for up to 300 cycles upon the assertion of reset, while the Tsi109 stops the output clocks immediately upon sensing a reset assertion. For designs that use an FPGA to control the resets, ensure it has a valid clock.

4. Other Issues

This section discusses various issues that were observed when bringing up a Tsi108/Tsi109 board in our lab or in customers' labs.

4.1 Incorrect Power-up Configuration Latched

When using weak pull-up resistors (10K) on the Tsi108/Tsi109 Power-up Configuration signals it is possible to latch an incorrect value when the reset is not held long enough (that is, released immediately). To prevent this problem, ensure the Tsi108/Tsi109 receives its reset input asserted long enough for the power-up strap to register a high. IDT recommends using 4.7K pull-ups on these power-up straps.

4.2 Processor Boot Vector Select

The Tsi108 maps the Processor BOOT vector (0x0_FFF0_0100) to Tsi108 HLP address 0x0_0000_0100. Designers that are familiar with the Tsi107 expect the Processor BOOT vector to be mapped to HLP address 0x0_0FF0_0100. Make sure Flash exists at 0x0_0000_0100 when using the Tsi108 unless an EEPROM is implemented to adjust the default HLP BOOT address.

The Tsi109 introduces a new power-up configuration strap to make the HLP address mapping selectable.

4.3 Random Reads to PB_OCN_SYNC_GEN and PFAB_SYNC_BAR

The Tsi108/Tsi109 Switch Fabric uses a synchronization method called SYNC packets to flush its buffers between selected Switch Fabric ports (for example, between the Processor and PCI/X Interfaces). A read from either the PB_OCN_SYNC_GEN register or the PFAB_SYNC_BAR register will generate a SYNC request packet. The priority of a SYNC request packet is set such that it is not allowed to pass either write or completion packets in any queue. The SYNC packet can be used to determine if the path from one Tsi108/Tsi109 port to another is clean, such that there are no write or completion packets within the internal buffers.

The consequences of reading PB_OCN_SYNC_GEN or PFAB_SYNC_BAR with invalid destination ports are a possible device lock up. Having the destination ports set to any value other than those specified in the PB_OCN_SYNC_DATA register or the PFAB_SYNC_BAR register may cause the Tsi108/Tsi109 internal buffers to lock out and not accept any transactions. Since the reset value of the registers that determine valid SYNC packet destination ports are reset to zero, any random read to the PB_OCN_SYNC_GEN or PFAB_SYNC_BAR is not recommended (or more information on these registers, see the *Tsi108/Tsi109 User Manual*).

4.4 HLP Data Swap Control

The Tsi108/Tsi109 HLP Interface can swap data from the device connected to it before returning the read data to the Switch Fabric, or before writing Switch Fabric data to the device. The data swap feature is controlled by HLP_DATA_SWAP_CTRL[DATA_SWAP] while the PWRUP_HLP_BSWP pin controls the reset value of the DATA_SWAP bit.

The data swapping feature should be used with care because it can produce unpredictable results if any of the data on a Switch Fabric datum is invalid. When using the data swap feature, all address and data must be 64-bit (8-byte) aligned.