



# Tsi108 Design Notes

80B5000\_DN001\_02

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## About this Document

This document describes design notes about the Tsi108.

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## Related Information

*Tsi108 Device Errata*

## Revision History

### **80B5000\_ER001\_02, October 2009**

This document was rebranded as IDT. It does not include any technical changes.

### **80B5000\_ER001\_01, February 2009**

This is the first version of the *Tsi108 Design Notes*. There is no new Tsi108 information in this document since the design note information used to reside in the *Tsi108 Device Errata*.

## Part Number Information

Part Number	Frequency	Temperature	Package	Pin Count
Tsi108-200CL	200 MHz	Commercial	BGA	1023
Tsi108-200CLY	200 MHz	Commercial	BGA (RoHS)	1023

## Device Notes

This section discusses design notes for the Tsi108. Design notes are unique or unintended functional characteristics of the device that may or may not be described in the *Tsi108/Tsi109 User Manual*.

**Table 1: Design Notes Summary**

Design Note	Applicability
	Tsi108-200CL/CLY
"[DN1] Resistor selection for IDSEL" on page 4	✓
"[DN2] Converting PCIXCAP to PCI_PCIXCAP[1:0]" on page 5	✓
"[DN3] Recovery from internal PCI timeouts" on page 5	✓
"[DN4] Byte swapping for Ethernet Controller" on page 5	✓
"[DN5] Boot vector mapping to HLP address" on page 6	✓
"[DN6] PCI_CLK and CG_REF clock frequency restrictions" on page 6	✓
"[DN7] Overshoot on HLP I/O pins" on page 7	✓

### [DN1] Resistor selection for IDSEL

The IDSEL signal is frequently resistively coupled to an address signal in PCI systems. In PCI-X based systems, this resistor is specified as a 2k-Ohm resistor. In PCI (2.3) based systems, the resistance is not specified. In both PCI and PCI-X systems, the system designer must ensure the resistance, bus frequency, and the capacitive loading on IDSEL are such that IDSEL is within valid logic levels when it is sampled during configuration accesses.

The *PCI-X Addendum to PCI Local Bus Specification (Revision 1.0a)* requires the configuration address to be driven for four clock cycles before the assertion of FRAME<sub>n</sub>. This provides five clock cycles for the master to drive the address, charge the IDSEL capacitance, and meet the target devices' setup requirements. The designer should ensure that IDSEL is charged to a valid logic level within the timing constraints of the system.

The *PCI Local Bus Specification (Revision 2.3)* does not specify the resistance for driving IDSEL, nor that the address be driven prior to the configuration cycle. The Tsi108 does not provide the address prior to the configuration cycle. The user must ensure that the resistor chosen to charge IDSEL is sized such that IDSEL is charged to a valid logic level within the timing constraints of the system and the capacitive loading of the system.

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System designers wishing to support both PCI(2.3) and PCI-X with a single resistor value should choose this resistance to be as high as possible while still meeting charge-time requirements. Because the Tsi108 automatically selects PCI(2.3) or PCI-X mode based on the PCIXCAP signals, the resistance chosen must work for both four clocks of pre-drive and zero clocks of pre-drive and the desired frequencies.

### **Recommendation**

The recommended resistor size depends on system design and the load it presents on the IDSEL signal. In most cases, however, a 165-Ohm resistor will be sufficient.

## **[DN2] Converting PCIXCAP to PCI\_PCIXCAP[1:0]**

The *PCI-X Addendum to PCI Local Bus Specification (Revision 1.0a)* provides a recommendation for converting the 3-level PCIXCAP signal to two binary signals. These signals are active low and are named “133 MHz” and “PCIX.” If “133 MHz” and “PCIX” are mapped to PCI\_PCIXCAP[1] and PCI\_PCIXCAP[0] respectively, the sense must be inverted. That is, instead of being active low, active high logic must be used for “133 MHz” and “PCIX.”

## **[DN3] Recovery from internal PCI timeouts**

As a target, the PCI/X Interface contains a timer for timing out Switch Fabric requests that are initiated by devices on its PCI/X bus. A timeout on a Switch Fabric access indicates a serious system problem because an access was unable to complete.

If the PCI/X Interface experiences a Switch Fabric timeout error it asserts the following bits in the PFAB\_CSR register: TEA, RESP\_TIMEOUT, and INVLD\_RESP. The PCI/X Interface, however, is unable to recover from the error and a software reset must be performed by setting MISC\_CSR[SOFT\_RESET] and PFAB\_CSR[SW\_RST].

## **[DN4] Byte swapping for Ethernet Controller**

To ensure proper operation of the Ethernet Controller, use one of the following byte swapping configurations.

### **Hardware cache coherency not used**

When hardware cache coherency is not used (that is, the Ethernet Controller accesses memory directly through the Switch Fabric), byte swapping and word swapping must be configured in the following way:

- For buffer descriptors – Byte and word swapping must be enabled so that the Processor Interface and Ethernet Controller have a consistent view of the buffer descriptors.
- For data – No swapping must be enabled so that data is maintained in “network” order.

## Hardware cache coherency used

When hardware cache coherency is used (that is, the Ethernet Controller accesses memory through the Processor Bus Master, or PBM), byte swapping and word swapping must be configured in the following way:

- For buffer descriptors – Word swapping must be enabled. Byte swapping must be disabled to account for the byte swapping performed by the Processor Interface.
- For data – Byte swapping must be enabled to cancel the byte swapping performed by the Processor Interface.

From the Processor Interface's description in the *Tsi108/Tsi109 User Manual*, it indicates that the Ethernet Controller's configuration for byte and word swap could be the same because the upper address bits could be used to communicate the required swapping to the PBM. However, the Ethernet Controller does not provide control of the full 64-bit internal address space; therefore, it cannot control the Processor Interface's byte swapping.

## [DN5] Boot vector mapping to HLP address

Immediately after a device reset, Tsi108's BARs are not enabled; however, the following are exceptions:

1. The processor's PB\_OCN\_BAR1 has the BOOT bit set which enables this BAR with default address mapping.
2. The HLP's base address for chip selects 0 and 1 are enabled.

With this configuration, the processor's boot vector, 0x0\_FFF0\_0100, is mapped to access the HLP's chip select 0 using a 24-bit address of 0x00\_0100.

## [DN6] PCI\_CLK and CG\_REF clock frequency restrictions

The Tsi108 uses the CG\_REF clock input to generate an internal Switch Fabric clock called OCN clock. The OCN clock frequency,  $T_{F\_OCN}^1$ , has the same frequency as CG\_REF when the Clock Generator is bypassed (that is,  $T_{F\_OCN} = T_{F\_NOPLL}$ ), and four times the frequency of CG\_REF when the Clock Generator is enabled (that is,  $T_{F\_OCN} = 4 * T_{F\_CG}$ ).

The Tsi108 requires that the PCI\_CLK frequency,  $T_{F\_PCI}$ , always be less than or equal to  $T_{F\_OCN}$ . Under most cases, this requirement is met by default:

- If Tsi108's CG\_PCI\_CLKO outputs (or buffered versions of CG\_PCI\_CLKO) provide the PCI/X bus clock, this requirement is met under all conditions.
- If  $T_{F\_PCI}$  is 25, 33, 50, 66 or 100MHz, this requirement is met.

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1.  $T_{F\_NOPLL}$ ,  $T_{F\_CG}$  and  $T_{F\_PCI}$  are specified in the "Electrical Characteristics" section of the *Tsi108/Tsi109 Hardware Manual*.  $T_{F\_OCN}$  is not specified in the Hardware Manual because it is derived from  $T_{F\_NOPLL}$  and  $T_{F\_CG}$ .

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The requirement that  $T_{F\_PCI}$  be less than or equal to  $T_{F\_OCN}$  can only be violated if  $PCI\_CLK$  is not driven by  $CG\_PCI\_CLKO$  and  $T_{F\_PCI}$  is greater than  $T_{F\_OCN}$ . This requirement may appear to be met but is actually violated under very specific conditions. If both the OCN clock and the PCI/X bus clock are nominally 133MHz but are driven from independent clock sources, the PCI clock may be marginally faster than the OCN clock due to inaccuracies in the clock sources. Enabling spread spectrum on  $PCI\_CLK$ , in the Clock Generator, or both, increases the amount of the violation.

Care must be taken to ensure that at all times (that is, including the maximum frequency deviations due to accuracy, age, jitter, spread spectrum, and noise),  $T_{F\_OCN}$  is greater than or equal to  $T_{F\_PCI}$ . Violating this requirement may degrade PCI/X Interface performance, lead to deadlock, or both.

## [DN7] Overshoot on HLP I/O pins

Overshoot and undershoot specifications exist in the *Tsi108/Tsi109 Hardware Manual* for all 3.3V I/O interfaces. The Tsi108 HLP I/Os are especially sensitive to overshoot, and failure to comply with this specification can result in permanent damage to the Tsi108. Care must be taken to ensure that the specified overshoot is not exceeded.

For more information about the overshoot and undershoot specifications, see the “Electrical Characteristics” section of the *Tsi108/Tsi109 Hardware Manual*.



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