ISL6288x Products

VR_ON Timing Guidelines

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Introduction

The rise time of the VR_ON signal must be designed such that the internal circuitry can tolerate noise dips to prevent improper soft-start of the controller. This document aids the user in designing the VR_ON circuitry.

The VR_ON signal is simply used by the controller to determine when to begin the soft-start sequence. Depending on the placement and layout of components around the controller, the magnitude of noise which could couple onto the VR_ON signal can vary. Typically a capacitor is placed on the VR_ON pin to provide decoupling of the signal from noise. Adjusting the rise time of the VR_ON signal can also address potential issues due to noise induced changes in the signal level.

Rise Time Analysis

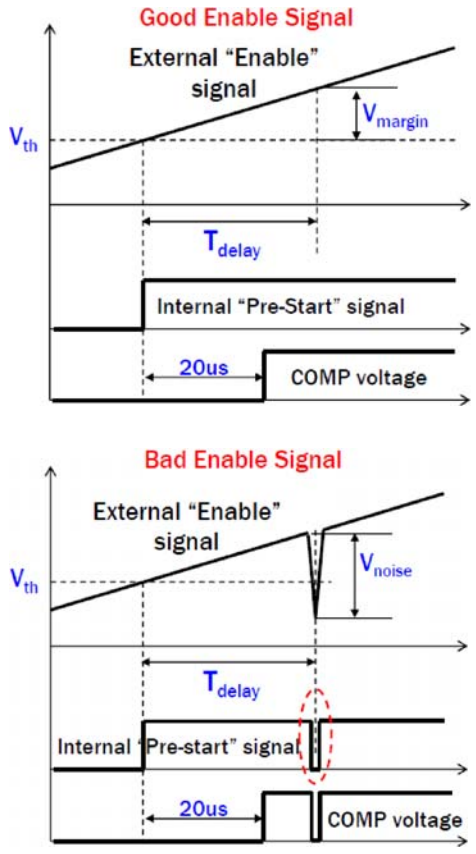

FIGURE 1.

Figure 1 shows two scenarios, one for a good and the other for a bad VR_ON signal. The V_{th} level represents the threshold at which the controller will begin the soft-start sequence as described in the datasheet. Once the VR_ON signal exceeds this threshold, an internal "Pre-Start" signal sets soft-start operation in motion. T_{delay} is a time delay which is typically 24µs, but has a minimum of 15µs. This is the delay in locking in the soft-start activity and this provides a measure of the voltage margin the controller can tolerate, V_{margin}. The COMP pin voltage will begin to rise 20µs after VR_ON exceeds the V_{th} threshold as the internal circuitry is beginning to power up. This all occurs during the 800µs delay time shown in the datasheet during which time the output voltage is not moving.

In the case of a bad enable signal, a noise event occurs during the T_{delay} time which drops VR_ON more than the V_{margin} level. This results in an internal glitch on the Pre-Start signal since the V_{th} threshold has been exceeded again. This can result in a failure to soft-start properly due to the glitch on the Pre-Start signal. In order to prevent noise related glitches from occurring, V_{margin} must be greater than V_{noise}.

The rise time of the VR_ON signal cannot be faster than 12µs. This allows the internal soft-start circuitry time to wake up once VDD is applied. A 15µs rise time on VR_ON is recommended for applications which require a fast rise time to provide margin above the 12µs outlined previously. The rise time is not recommended to be slower than 500µs. This prevents slow moving VR_ON signals from encountering issues due to noise. If a slower rise time on VR_ON is needed, then Equation 1 must be met to prevent soft-start issues.

$$\text{VR\_ON Total Rise Time} < \frac{\text{VR\_ON Logic Level}}{\left[\frac{\text{Noise Level}_{max}}{T_{delay_{min}}}\right]} \quad \text{(EQ. 1)}$$

For example, if a noise level of 30mV is the maximum in a design. Then, using a typical logic level of 3.3V that VR_ON is rising to and the T_{delay} minimum timing of 15µs, the total rise time VR_ON must be below calculates to be 1.65ms. See the calculation below in Equation 2:

$$\frac{3.3V}{\left[\frac{30mV}{15\mu s}\right]} = 1.65ms \quad \text{(EQ. 2)}$$

For a 30mV noise level, the rise time of VR_ON must be faster than 1.65ms for V_{margin} to be greater than V_{noise} to prevent soft-start issues due to noise glitches on VR_ON. The noise level used in the calculation must be worse case expectation to accurately predict and prevent soft-start issues.

A second area of concern with soft-start is the state of the VID pin pull-up voltage at the time VR_ON is applied or removed. The pull-up voltage must be present prior to VR_ON rising or enabling the controller. If the pull-up voltage is not present, the controller will read the improper VID code prior to soft-start. The pull-up voltage for the VID pins must also be present during the time VR_ON is falling until the controller is disabled. Without proper voltage available for the VID pins during either VR_ON event, the controller can get incorrect VID information which can result in improper operation. For example, if the pull-up voltage is not available prior to or during VR_ON rising and enabling the controller, the VID information decoded for soft-start output voltage would be all zeros for the VIDs. This results in the output voltage being programmed to 1.50V, which could be well beyond the level desired by design of the system.

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