Going Beyond the HD-6409 Data Sheet

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Oscillator

The oscillator circuit provides the clock signal for the entire HD-6409 Encoder/Decoder. The oscillator may be used by connecting a crystal between the IX and OX inputs, or IX may be driven by an external clock. The clock output (CO) is provided as a buffered output of the IX clock.

All gates of the oscillator circuit will be exercised when using a crystal to drive the HD-6409. The CO output should be tested to ensure it follows the IX clock input.

Decoder Section

Bipolar Data Converter

The Bipolar Data Converter provides input for Manchester data at the BOI (Bipolar One Input) BZI (Bipolar Zero Input) and UDI (Unipolar Data Input). The UDI Input will accept only non-inverted BOI while the BOI and BZI inputs will accept data from differential input such as a comparator sense transformer and convert it to unipolar data through the use of a latch and feedback gating. The incoming Manchester data is latched by the 16x or 32x oscillator clock thereby obtaining 16 or 32 data samples per bit period. These data samples are then passed on to the Edge Detect and Digital Phase Lock Loop Circuit.

The Bipolar Data Converter will be fully exercised by using either the decoder or repeater modes and functionally testing the HD-6409, both with the unipolar input and the bipolar input pair.

Edge Detector

The Edge Detector Circuit continuously monitors incoming Manchester data by latching it with the 16x or 32x oscillator clock. It then compares consecutive data samples by EXCLUSIVE–OR and identifies when a data edge (i.e. transition from ‘0’ to ‘1’ or ‘1’ to ‘0’) has occurred. The Edge Detector signal is passed to the DPLL circuit for sample timing purposes.

All Portions of the Edge Detector circuit are exercised during a standard decoder or repeater operation.

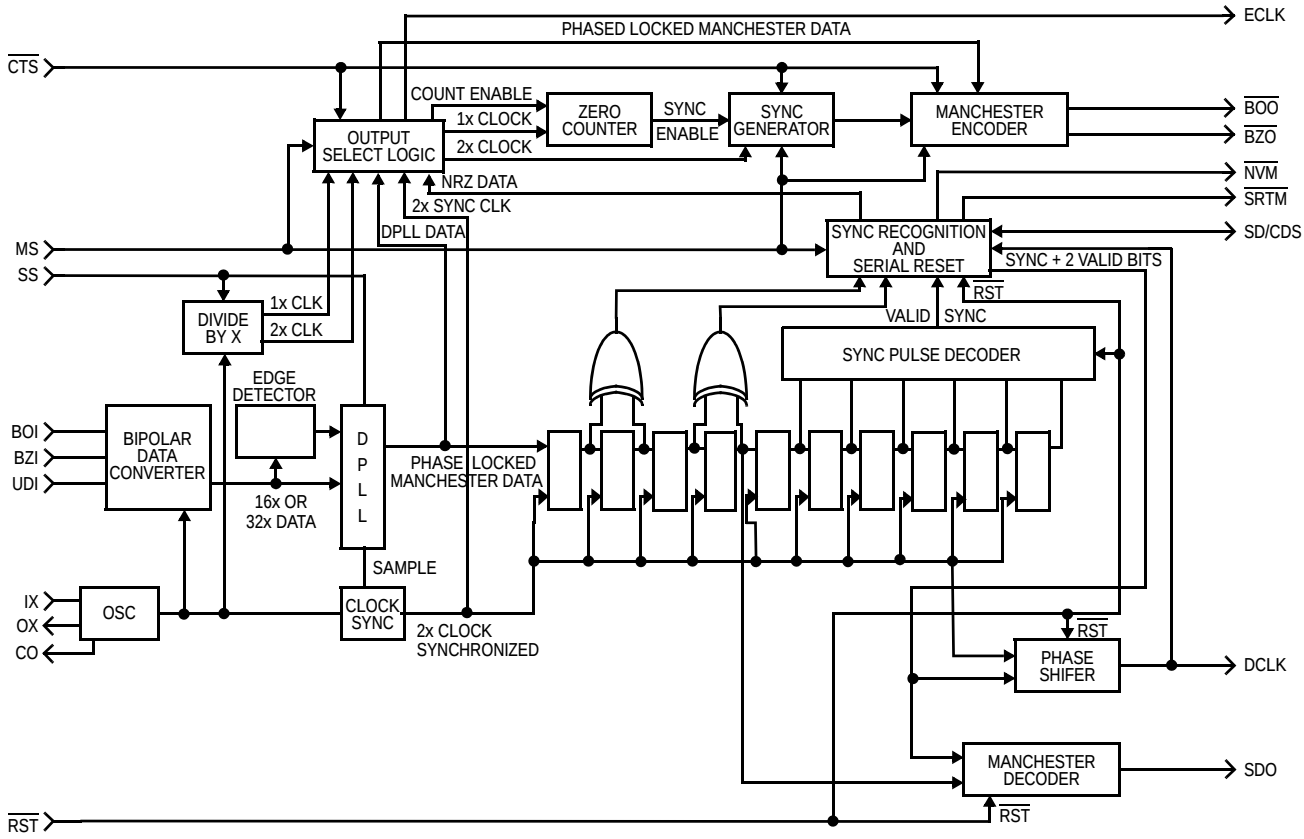


FIGURE 1. HD-6409 BLOCK DIAGRAM

Digital Phase Lock Loop

The DPLL (Digital Phase Lock Loop) circuit provides the synchronizer for the HD-6409. The purpose of the synchronizer is to ensure that the receiver samples the incoming data at a point furthest from the data transition. This is necessary since signal waveforms have non-zero rise and fall times, and the data will be most stable at a point furthest from any data transitions. The DPLL circuit makes use of the 16x or 32x Clock, the Edge Detector and the Sample Counter. Depending upon whether the 16x or 32x speed is selected, two data points, Mid Count and End Count are initialized. Mid Count is nominally the time when the decoder expects a data transition, and End Count is the time when the decoder expects to sample. A sample is actually taken at one of two places, End Count or a Computed Final Count, based upon where data transition actually occurs with respect to Mid Count. If a transition occurs earlier than expected, the sample is taken one clock cycle early. If the transition occurs late, the sample is taken one clock cycle late. If no transition occurs, the sample is taken at the End Count. The advantage of the above algorithm and the DPLL synchronizer is that it can make adjustments for phase in either direction.

Decoder Sampling Timing Diagram

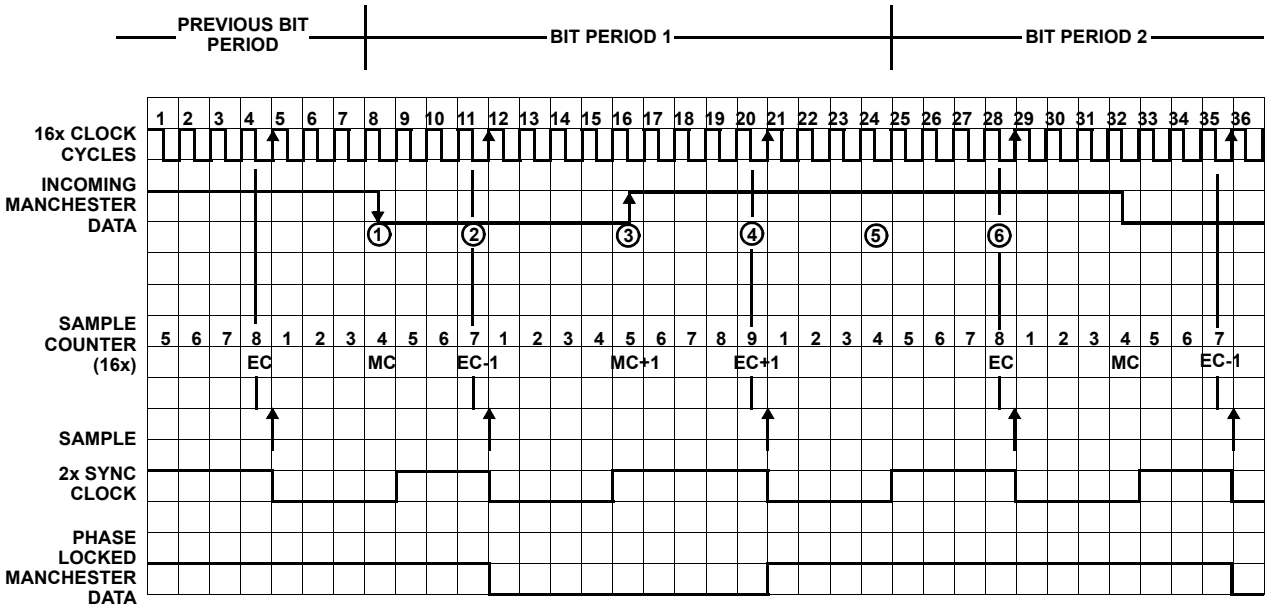
Figure 2 shows examples of the Manchester data transitions occurring earlier than expected, later than expected and not at all. In the first case, the transition occurs at Mid Count ①, which the algorithm considers early, so the sample occurs at EC-1 ②. In the second case, the transition occurs late at MC+1 ③, and the sample is taken at EC+1 ④. The last case contains no transition at the time expected ⑤, so the sample is taken at the End Count ⑥.

Since the DPLL will make phase adjustments in either direction, the circuit may be tested by adjusting the Manchester data so that the transition randomly occurs at up to ±3 oscillator clock periods from the mid-bit position. The DPLL circuit should adjust it's sampling accordingly and give the correct decode results.

Clock Synchronizer

The Clock Synchronizer circuit provides the decoder with a clock signal of 2 times the data rate synchronized with the phase locked Manchester data. This circuit consists of a low-time counter which counts to a value of 4 or 8 depending upon the speed selected, and toggles the clock to a high level. When DPLL circuit samples the incoming data, the counter is reset to '0' and the clock is brought low. The counter then begins its counting sequence again. Note that the 2x clock high time may vary depending upon where the DPLL sampling actually occurs (i.e. EC-1, EC or EC+1). Nominally, the 2x clock should have a high time and low time of 4 oscillator clock cycles (assuming 16x Clock speed). Figure 2 shows examples of the 2x clock being adjusted for synchronization with the incoming Manchester data. The high time is reduced to 3 oscillator clock periods when sampling occurs at EC-1 ②. It is increased to 5 oscillator clock periods, when sampling occurs at EC+1 ④, and remains at 4 oscillator clock periods when sampling actually occurs at EC ⑥. This counting and reset sequence is continuously repeated, thereby ensuring that the clock is synchronized with the Manchester data at all times.

The clock synchronizer circuit may also be tested in the same manner as the DPLL circuit.



SPEED COUNT	MID COUNT	END COUNT
16x	4	8
32x	8	16

FIGURE 2. DECODER SAMPLING TIMING DIAGRAM

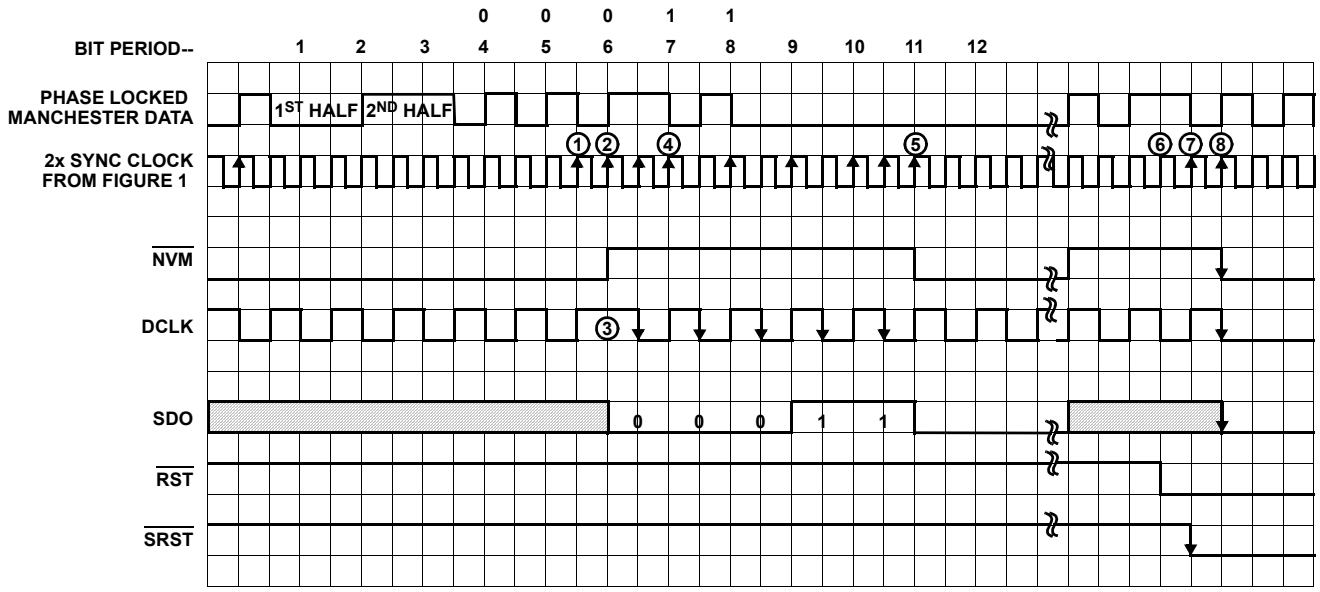


FIGURE 3. DECODER TIMING DIAGRAM

Sync Pulse Decoder and Sync Recognition Circuits

The Sync Pulse Decoder and Sync Recognition circuits consist of a 10-stage shift register which is clocked by the 2x synchronous clock from the clock synchronizer circuit. It is continuously monitoring the phase locked Manchester data for a valid 5 bit wide pattern (i.e. a 3 bit sync pulse followed by a 2 valid Manchester bits). Since the sync pulse consists of 1½ bit periods in '1' or '0' state followed by 1½ bit periods in the opposite state, and valid Manchester data contains mid-bit transitions, there are 10 specific states which must be recognized in order to initiate synchronization. When these 10 states are recognized, a synchronization signal is sent to the phase shifter and Manchester decoder circuits.

This portion of the circuit may be tested by using the HD-6409 for a standard decoding operation while ensuring there is invalid data present both before and after the valid synchronization sequence and Manchester data. The $\overline{NVM}$ line should toggle to indicate the presence of the invalid data (refer to Figure 3).

Phase Shifter

The Phase Shifter Circuit adjusts the phase of the DCLK output upon the receipt of a synchronization signal from the sync recognition circuit. The phase adjustment is necessary in order to ensure that the serial data output from the decoder will be phase matched with the DCLK so that the falling edges of DCLK may be used to latch the data from SDO.

The phase shifter may be tested by phase adjusting the input Manchester data with respect to the DCLK output signal. The DCLK signal should always go high coincident with the $\overline{NVM}$ recognition of a valid data sequence, or should remain high at this point and become 180° phase shifted. The following DCLK falling edge may then be used for latching the first serial data bit at SDO (refer to Figure 3).

Manchester Decoder

The Manchester Decoder circuit provides the decoded Manchester data as serial NRZ data on the SDO output. This data is provided coincident with the rising edge of DCLK so that the next DCLK falling edge may be used to latch the serial data to the external device.

The Manchester decoder will be fully exercised during a standard decoder operation.

Decoder Timing Diagram

Figure 3 further illustrates the relationships between the various decoder input and output signals. The phase locked Manchester data is shifted into the 10-stage shift register of the sync recognition circuit on every rising edge of the 2x synchronous clock (Note that the 2x clock signal is provided by the DPLL circuit and is continuously being adjusted to match the incoming data). Bit periods 1-5 provide the sync pulse and 2 valid Manchester bits. This data is shifted into sync recognition position at clock edge ①.

The $\overline{NVM}$ output will go high at the following clock edge ②, indicating valid data is being received. At this point, DCLK is also latched high regardless of its previous state (note that DCLK may change phase by 180° ③).

The first valid data bit will also be provided at the SDO (serial data out) at this clock edge ②.

Serial data will continue to be supplied to the SDO output at every other rising edge of the 2x synchronous clock ④. When invalid Manchester data is detected, the $\overline{NVM}$ line will go low three synchronous clock periods after the invalid data is received.

At any time during a decoding operation, a low on $\overline{RST}$ input ⑥ will force SRST (Serial Reset) low one clock cycle later ⑦. It will also force DCLK, $\overline{NVM}$ and SDO low two synchronous clock cycles later ⑧.

Encoder Section

Divide-By-X

The Divide-By-X circuit simply takes the incoming oscillator clock and reduces it to free running clock signals of 1 and 2 times the data rate. These clock signals are used by the encoder only.

Output Select Logic:

The Output Select Logic controls the data that is supplied to the remainder of the Encoder circuit. Depending upon the mode select, either the NRZ data is provided to the encoder, or the Phase-Lock Manchester data is provided to the Encoder circuit for output on the $\overline{BOO}$, $\overline{BZO}$ lines. The output select logic also controls which internal clock signal will drive the ECLK output. The 2x synchronous clock from the clock synchronizer circuit is used for the repeater mode, and the 1x free running clock is used for the encoder mode.

Zeros Counter

The Zeros Counter circuit, upon initiation of a count enable signal, begins counting the series of Manchester zeros being supplied by the encoder on the $\overline{BOO}$, $\overline{BZO}$ lines. The counting sequence is initiated by the assertion of the $\overline{CTS}$ (Clear To Send) line. When the Zeros Counter reaches a count of eight (8), a sync enable signal will be issued to the Sync Generator circuit. The Zeros Counter is driven by the 1x free running clock.

Sync Generator

The Sync Generator provides the sync pulse on the $\overline{BOO}$ and $\overline{BZO}$ outputs immediately following the eight Manchester zeros sequence. The Sync Generator will initiate the sync pulse when it receives a sync enable signal from the Zeros Counter.

Manchester Encoder

The Manchester Encoder circuit makes use of the 2x free running clock and the NRZ serial data. It provides the Manchester equivalent data sequence of the NRZ data stream being latched into the SD/CDS pins. This circuit will also provide the phase-lock Manchester data from the DPLL circuit synchronous with the ECLK signal if operating in the repeater mode.

Encoder Input to Output Timing Diagram

Figure 4 illustrates the operation of the HD-6409 encoder section. The encoder operates with 1x and 2x free running clock signals taken from the 16x or 32x oscillator clock from the Divide-by-X circuit. The encoder outputs $\overline{BOO}$ and $\overline{BZO}$ will both remain high and ECLK will remain low while $\overline{CTS}$ is not asserted. The encoder cycle begins when the $\overline{CTS}$ control line is toggled to a '0' state. The next falling edge of the 1x clock ① latches the $\overline{CTS}$ signal. The next rising edge of the 2x clock ② outputs the following:

$\overline{BZO} = \overline{1xCLK}$

$\overline{BOO} = 1xCLK$

The $\overline{BOO}$ and $\overline{BZO}$ output will continue to supply the 1x clock until the zeros counter reaches a count of eight (8). The Zeros Counter begins counting on falling edge ③ of the 1x clock and continues counting on all following falling edges of the 1x clock until the sync enable count is reached at ④. The following rising edge of the 2x clock ⑤ begins counting in the Sync Generator circuit and provides the sync pulse on the $\overline{BOO}$ and $\overline{BZO}$ outputs. When the Zeros Counter reaches a count of eleven ⑥, the sync enable signal becomes inactive, the Sync Generator is disabled, and NRZ data is allowed to be gated through to the encoder circuit.

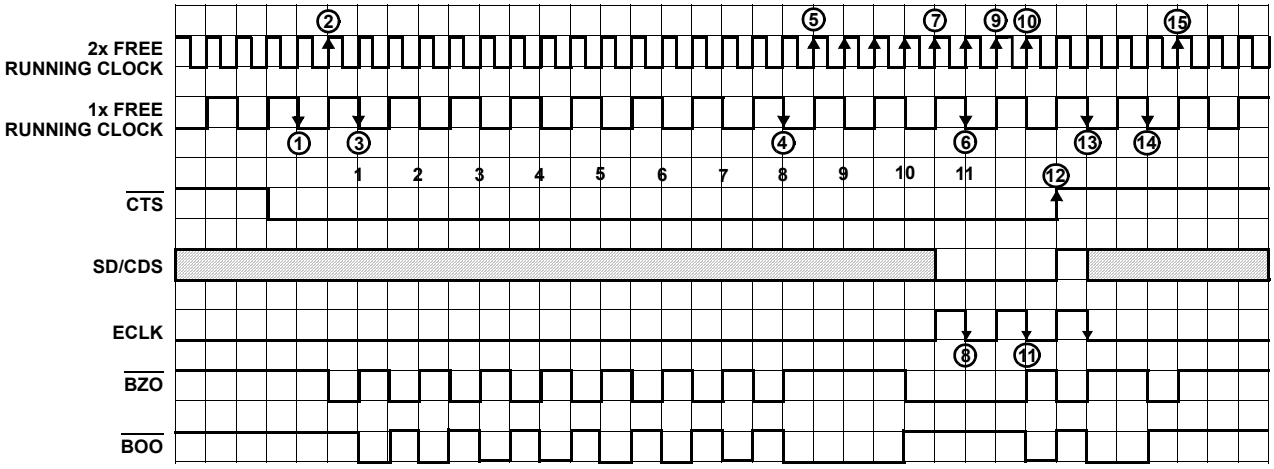


FIGURE 4. ENCODER INPUT TO OUTPUT TIMING DIAGRAM

The rising edge of the 2x clock ⑦ latches ECLK to the inverted state of the 1x clock signal. ECLK will continue being latched on every rising edge of the 2x clock for the remainder of the encoder period. The first falling edge of the ECLK ⑧ latches the incoming NRZ data. The next rising edge of the 2x clock ⑨ latched the following:

$\overline{BOO}$ = $\overline{NRZ}$ Data

$\overline{BZO}$ = NRZ Data

The next rising 2x clock edge ⑩ forces the outputs to change state, thereby completing the Manchester data bit and the falling edge of the ECLK ⑪ latches the next NRZ data bit.

Data will continue to be encoded in this fashion until the $\overline{CTS}$ line is brought high. When $\overline{CTS}$ goes high ⑫, the next falling edge of the 1x clock forces ECLK low ⑬ and latches the last NRZ data bit. The following bit period ⑭ completes the final Manchester data bit. The next rising 2x clock edge ⑮ forces the $\overline{BOO}$ and $\overline{BZO}$ outputs to a logic ‘1’ state.

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