

### Introduction

The Intersil HSP45116/HSP45116A Numerically Controlled Oscillator/Modulator can be also used as a high speed 16-Bit Multiplier/Accumulator (CMAC). This technical briefing details the part configuration to perform such functions; it provides a functional block diagram of the interface circuit that is required, and it shows the timing diagrams of the data and control signals involved.

The features of the HSP45116/HSP45116A configured as a CMAC include:

- 25 or 33MHz Output Rate of the Complex Vector (HSP45116)
- 52MHz Output Rate of the Complex Vector (HSP45116A)
- 16-Bit Complex Inputs
- 20-Bit Complex Output
- 32-Bit Internal Accumulator
- Two's Complement or Offset Binary (Unsigned) Outputs Available
- Peak Bit Growth in the Accumulator Available through Status Pins
- The HSP45116A additionally provides higher speed operation at 52MHz, and is available in a 160 Ld MQFP.

The HSP45116/HSP45116A combines a high performance quadrature numerically controlled oscillator and a high speed 16-bit complex multiplier/accumulator.

To utilize the HSP45116/HSP45116A as a CMAC only, a number of input pins have to be set at the logic levels as specified on the attached Pin Settings for Complex Multiplier Operation Table. These pin assignments are necessary in order to bypass the operations of the Numerically Controlled Oscillator (NCO) and advance the data directly to the CMAC portion of the device. In order to accomplish proper data alignment within the part, some external interface circuitry is required as illustrated on the functional block diagram of Figure 1.

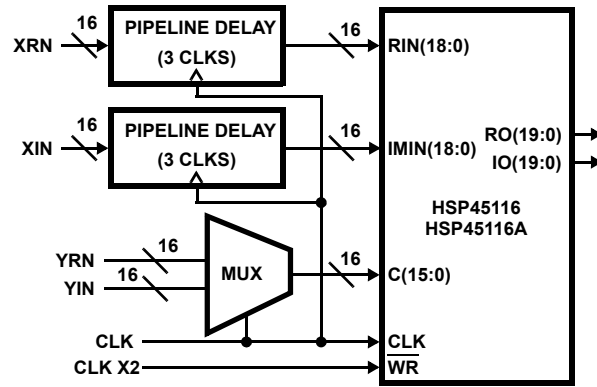
Each complex input includes a real and an imaginary component. Notice that while the first complex input vector is being clocked in the HSP45116/HSP45116A through the parallel input ports RIN(18:0) and IMIN(18:0), the second complex input vector is being clocked from a single 16-bit input port (C(15:0)), by clocking one complex component at the time. This implies that the clock of the second complex vector ( $\overline{WR}$ ) must be twice the frequency of the clock for the first complex vector (CLK).

The exact timing relationships between inputs, outputs, control signals, and clocks are shown on Figure 2. Given the timing diagram of Figure 2 and the external interface circuit as shown on Figure 1, then full data alignment can be accomplished.

Figure 3 shows an internal block diagram of the device. The block diagram illustrates the additional data path of the second complex vector being input through the C(15:0) port follows before it lines up with the first complex vector internal to the device. In addition, this second input vector C(15:0) must be transferred to the CMAC without being altered by any of the NCO HSP45116/HSP45116A functions.

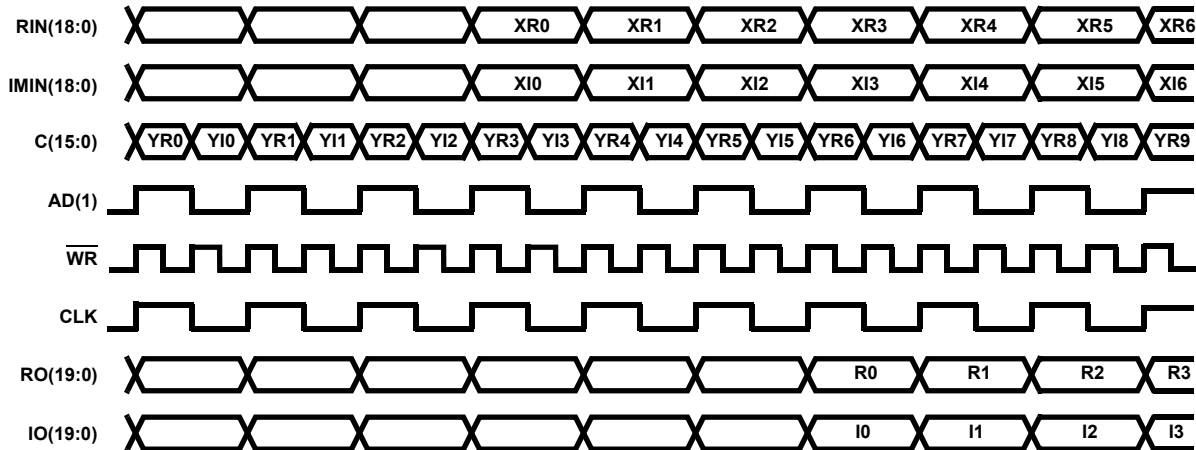
The highlighted signal path of the second complex vector C(15:0), shows the three additional registers that the data is being clocked through compared with the direct path (to the CMAC) of the first complex vector of the RIN(18:0) and IMIN(18:0) inputs. This three register delay derives the requirement for the external pipeline delays as shown on Figure 1 for the data alignment of the two complex vectors. In addition, the suggested pin configuration, on the attached pin configuration table, allows the C(15:0) data to flow unaltered by any NCO operation to the inputs of the CMAC. By following this internal data path, one can verify that the suggested logic levels assure the transparent transfer of data to the CMAC portion of the HSP45116/HSP45116A.

Note that the maximum data size of the second complex input vector is 16 bits, for each of the real and imaginary components, while the data size of the first complex input through RIN(18:0) and IMIN(18:0) can accommodate a longer length.



NOTE: Refer to Figure 2 for timing relationship between input signals, control signals and clocks.

FIGURE 1. INTERFACE BLOCK DIAGRAM UTILIZING THE HSP45116/HSP45116A AS A CMAC



NOTES:

1. Timing assumes no accumulations of the complex product. Accumulations can be accomplished by controlling the ACC input (refer to DSP Data Book).
2. XR(n)=This represents the real data of the first input vector.
3. XI(n)=This represents the imaginary data of the first input vector.
4. YR(n)=This represents the real data of the second input vector.
5. YI(n)=This represents the imaginary data of the second input vector.

FIGURE 2. TIMING DIAGRAM OF THE HSP45116/HSP45116A USED AS A CMAC

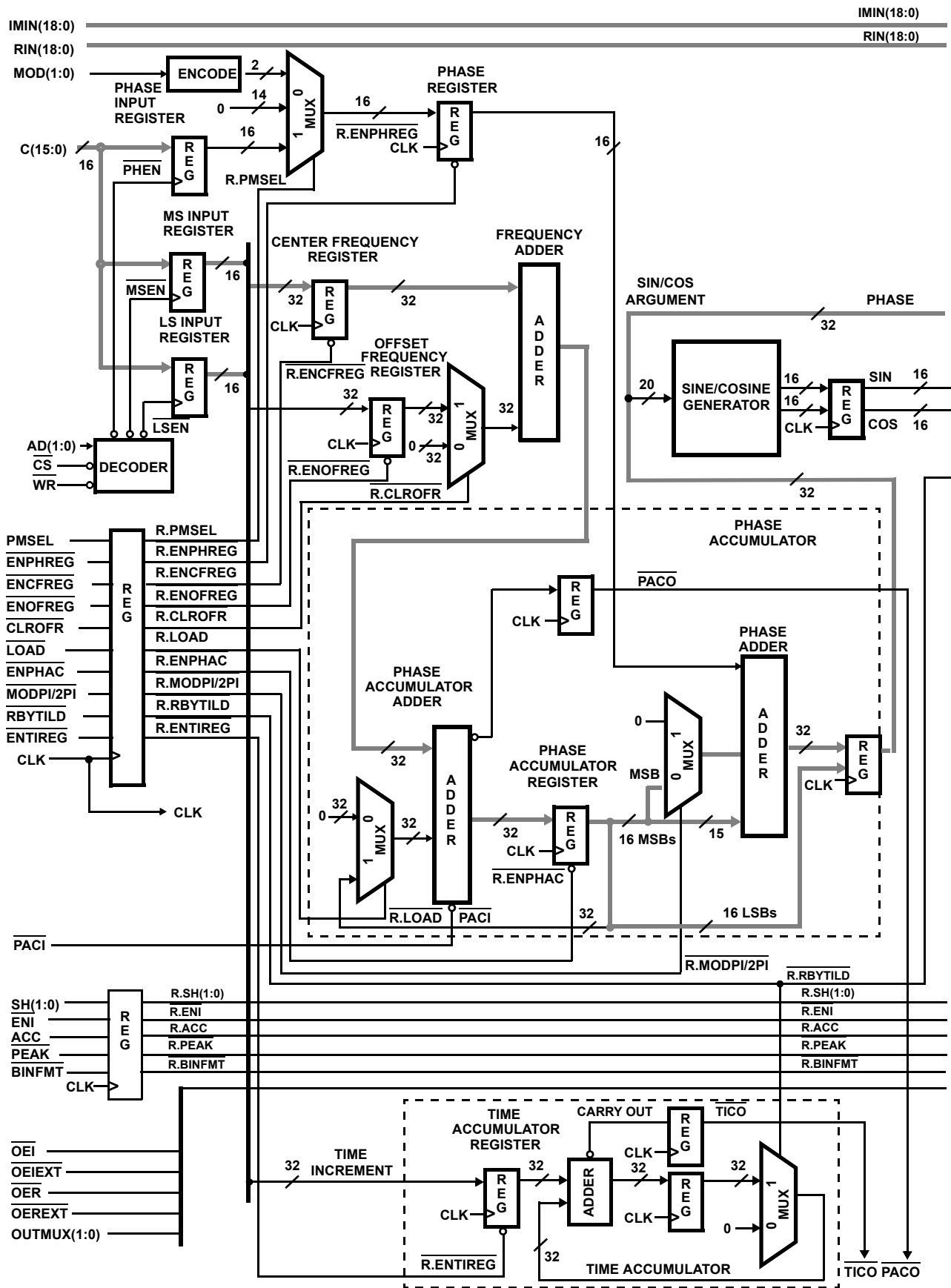


FIGURE 3. BLOCK DIAGRAM OF THE HSP45116/HSP4511A SHOWING SIGNAL PATHS WHEN USED AS A CMAC

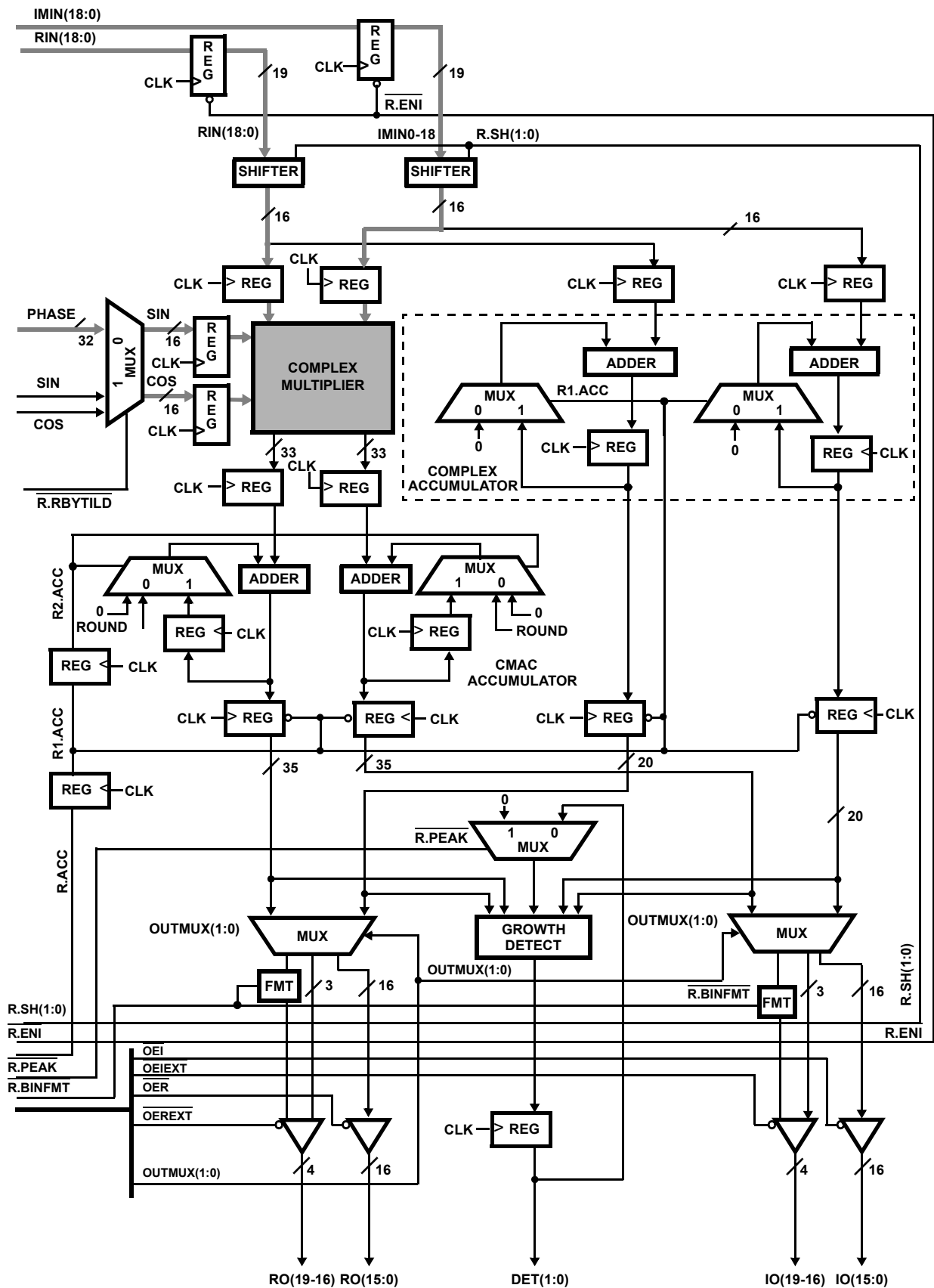


FIGURE 3. BLOCK DIAGRAM OF THE HSP45116/HSP4511A SHOWING SIGNAL PATHS WHEN USED AS A CMAC (Continued)

### Pin Settings for Complex Multiplier Operation

NAME	PIN NUMBER (HSP45116)	PIN NUMBER (HSP45116A)	TYPE	DESCRIPTION
V <sub>CC</sub>	A1, A9, A15, G1, J15, Q1, Q7, Q15	22, 34, 50, 87, 95, 102, 111, 124, 132, 145, 159	I	V <sub>CC</sub>
GND	A8, A14, B1, H1, H15, P15, Q2, Q8	7, 20, 32, 48, 62, 73, 83, 92, 98, 108, 114, 119, 125, 131, 143, 157	I	GND
C(15:0)	N8-11, P8-13, Q9-14	54-61, 63-70	I	Input for real and imaginary for one of the complex vectors.
AD(1:0)	N7, P7	51, 52	I	Selects to write alternatively (R) or (I) data from C(15:0).
$\overline{\text{CS}}$	P6	47	I	Chip Select.
$\overline{\text{WR}}$	Q6	53	I	Writes C(15:0) data, must be twice the clock frequency.
CLK	Q5	49	I	Clock.
$\overline{\text{ENPHREG}}$	M1	27	I	Logic "0".
$\overline{\text{ENOFREG}}$	N1	28	I	Logic "1".
$\overline{\text{ENCRFEG}}$	N5	42	I	Logic "0".
$\overline{\text{ENPHAC}}$	Q3	43	I	Logic "0".
$\overline{\text{ENTIREG}}$	P5	44	I	Logic "0".
$\overline{\text{ENI}}$	Q4	45	I	Logic "0".
$\overline{\text{MODPI/2PI}}$	N6	46	I	Logic "0".
$\overline{\text{CLROFR}}$	P4	41	I	Logic "0".
$\overline{\text{LOAD}}$	N4	38	I	Logic "0".
MOD(1:0)	M3, N3	35, 36	I	Both pins at Logic "0".
PMSEL	P3	39	I	Logic "0".
$\overline{\text{RBYTILD}}$	L3	30	I	Logic "0".
$\overline{\text{PACI}}$	P2	37	I	Logic "1".
PACO3	L13	79	O	
TICO3	P1	33	O	
RIN(18:0)	C1, C2, D1, D2, E1-3, F1-3, G2, G3, H2, H3, J1-3, K1, K2	2-19, 21, 23	I	Input for real data for one of the input vectors with the imaginary data at IMIN(18:0).
IMIN(18:0)	A2-7, B2-7, C3-8, D3	1, 138-142, 144, 146-156, 158	I	Input for imaginary data for one of the input vectors with the real data at RIN(18:0)
SH(1:0)	K3, L1	24, 25	I	Shift Control Inputs. These lines control the input shifters of the RIN and IIN inputs of the complex multiplier. The shift controls are common to the shifters on both of the busses.
ACC	L2	26	I	Accumulate/Dump Control. This input controls the complex accumulators and their holding registers. When high, the accumulators accumulate and the holding registers are disabled. When low, the feedback in the accumulators is zeroed to cause the accumulators to load. The holding registers are enabled to clock in the results of the accumulation. This input is registered by CLK.
$\overline{\text{BINFMT}}$	N2	31	I	This input is used to convert the two's complement output to offset binary (unsigned) for applications using D/A converters. When low, bits RO19 and IO19 are inverted from the internal two's complement representation. This input is registered by CLK.

**Pin Settings for Complex Multiplier Operation** (Continued)

NAME	PIN NUMBER (HSP45116)	PIN NUMBER (HSP45116A)	TYPE	DESCRIPTION
$\overline{\text{PEAK}}$	M2	29	I	This input enables the peak detect feature of the block floating point detector. When high, the maximum bit growth in the output holding registers is encoded and output on the DET(1:0) pins. When the PEAK input is asserted, the block floating point detector output will track the maximum growth in the holding registers, including the data in the holding registers at the time that PEAK is activated.
OUTMUX(1:0)	N12, N13	71, 72	I	Logic "0".
RO(19:0)	C15, D14, D15, E14, E15, F13-15, G13-15, H13, H14, J13, J14, K13-15, L15, M15	84-86, 88-91, 93-94, 96-97, 99-101, 103-107, 109	O	These three state outputs are controlled by $\overline{\text{OER}}$ and $\overline{\text{OEREXT}}$ . OUTMUX(1:0) select the data output on the bus.
IO(19:0)	A10-13, B8-15, C9-14, D13, E13	110, 112-113, 115-118, 121-123, 126-130, 133-137	O	Imaginary output data bus. These three-state outputs are controlled by $\overline{\text{OEI}}$ and $\overline{\text{OEIEXT}}$ . OUTMUX(1:0) select the data output on the bus.
DET(1:0)	N15, L14	81, 82	O	These output pins indicate the number of bits of growth in the accumulators. While PEAK is low, these pins indicate the peak growth. The detector examines bits 15-18, real and imaginary accumulator holding registers and bits 30-33 of the real and imaginary CMAC holding registers. The bits indicate the largest growth of the four registers.
$\overline{\text{OER}}$	P14	74	I	Three-state control for bits RO(15:0). Outputs are enabled when the line is low.
$\overline{\text{OEREXT}}$	M13	76	I	Three-state control for bits RO(19:16). Outputs are enabled when the line is low.
$\overline{\text{OEI}}$	M14	79	I	Three-state control for bits IO(15:0). Outputs are enabled when the line is low.
$\overline{\text{OEIEXT}}$	N14	77	I	Three-State control for bits IO(19:16). Outputs are enabled when the line is low.
$\overline{\text{RND}}$	N/A	75	I	Round enable (available on HSP45116A only). This input enables rounding of the output data precision from 9 to 20 bits (see HSP45116A Description and Operation). This input is active "low". This input must be tied either high or low.

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