

Pipeline Delay Through the HSP45116

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The following Timing Diagrams show the pipeline delays through the HSP45116 NCOM from the time that data is applied to the inputs until the outputs are affected by the

change. The delay is shown as a number of clock cycles, with no attempt made to accurately represent the setup and hold times or the clock to output delays.

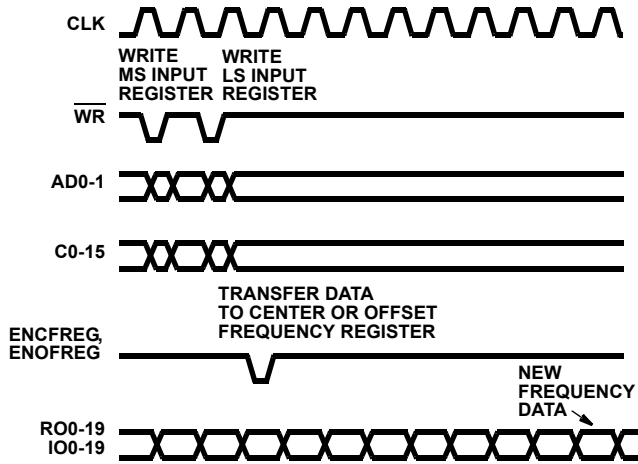


FIGURE 1. FREQUENCY TO OUTPUT DELAY

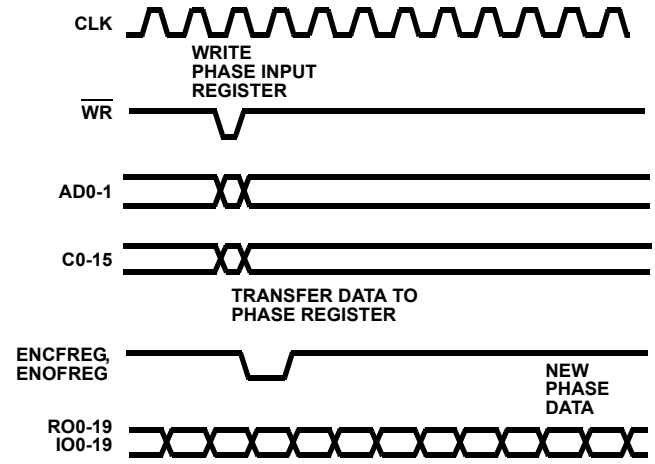


FIGURE 2. PHASE TO OUTPUT DELAY

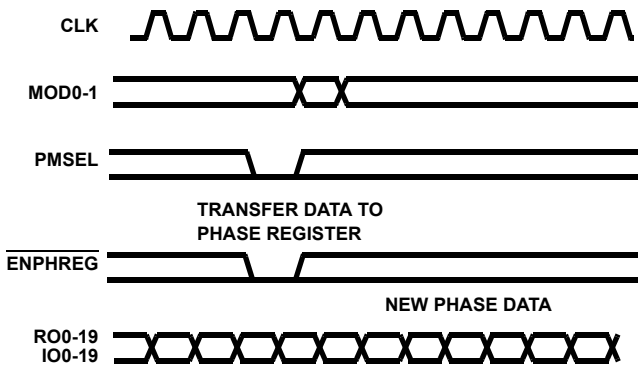


FIGURE 3. PHASE MODULATION TO OUTPUT DELAY

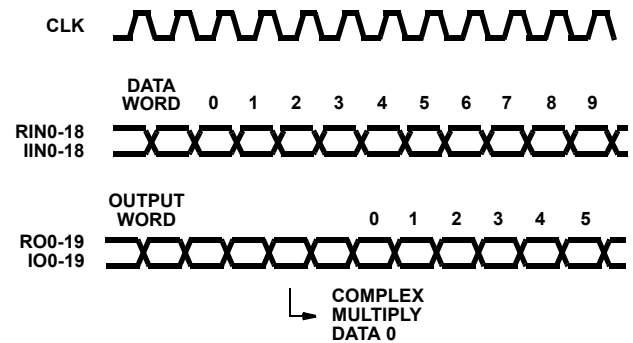


FIGURE 4. VECTOR INPUT TO OUTPUT DELAY

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