RX71M High-Speed USB

Guidelines for High-Speed USB2.0 Board Design

Introduction

This document describes the guidelines for High-Speed USB 2.0 board design.

Target Device

The application explained in this document applies to the following .

· RX71M

Note: The contents in this document are provided as a reference example based on USB specification, and the signal system quality is not guaranteed. When implementing this example into an existing system, the overall system should be thoroughly evaluated, and the user should integrate at their own discretion.

Contents

1. Introduction

This document is described by using the pin names of RX71M USB 2.0 Host/Peripheral module. Table 1 lists the outline of host/Peripheral module pin.

Table1 Outline of RX71M Host/Peripheral Module Pin

Pin Name	I/O	Function
USBA_DP USB0_DP	I/O	D+ I/O pin of the USB on-chip transceiver. This pin should be connected to the D+ pin of the USB bus.
USBA_DM USB0_DM	I/O	D- I/O pin of the USB on-chip transceiver. This pin should be connected to the D- pin of the USB bus.
USBA_VBUS USB0_VBUS	I	<Host Controller> Leave open or connect directly to Vbus of USB bus. *This pin cannot supply Vbus to the connected device. <Peripheral Controller> Connect directly to Vbus of USB bus. Can detect Vbus connection/disconnection. Connect to 5V when not connecting to Vbus.
USBA_RREF	I	Connect to AVSS_USBA via 2.2kΩ ±1% resistor
USBA_EXICEN USB0_EXICEN	O	Used for low-power consumption mode ON/OFF switch when external power supply circuit has low-consumption mode.
USBA_VBUSEN USB0_VBUSEN	O	Used for ON/OFF output to external power supply circuit.
USBA_OVRCURA USBA_OVRCURB USB0_OVRCURA USB0_OVRCURB	I	Used for input of over-current detection from external power supply circuit.
USBA_ID USB0_ID	I	When using USB Micro-AB receptacle, connect to ID pin.
VCC_USBA	I	Digital power supply for USBA.
VSS1_USBA VSS2_USBA	I	Digital ground for USBA.
AVCC_USBA	I	Analog power supply for USBA.
AVSS_USBA	I	Analog ground for USBA. Connect the PVSS_USBA pin.
PVSS_USBA	I	PLL ground for USBA. Connect the AVSS_USBA pin.
VCC_USB	I	Digital power supply for USB0.
VSS_USB	I	Digital ground for USB0.

2. USB Transmission Line

The USB transmission line indicates the wiring pattern that connects the USB connector and the RX71M embedded USB transceiver.
USB2.0 has three communication modes: High-Speed, Full-Speed and Low-Speed modes. The High-Speed mode has a 480Mbps communication speed. Therefore, the USB transmission lines must be designed as a high-frequency circuit. Impedance control is required for the USB transmission lines.
.
Notes on designing the wiring pattern of USB transmission lines are described below.

- The characteristic impedance required for the USB transmission lines is the differential impedance 90Ω ±15%.
-
- The pattern width and pattern pitch for impedance control vary depending on board thickness, material, and layer configuration. Contact the board manufacturer for more details.

- The wiring pattern length of USB transmission lines from the RX71M to the USB connector must be designed not to exceed the maximum delay time which is regulated by the USB specification. Table 2 lists the recommended values for the wiring pattern length of USB transmission lines for host and Peripheral.

Table 2 Recommended Value for the Wiring Pattern Length of USB Transmission Line

	Maximum Delay Time (USB Specification)	Wiring Length	D+ and D- Wiring Length Differential
Host Controller	3ns	300mm or less	2.5mm or less
Peripheral Controller	1ns	100mm or less	2.5mm or less

- The lower layer of the USB transmission lines must be a ground plane. The ground plane must be at least 2mm wider than the USB transmission lines. The power supply for the ground plane is GND

- Do not allocate other signal lines near the USB transmission lines. Particularly lines of heavily fluctuating signals, such as clock and data bus lines must be allocated far from the USB transmission lines. Moreover, the USB transmission lines and other lines must not cross.

- The same layer (surface layer) as the USB transmission lines should be allocated 1mm from the USB transmission lines, and grounded with a guard ring.

- USB transmission lines should be allocated on the same layer without passing through a hole. In addition, wiring should not be divaricated.

- The USB transmission lines should be wired with uniform spaces.

- The USB transmission lines should be allocated far from the oscillator, power supply circuit, and other I/O connectors.

- The USB transmission lines should be wired with straight lines. If they are bent, they should be bent gently in an arc or up to 135 degrees, and not bent at acute angles (right angles).

Figure 1 shows a design example of a Host controller USB transmission line pattern, and figure 2 shows a design example of a Peripheral controller USB transmission line pattern.

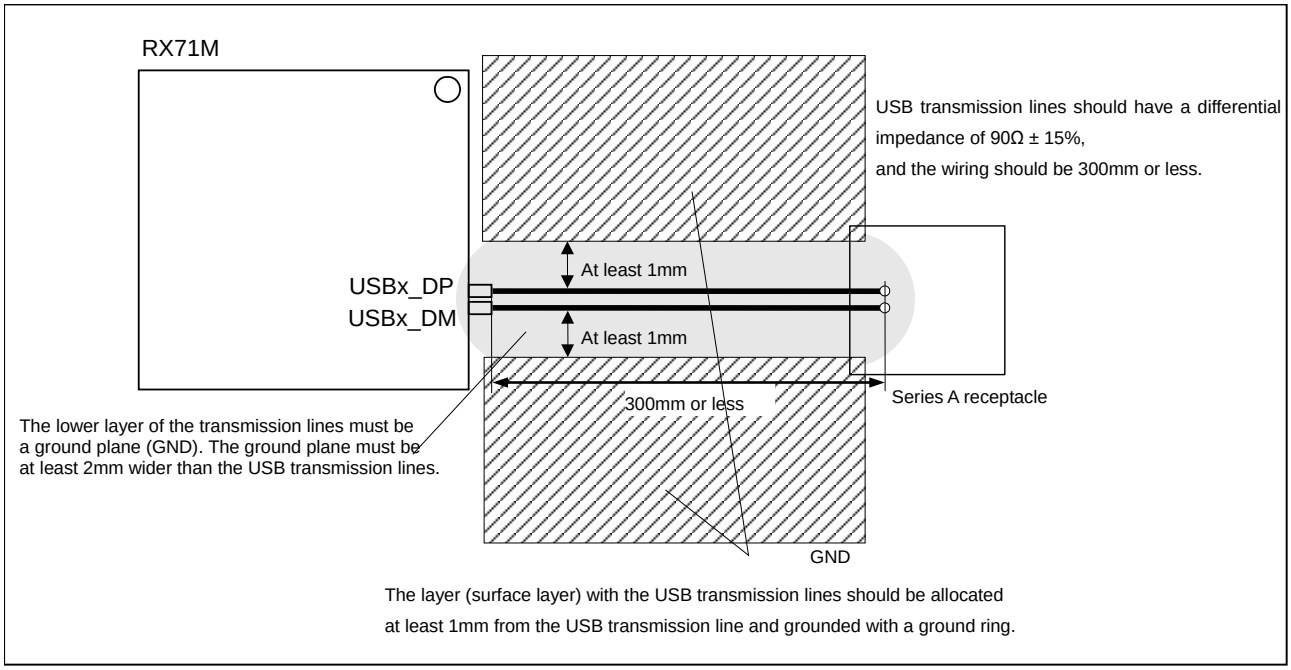

Figure 1 Design Example of a Host Controller USB Transmission Line Pattern

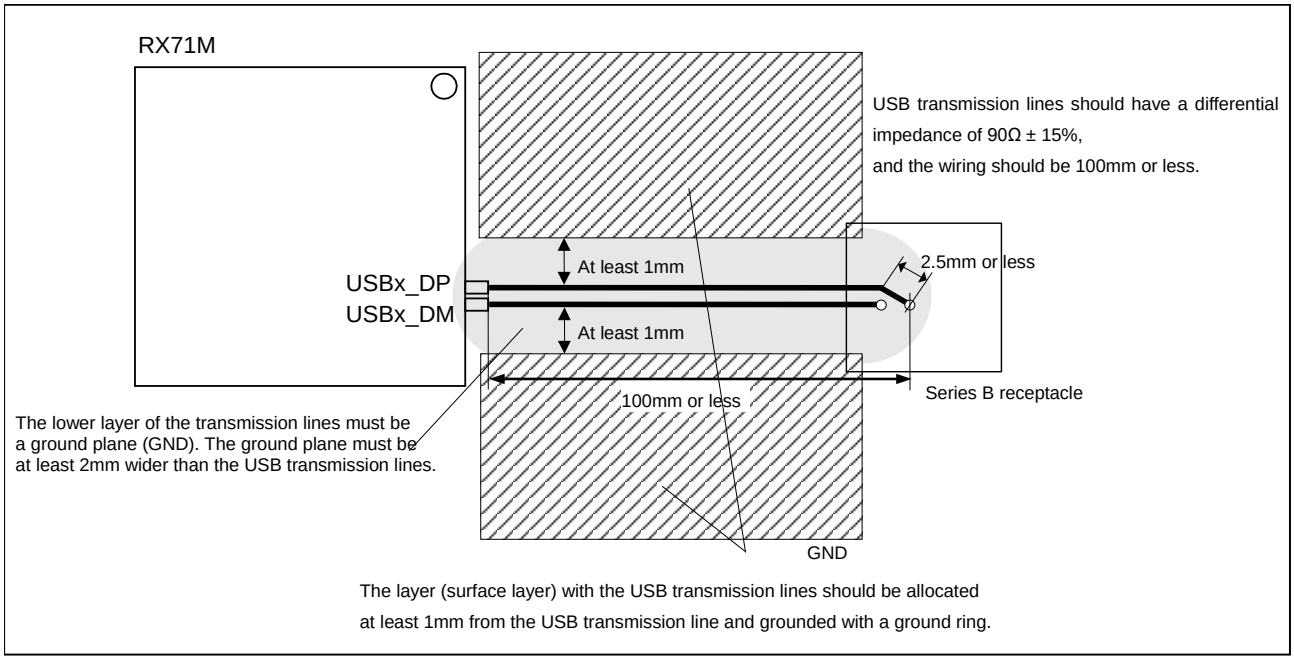

Figure 2 Design Example of a Peripheral Controller USB Transmission Line Pattern

3. USBA_RREF Line

The RX71M High-speed driver's steady-state current and PLL bias current are generated by the reference voltage determined by the external resistor between USBA_RREF and GND.

In other words, voltage fluctuation of the USBA_RREF wiring fluctuates the steady-state current and bias current, and affects the stability of the PLL and the transmission and reception waveform (jitter and amplitude of the transmission waveform).

Therefore, noise countermeasures are required.

- Place a reference resistor 2.2kΩ (resistance accuracy ±1%) between USBA_RREF and GND.
- Do not place a capacitor in parallel with the reference resistor.
- Avoid interference with other signals in the reference resistor.
- Design the parasitic resistance of the USBA_RREF wiring to 0.5Ω or less.
- Avoid interference with other signals, such as using the inner layer of the USBA_RREF wiring, in order to prevent interference with noise sources.
- Wire so that other signal wiring does not cross USBA_RREF wiring.
- Keep the USBA_RREF wiring away from other signal wiring.

4. Power Supply and Ground Pattern

(1) Analog power supply

Connect the AVCC_USBA pin to the analog power supply plane.
Keep the wiring impedance of the analog power supply as small as possible.
Separate the analog power supply from the digital power supply via the inductor and ferrite. In that case, please separate near the regulator of digital power supply. However, depending on the board, even if they are not separated, the PLL stability and transmit / receive waveform may not be affected. In the end, evaluation is made as a board, and if there is no problem with the result, there is no problem in removing the inductor and ferrite.
Place a decoupling capacitor between each power supply and GND to suppress voltage fluctuations.
Place the ceramic capacitor 10000pF near the chip.
Wire so that no other signal wiring crosses the analog power plane.
Keep the analog power supply plane away from other signal wiring.

(2) Digital power supply

Connect the VCC_USBA terminal to the digital power supply plane.
Make the wiring impedance of the digital power supply as small as possible.
Place a decoupling capacitor between each power supply and GND to suppress voltage fluctuations.
Place the ceramic capacitor 10000pF near the chip. There is no problem even if the electrolytic capacitor 47uF is separated from the chip.

(3) GND

Connect the VSS1_USBA / VSS2_USBA / PVSS_USBA / AVSS_USBA pin to the USB GND plane.
Make the GND wiring impedance as small as possible. Make sure that no other signal wiring crosses the USB GND plane. Keep the USB GND plane away from other signal wiring.

5. Connection example

The connection example is shown below.

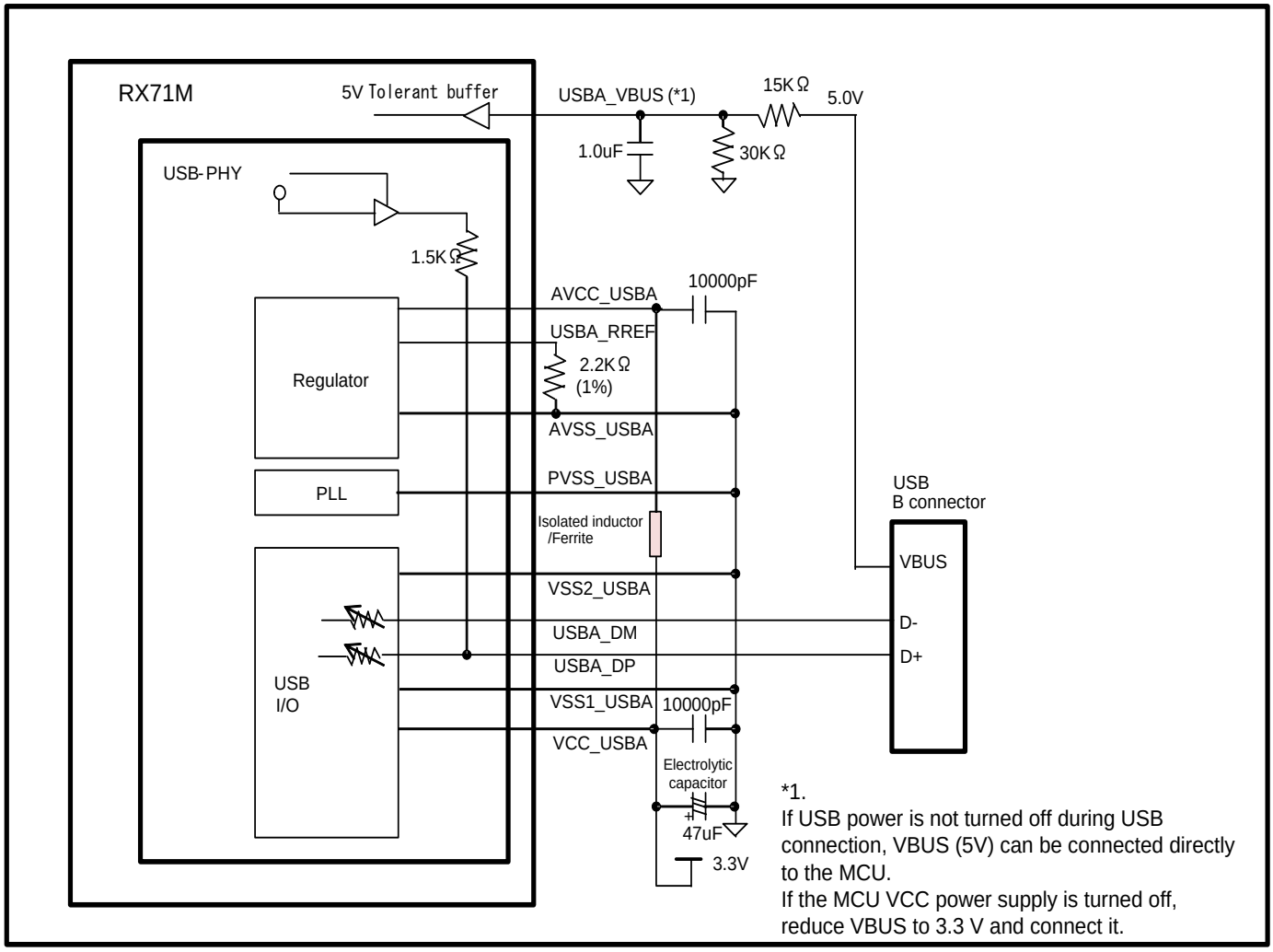

Figure 3 Self-powered function connection example

6. VBUS Power Supply Circuit

Notes on designing the VBUS power supply circuit are described below.

- When the RX71M is used as a Host controller, the additional capacity of the VBUS line should be designed to be 120uF or more.

- When the RX71M is used as a Peripheral controller, the additional capacity of the VBUS line should be designed to be within 1.0uF to 10uF.

- The VBUS line should include a filter circuit as an overshoot may be caused by inconsistent impedance when the USB cable is connected. The 1.0uF capacitor and 100Ω to 1kΩ resistor should be added as a filter circuit. The constant should be defined after confirming that an overshoot has not occurred on the board. Also, a resistor of more than 1kΩ should not be added.

- When the RX71M is used as a Host controller, the VBUS power should be supplied to the Peripheral devices. A power supply switch IC with over-current protection for the USB power bus (hereinafter called “USB power supply switch IC”) is recommended for the VBUS power supply control. Make sure to consider the limitation value of the current of VBUS power supply line based on the current value used by the system power supply applied and the USB Peripheral devices communicated. In addition, refer to the USB power supply switch IC datasheet used for VBUS power supply control circuit.

Figure 4 shows an example of the VBUS power supply circuit when it is used as a Host controller and Figure 5 shows an example of the VBUS power supply circuit when it is used as a Peripheral controller.

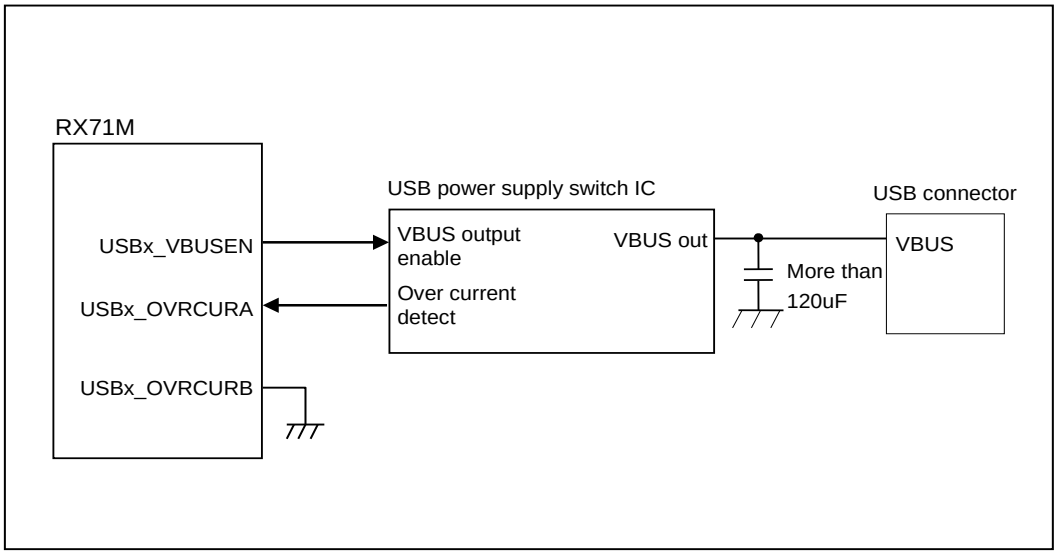

Figure 4 Example of Host Controller VBUS Power Supply Circuit

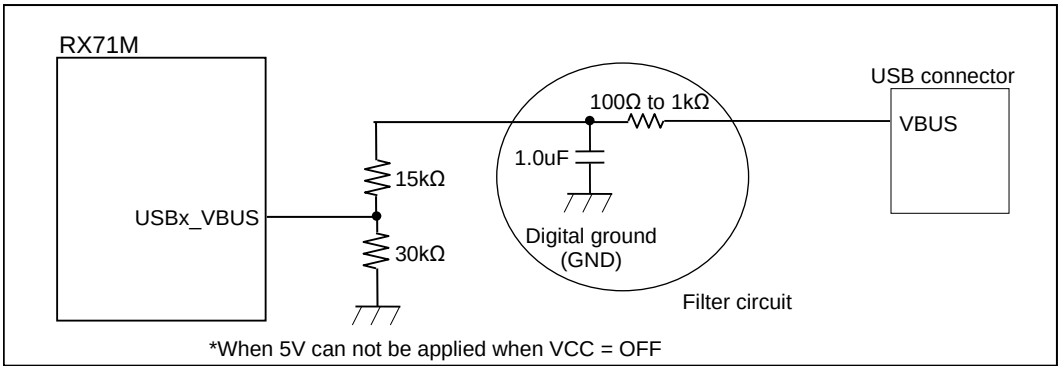

Figure 5 Example of Peripheral Controller VBUS Power Supply Circuit

7. EMI/ESD Workarounds

Notes on EMI/ESD workarounds are described below.

- When components for EMI/ESD workarounds such as coils and diodes are mounted on the USB transmission lines, they should be allocated near the USB transmission lines and the wiring should be as short as possible.

- The components for the EMI/ESD workarounds must be USB2.0 compliant. Also, by mounting EMI/ESD workaround components, an inconsistent impedance may occur on the USB transmission lines, and the waveform may become distorted. Components for use should be selected after thorough evaluation.

Figure 6 shows the block diagram of a connection example when the components for EMI/ESD workarounds are used.

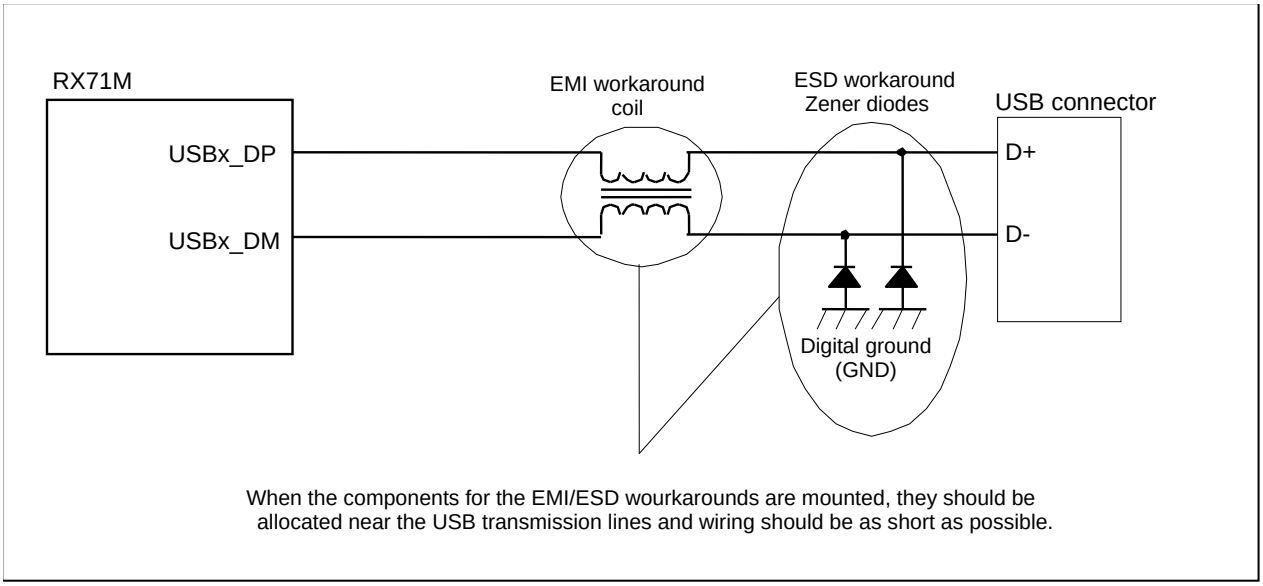

Figure 6 Connection Example When Components for EMI/ESD Workarounds are Used

Renesas Electronics Website
http://www.renesas.com/

Inquiries
http://www.renesas.com/contact

Revision History

Rev.	Date	Description	
		Page	Summary
1.0	July. 16. 19	-	First edition issued

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)

   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on

   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state

   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins

   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals

   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin

   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses

   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products

   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

Notice

1. Descriptions of circuits, software and other related information in this document are provided only to illustrate the operation of semiconductor products and application examples. You are fully responsible for the incorporation or any other use of the circuits, software, and information in the design of your product or system. Renesas Electronics disclaims any and all liability for any losses and damages incurred by you or third parties arising from the use of these circuits, software, or information.
2. Renesas Electronics hereby expressly disclaims any warranties against and liability for infringement or any other claims involving patents, copyrights, or other intellectual property rights of third parties, by or arising from the use of Renesas Electronics products or technical information described in this document, including but not limited to, the product data, drawings, charts, programs, algorithms, and application examples.
3. No license, express, implied or otherwise, is granted hereby under any patents, copyrights or other intellectual property rights of Renesas Electronics or others.
4. You shall not alter, modify, copy, or reverse engineer any Renesas Electronics product, whether in whole or in part. Renesas Electronics disclaims any and all liability for any losses or damages incurred by you or third parties arising from such alteration, modification, copying or reverse engineering.
5. Renesas Electronics products are classified according to the following two quality grades: “Standard” and “High Quality”. The intended applications for each Renesas Electronics product depends on the product’s quality grade, as indicated below.
   "Standard": Computers; office equipment; communications equipment; test and measurement equipment; audio and visual equipment; home electronic appliances; machine tools; personal electronic equipment; industrial robots; etc.
   "High Quality": Transportation equipment (automobiles, trains, ships, etc.); traffic control (traffic lights); large-scale communication equipment; key financial terminal systems; safety control equipment; etc.

   Unless expressly designated as a high reliability product or a product for harsh environments in a Renesas Electronics data sheet or other Renesas Electronics document, Renesas Electronics products are not intended or authorized for use in products or systems that may pose a direct threat to human life or bodily injury (artificial life support devices or systems; surgical implantations; etc.), or may cause serious property damage (space system; undersea repeaters; nuclear power control systems; aircraft control systems; key plant systems; military equipment; etc.). Renesas Electronics disclaims any and all liability for any damages or losses incurred by you or any third parties arising from the use of any Renesas Electronics product that is inconsistent with any Renesas Electronics data sheet, user’s manual or other Renesas Electronics document.
6. When using Renesas Electronics products, refer to the latest product information (data sheets, user’s manuals, application notes, “General Notes for Handling and Using Semiconductor Devices” in the reliability handbook, etc.), and ensure that usage conditions are within the ranges specified by Renesas Electronics with respect to maximum ratings, operating power supply voltage range, heat dissipation characteristics, installation, etc. Renesas Electronics disclaims any and all liability for any malfunctions, failure or accident arising out of the use of Renesas Electronics products outside of such specified ranges.
7. Although Renesas Electronics endeavors to improve the quality and reliability of Renesas Electronics products, semiconductor products have specific characteristics, such as the occurrence of failure at a certain rate and malfunctions under certain use conditions. Unless designated as a high reliability product or a product for harsh environments in a Renesas Electronics data sheet or other Renesas Electronics document, Renesas Electronics products are not subject to radiation resistance design. You are responsible for implementing safety measures to guard against the possibility of bodily injury, injury or damage caused by fire, and/or danger to the public in the event of a failure or malfunction of Renesas Electronics products, such as safety design for hardware and software, including but not limited to redundancy, fire control and malfunction prevention, appropriate treatment for aging degradation or any other appropriate measures. Because the evaluation of microcomputer software alone is very difficult and impractical, you are responsible for evaluating the safety of the final products or systems manufactured by you.
8. Please contact a Renesas Electronics sales office for details as to environmental matters such as the environmental compatibility of each Renesas Electronics product. You are responsible for carefully and sufficiently investigating applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive, and using Renesas Electronics products in compliance with all these applicable laws and regulations. Renesas Electronics disclaims any and all liability for damages or losses occurring as a result of your noncompliance with applicable laws and regulations.
9. Renesas Electronics products and technologies shall not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable domestic or foreign laws or regulations. You shall comply with any applicable export control laws and regulations promulgated and administered by the governments of any countries asserting jurisdiction over the parties or transactions.
10. It is the responsibility of the buyer or distributor of Renesas Electronics products, or any other party who distributes, disposes of, or otherwise sells or transfers the product to a third party, to notify such third party in advance of the contents and conditions set forth in this document.
11. This document shall not be reprinted, reproduced or duplicated in any form, in whole or in part, without prior written consent of Renesas Electronics.
12. Please contact a Renesas Electronics sales office if you have any questions regarding the information contained in this document or Renesas Electronics products.

(Note1) “Renesas Electronics” as used in this document means Renesas Electronics Corporation and also includes its directly or indirectly controlled subsidiaries.
(Note2) “Renesas Electronics product(s)” means any product developed or manufactured by or for Renesas Electronics.

(Rev.4.0-1 November 2017)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.

Contact information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit:
www.renesas.com/contact/.