

## R8C/LAxA Group

### Input port characteristics

Page

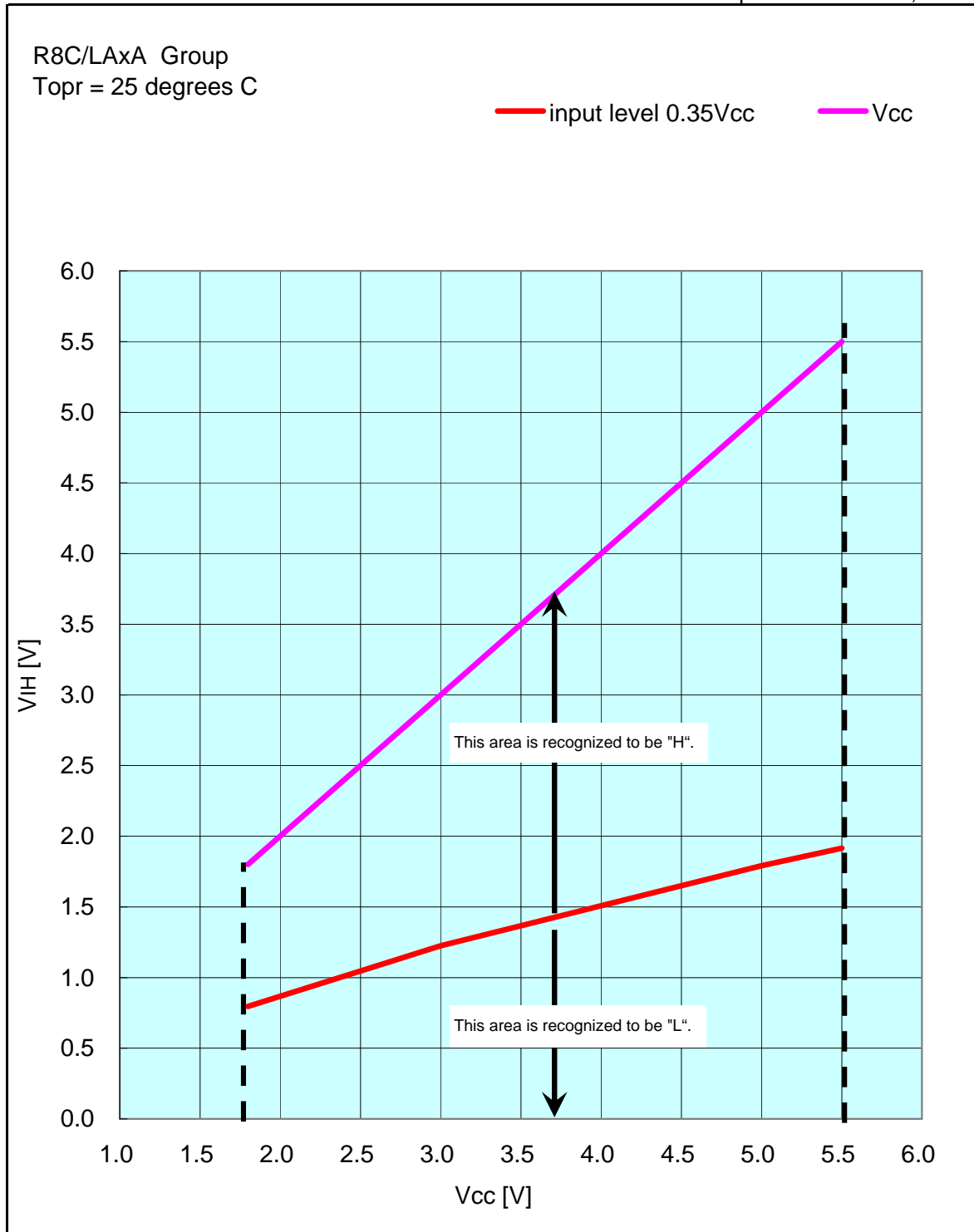
Prepared on May 12, 2011

- 1 [Input level 0.35VCC VIH/VIL VS Vcc\(P0-P9\)](#)
- 2 [Input level 0.5VCC VIH/VIL VS Vcc\(P0-P9\)](#)
- 3 [Input level 0.7VCC VIH/VIL VS Vcc\(P0-P9\)](#)
- 4 [VIH/VIL VS Vcc\(Hysteresis characteristic\)](#)
- 5 [VIH/VIL VS Vcc\(Hysteresis characteristic\)\(RESET,WKUP0\)](#)

# Input level 0.35Vcc\_VIH/VIL VS Vcc

(P0-P9)

Prepared on Nov. 30, 2010

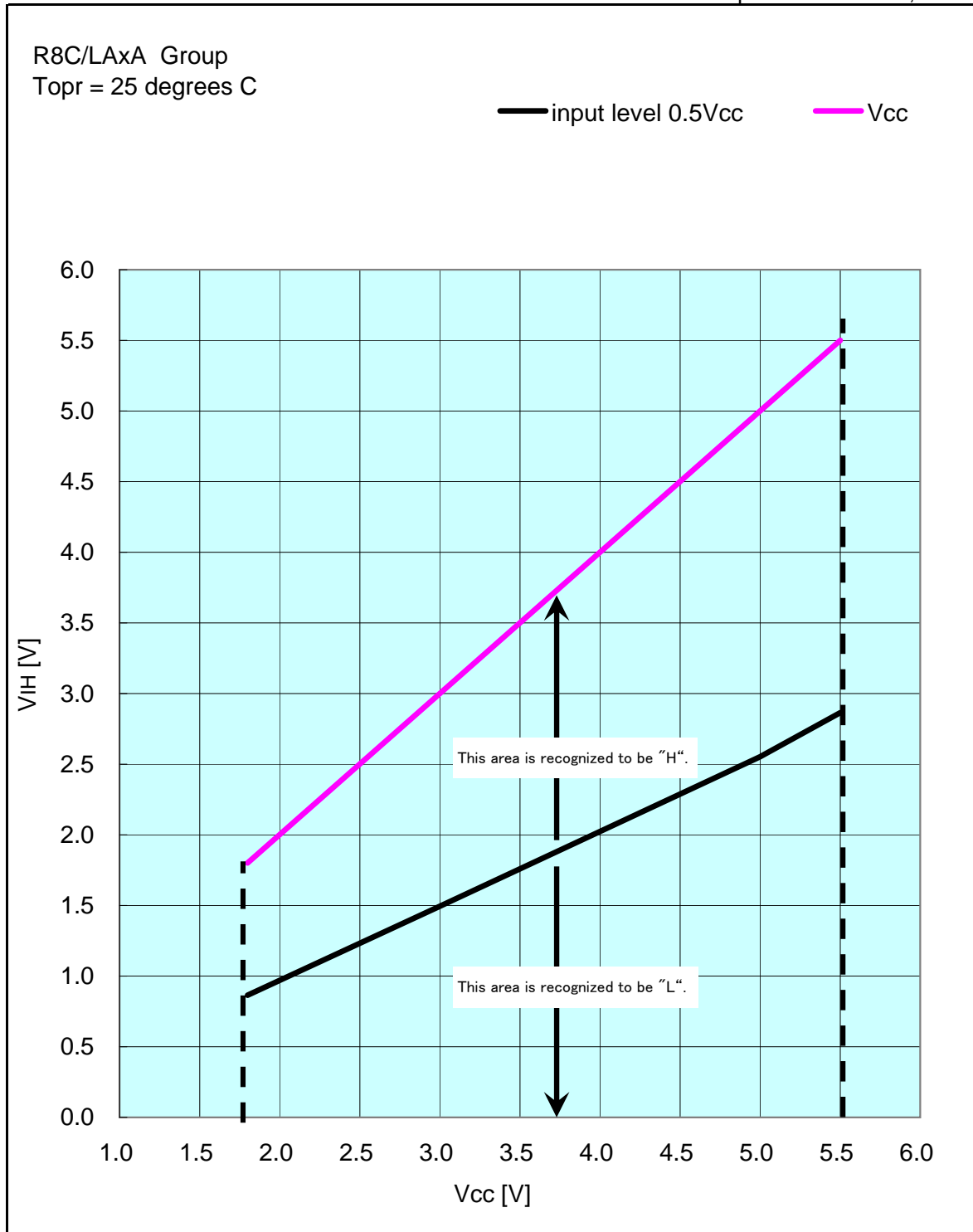


The mentioned value is only for your reference. The value is for the arbitrary samples and does not guarantee the product's characteristics

# Input level $0.5V_{cc}$ $V_{IH}/V_{IL}$ VS $V_{cc}$

(P0-P9)

Prepared on Nov. 30, 2010

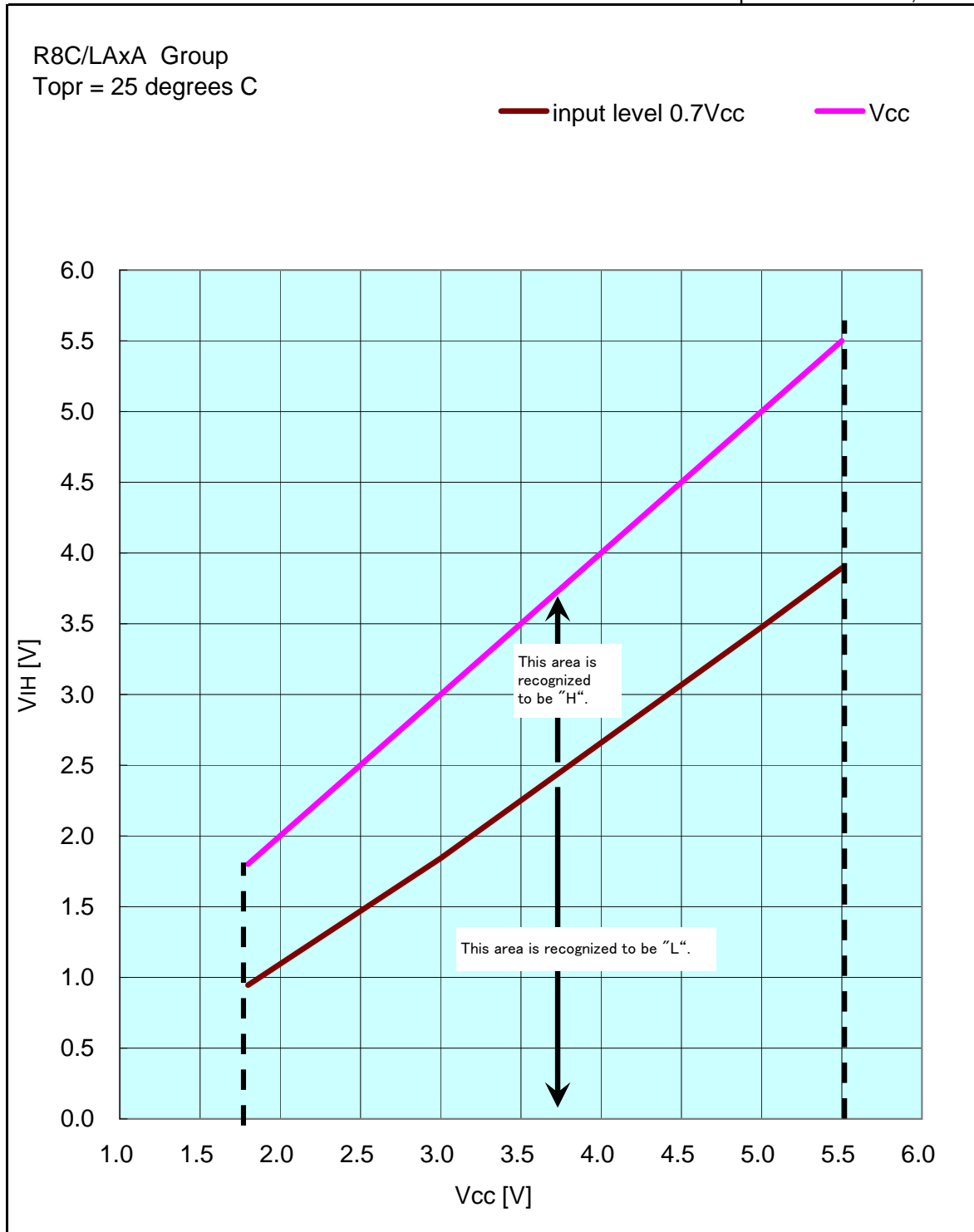


The mentioned value is only for your reference. The value is for the arbitrary samples and does not guarantee the product's characteristics

# Input level $0.7V_{cc}$ $V_{IH}/V_{IL}$ VS $V_{cc}$

(P0-P9)

Prepared on Nov. 30, 2010

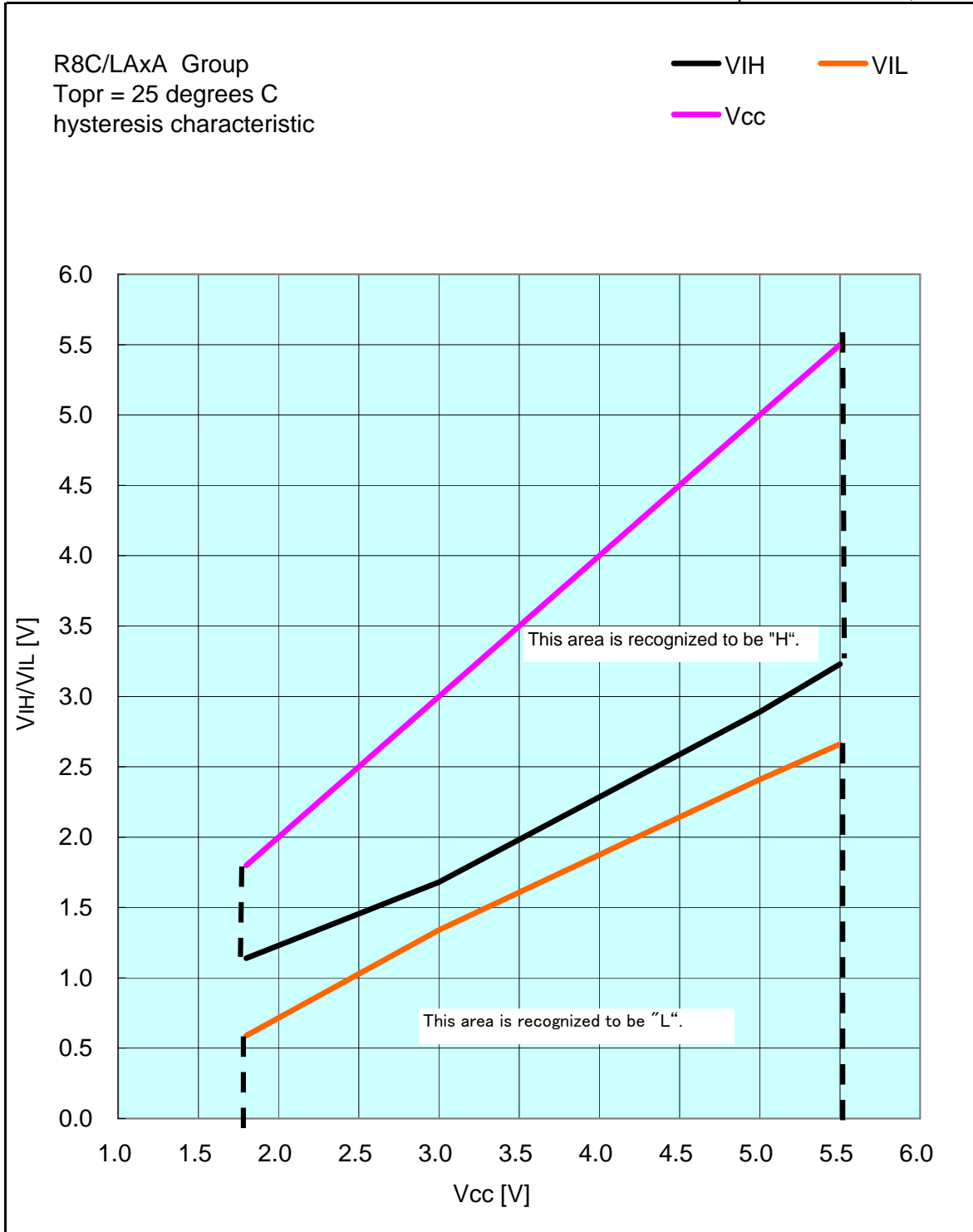


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# V<sub>IH</sub>/V<sub>IL</sub> VS V<sub>CC</sub>

INT0, INT1, INT2, INT3, INT4, INT5, INT6, INT7, KI0, KI1, KI2, KI3, KI4, KI5, KI6, KI7, TRCIOA, TRCIOB, TRCIOC, TRCIOD, TRJ0IO, TRJ1IO, TRJ2IO, TRCTRG, TRCCLK, ADTRG, RXD0, RXD2, CLK0, CLK2, SSI, SCL, SDA, SSO

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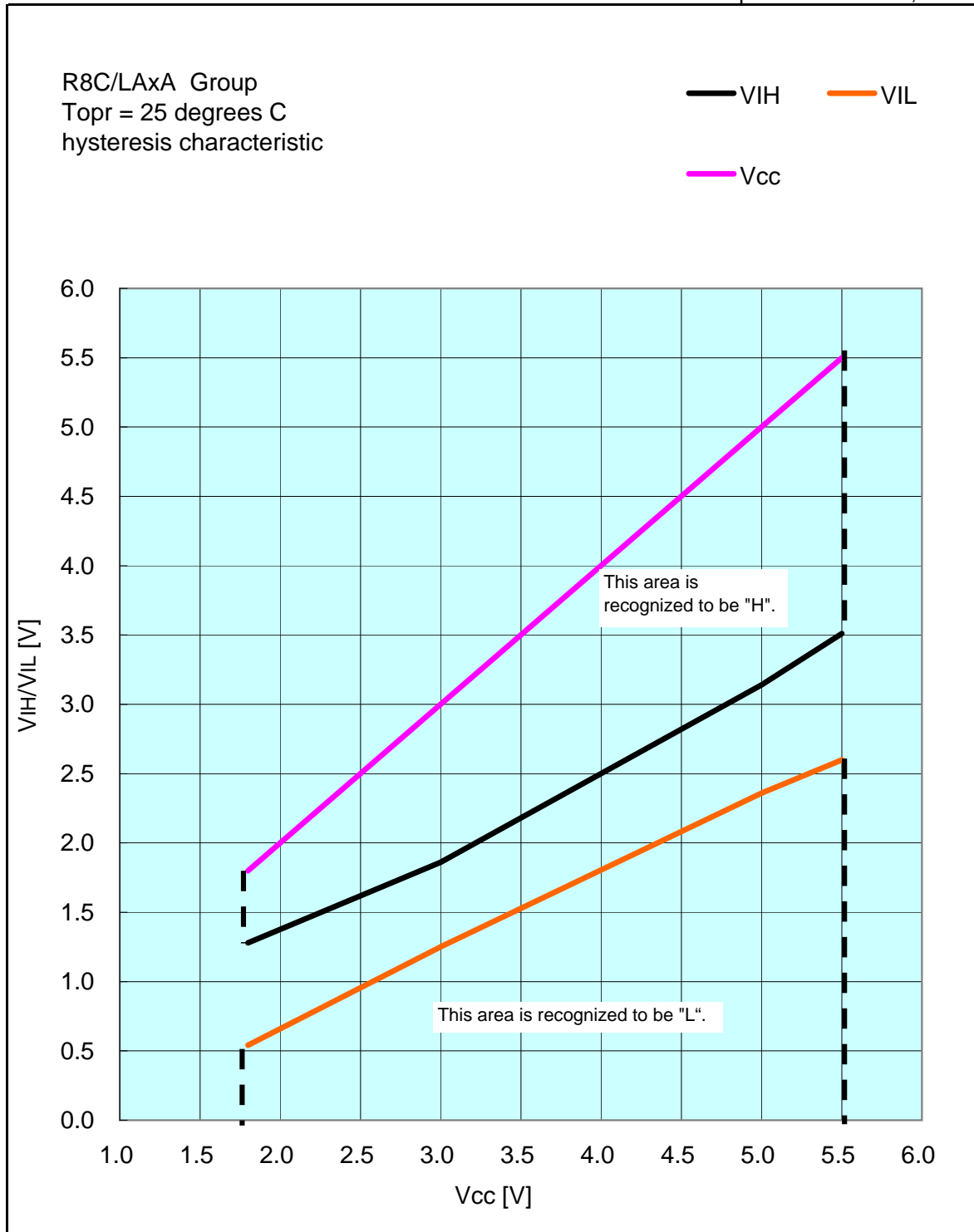


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# VIH/VIL VS Vcc

RESET, WKUP0

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