QSpan II™ Design Notes

8091862_DN001_03

October 2009

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Revision History

8091862_DN001_03, October 2009

This version of the document was rebranded as IDT. It does not include any technical changes.

8091862_DN001_02, July 2000

Revised lines 8 and 12 of Table 2.

8091862_DN001_01, July 2000

Document Creation.

Design Notes

This document identifies some important design differences for the QSpan II (CA91L862A) device and the QSpan (CA91C860B, CA91L860B) device.

Redefinition of VIO to VH pin

The QSpan (CA91L860B-xxCE) and QSpan IIZ/Z1 (CA91L862A-xxCEZx) define pin R3 as VIO. Pin R3 has been redefined in the QSpan II (CA91L862A-xxCE) as VH. This change may impact some board designs. The QSpan II (CA91L862A-xxCE) is the production device.

The QSpan/QSpan IIZ/QSpan IIZ1 defines VIO as an input pin. The VIO pin is used to determine the PCI signalling characteristics. This implementation restricts the power up sequencing of the device. If 5V is applied to the VIO pin, then the 3.3V power ramp must occur before the 5V power to ensure the current specification for the VIO pin is not exceeded. The current may be limited to VIO through an external series resistor.

The QSpan II (CA91L862A-xxCE) defines VH (Highest I/O voltage) as a power pin. This implementation removes the restriction on power sequencing. VH must be connected to the highest voltage level that the QSpan II I/Os will observe on either the QBus or the PCI Bus (see Table 1). The QSpan II (CA91L862A-xxCE) contains Universal PCI Buffers eliminating the requirement for a VIO pin. Since the QSpan II (CA91L862A-xxCE) contains Universal PCI Buffers, the signalling characteristics of the QSpan II (CA91L862A-xxCE) operate within the PCI specification electrical requirements of both a 5V and 3.3V signalling environment.

Table 1: Voltage required to be applied to VH

PCI Bus Voltage (V)	QBus Voltage (V)	VH Voltage (V)
3.3	3.3	3.3
5	5	5
3.3	5	5
5	3.3	5
VIO*	3.3	VIO*
VIO*	5	5

*VIO denotes the signal connection to the PCI bus connector for Universal Signalling.

The transition to the QSpan II (CA91L862A-xxCE) will require you to review the current board design. This may require a change to your assembly instructions/BOM (bill of materials) (for example, the requirement to change resistor value) or worst case require a change to the PCB (or strap added). The key areas to review are:

- the value of the current limiting resistor on VIO
- the voltage that is applied to VH/VIO pin on QSpan
- the highest I/O voltage level the QSpan II (CA91L862A-xxCE) will observe

Please see Table 2 for the full details on the required actions for each possible design implementation. The yellow rows within Table 2 indicate the majority of designs that will be impacted, provided the previously defined requirements for VIO (R3 on device) were implemented.

Table 2: Implications of VIO/VH redefinition.

Current VIO Connection	PCI Bus Voltage (V)	QBus Voltage (V)	Required Action for VH Connection
Directly to 3.3V	3.3	3.3	No change required.
	3.3	5	Connect VH directly to 5V
	5	3.3	Connect VH directly to 5V
	5	5	Connect VH directly to 5V
	VIO*	3.3	Connect VH directly to VIO*
	VIO*	5	Connect VH directly to 5V
Series resistor to 3.3V	3.3	3.3	Replace with 0 ohm resistor
	3.3	5	Remove the resistor Connect VH directly to 5V
	5	3.3	Replace with 0 ohm resistor Connect VH directly to 5V
	5	5	Replace with 0 ohm resistor Connect VH directly to 5V
	VIO*	3.3	Replace with 0 ohm resistor Connect VH directly to VIO*
	VIO*	5	Remove the resistor Connect VH directly to 5V
Directly to 5V	3.3	3.3	Connect VH directly to 3.3V
	3.3	5	No change required.
	5	3.3	No change required.
	5	5	No change required.
	VIO*	3.3	Connect VH directly to VIO*
	VIO*	5	No change required.
Series resistor to 5V	3.3	3.3	Replace with 0 ohm resistor Connect VH directly to 3.3V
	3.3	5	Replace with 0 ohm resistor
	5	3.3	Replace with 0 ohm resistor
	5	5	Replace with 0 ohm resistor
	VIO*	3.3	Replace with 0 ohm resistor Connect VH directly to VIO*
	VIO*	5	Replace with 0 ohm resistor
Directly to VIO*	3.3	3.3	Connect VH directly to VIO*
	3.3	5	Connect VH directly to 5V
	5	3.3	Connect VH directly to 5V
	5	5	Connect VH directly to 5V
	VIO*	3.3	No change required.
	VIO*	5	Connect VH directly to 5V
Series resistor to VIO*	3.3	3.3	Replace with 0 ohm resistor Connect VH directly to VIO*
	3.3	5	Replace with 0 ohm resistor Connect VH directly to 5V
	5	3.3	Replace with 0 ohm resistor Connect VH directly to 5V
	5	5	Replace with 0 ohm resistor Connect VH directly to 5V
	VIO*	3.3	Replace with 0 ohm resistor
	VIO*	5	Replace with 0 ohm resistor Connect VH directly to 5V

*VIO denotes the signal connection to the PCI bus connector for Universal Signalling.

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Document: 8091862_DN001_03

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