

# **SLG4AD41757**

# **Power Sequencer**

## **General Description**

Silego SLG4AD41757 is a low power and small form device. The SoC is housed in a 2mm x 3mm STQFN package which is optimal for using with small devices.

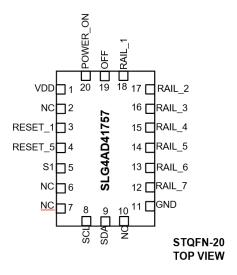
#### **Features**

- Low Power Consumption
- Pb-Free / RoHS Compliant
- Halogen-Free
- STQFN-20 Package

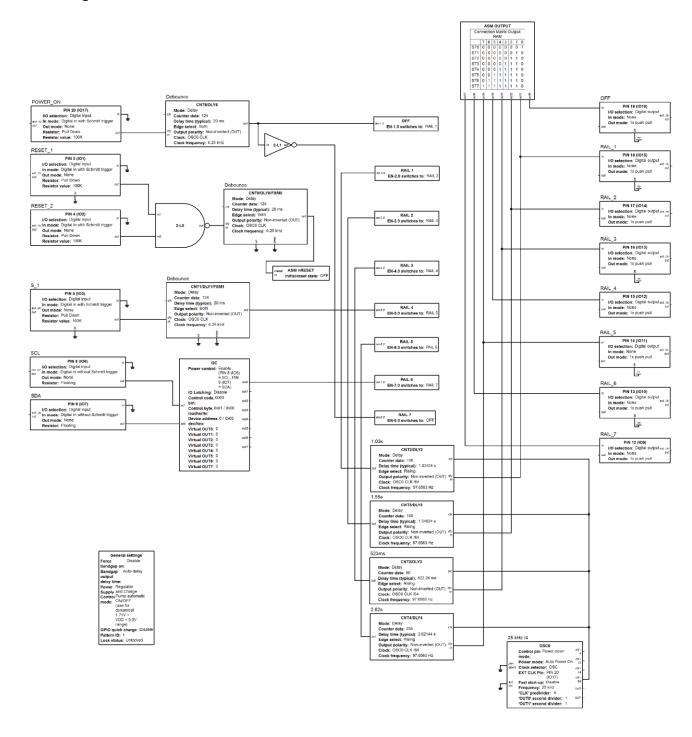
#### **Output Summary**

• 8 Outputs — Push Pull 1X

## **Pin Configuration**



## **Block Diagram**



# Pin Configuration

Pin #	Pin Name	Type	Pin Description
1	VDD	PWR	Supply Voltage
2	NC		Keep Floating or Connect to GND
3	RESET_1	Digital Input	Digital Input with Schmitt trigger
4	RESET_5	Digital Input	Digital Input with Schmitt trigger
5	S1	Digital Input	Digital Input with Schmitt trigger
6	NC		Keep Floating or Connect to GND
7	NC		Keep Floating or Connect to GND
8	SCL	Digital Input	Digital Input without Schmitt trigger
9	SDA	Digital Input	Digital Input without Schmitt trigger
10	NC		Keep Floating or Connect to GND
11	GND	GND	Ground
12	RAIL_7	Digital Output	Push Pull 1X
13	RAIL_6	Digital Output	Push Pull 1X
14	RAIL_5	Digital Output	Push Pull 1X
15	RAIL_4	Digital Output	Push Pull 1X
16	RAIL_3	Digital Output	Push Pull 1X
17	RAIL_2	Digital Output	Push Pull 1X
18	RAIL_1	Digital Output	Push Pull 1X
19	OFF	Digital Output	Push Pull 1X
20	POWER_ON	Digital Input	Digital Input with Schmitt trigger

# **Ordering Information**

Part Number	Package Type
SLG4AD41757V	V=STQFN-20
SLG4AD41757VTR	VTR=STQFN-20 – Tape and Reel (3k units)

# **Absolute Maximum Conditions**

Parameter	Min.	Max.	Unit
V <sub>HIGH</sub> to GND	-0.3	7	V
Voltage at input pins	-0.3	7	V
Current at input pin	-1.0	1.0	mA
Storage temperature range	-65	125	°C
Junction temperature		150	°C
ESD Protection (Human Body Model)	2000		V
ESD Protection (Charged Device Model)	1300		V
Moisture Sensitivity Level	1		

## **Electrical Characteristics**

(@ 25°C, unless otherwise stated)

Symbol	Parameter	Condition/Note	Min.	Тур.	Max.	Unit		
$V_{DD}$	Supply Voltage		3	5	5.5	V		
TA	Operating Temperature		-40	25	85	°C		
ΙQ	Quiescent Current	Static inputs and floating outputs		1		μA		
Vo	Maximal Voltage Appliedto any PIN in High- Impedance State				VDD	V		
lo	Maximal Average or DCCurrent (note 1)	Per Each Chip Side (PIN2-PIN10, PIN12-PIN20)			90	mA		
		Logic Input, at VDD=3.3V	1.81		VDD			
	HIOLITY ALLOW OVARAGE	Logic Input with Schmitt Trigger,at VDD=3.3V	2.14		VDD	]		
V <sub>IH</sub>	HIGH-Level Input Voltage	Logic Input, at VDD=5.0V	2.68 VI			- V		
		Logic Input with Schmitt Trigger,at VDD=5.0V	3.34		VDD			
	LOW-Level Input Voltage	Logic Input, at VDD=3.3V	0		1.31			
		Logic Input with Schmitt Trigger,at VDD=3.3V	0		0.97	_ v		
VIL		Logic Input, at VDD=5.0V	0		1.96			
		Logic Input with Schmitt Trigger,at VDD=5.0V	0		1.41			
\/	Schmitt Trigger HysteresisVoltage	Logic Input with Schmitt Triggerat VDD=3.3V	0.29	0.62	0.94	V		
V <sub>HY</sub> s		Logic Input with Schmitt Triggerat VDD=5.0V	0.44	0.90	1.38	\ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \		
Іін	HIGH-Level Input Current	Logic Input PINs; V <sub>IN</sub> = VDD	-1.0		1.0	μA		
IIL	LOW-Level Input Current	Logic Input PINs; V <sub>IN</sub> = 0V	-1.0		1.0	μA		
Van	HIGH-Level OutputVoltage	Push Pull & PMOS OD, I <sub>OH</sub> = 3mA, 1X Driver, at VDD=3.3 V	2.70	3.12		V		
Vон	, -	Push Pull & PMOS OD, IoH = 5mA, 1X Driver, at VDD=5.0 V				V		

	LOW-Level Output	Push Pull, I <sub>OL</sub> = 3mA, 1X Driver, at VDD=3.3 V		0.13	0.23	
Vol	Voltage	Push Pull, I <sub>OL</sub> = 5mA, 1X Driver, at VDD=5.0 V		0.19	0.24	V
la	HIGH-Level Output	Push Pull & PMOS OD, V <sub>OH</sub> = 2.4 V, 1X Driver, at VDD=3.3 V	6.05	12.08		mA
Іон	Current	Push Pull & PMOS OD, V <sub>OH</sub> = 2.4 V, 1X Driver, at VDD=5.0 V	22.08	34.04		IIIA
loL	LOW-Level Output	Push Pull, V <sub>OL</sub> = 0.4V, 1X Driver, at VDD=3.3 V	4.88	8.24		mA
	Current	Push Pull, VoL = 0.4V, 1X Driver, at VDD=5.0 V	7.22	11.58		
R <sub>PULL_DOWN</sub>	Internal Pull Down Resistance	Pull down on PINs 3, 4, 5, 20	87.5	109.7	136.6	kΩ
T <sub>DLY0</sub>	Delay0 Time	At temperature 25°C At temperature -40°C +85°C (note 1)	19.22 18.33	20.05	20.66 21.52	ms
T <sub>DLY1</sub>	Delay1 Time	At temperature 25°C At temperature -40°C +85°C (note 1)	19.22 18.33	20 20.05	20.66 21.52	ms
T <sub>DLY2</sub>	Delay2 Time	At temperature 25°C	996.74	1035.75	1065.92	ms
_		At temperature -40°C +85°C (note 1) At temperature 25°C	951.20 503.27	1046.93 523	1109.34 538.25	
T <sub>DLY3</sub>	Delay3 Time	At temperature -40°C +85°C (note 1) At temperature 25°C	480.28 2.53	524.12 2.62	560.20 2.071	S
T <sub>DLY4</sub>	Delay4 Time	At temperature -40°C +85°C (note 1)	2.41	2.63	2.82	ms
T <sub>DLY5</sub>	Delay5 Time	At temperature 25°C At temperature -40°C +85°C (note 1)	1.49 1.42	1.55 1.55	1.60 1.66	s
T <sub>DLY6</sub>	Delay6 Time	At temperature 25°C At temperature -40°C +85°C (note 1)	19.22 18.33	20 20.05	20.66 21.52	ms
Tsu	Start up Time	From VDD rising past PONTHR	0.526	1.4	5.148	ms
PONTHR	Power On Threshold	VDD Level Required to Start Up the Chip	0.950	1.462	1.708	V
POFF <sub>THR</sub>	Power Off Threshold	VDD Level Required to Switch Off the	0.935	1.103	1.281	V
Fscl	Clock Frequency, SCL	Chip V <sub>DD</sub> = (1.71) V			400	kHz
tLOW	Clock Pulse Width Low	V <sub>DD</sub> = (1.71) V V <sub>DD</sub> = (1.71) V	1300			ns
thigh	Clock Pulse Width High	V <sub>DD</sub> = (1.71) V	600			ns
CHIOH	Input Filter Spike	$V_{DD} = 1.8 \text{ V} \pm 5 \%$			168	110
tı	Suppression (SCL,	$V_{DD} = 3.3 \text{ V} \pm 10 \%$			157	ns
ч	SDA)	$V_{DD} = 5.0 \text{ V} \pm 10 \%$			156	1 115
taa	Clock Low to Data Out Valid	V <sub>DD</sub> = (1.71) V			900	ns
t <sub>BUF</sub>	Bus Free Time between Stop and Start	V <sub>DD</sub> = (1.71) V	1300			ns
thd_sta	Start Hold Time	V <sub>DD</sub> = (1.71) V	600			ns
tsu_sta	Start Set-up Time	V <sub>DD</sub> = (1.71) V	600			ns
thd_dat	Data Hold Time	V <sub>DD</sub> = (1.71) V	0			ns
tsu_dat	Data Set-up Time	V <sub>DD</sub> = (1.71) V	100			ns
t <sub>R</sub>	Inputs Rise Time	V <sub>DD</sub> = (1.71) V			300	ns
tϝ	Inputs Fall Time	V <sub>DD</sub> = (1.71) V			300	ns
tsu_std	Stop Set-up Time	V <sub>DD</sub> = (1.71) V	600			ns
t <sub>DH</sub>	Data Out Hold Time	V <sub>DD</sub> = (1.71) V	50			ns

		VDD = 1.8 V ± 5 %	255	 275	
tst_out_del	State Machine Output Delay				ns
ay	Time	VDD = 3.3 V ± 10 %	95	 118	
		VDD = 5.0 V ± 10 %	67	 77	
		VDD = 1.8 V ± 5 %		 165	
tst_out	State Machine Output				ns
	Transition Time	VDD = 3.3 V ± 10 %		 70	
		VDD = 5.0 V ± 10 %		 46	
		VDD = 1.8 V ± 5 %	29	 	
tst_pulse	State Machine Input Pulse				ns
-	Acceptance Time	VDD = 3.3 V ± 10 %	14	 	1
		VDD = 5.0 V ± 10 %	9.2	 	1
	State Machine Input Compete	VDD = 1.8 V ± 5 %		 29	
tst_comp	Time				ns

<sup>1.</sup> Guaranteed by Design.

# Chip address

HEX	BIN	DEC
0	0000000	0

## **Description**

#### 1. I2C Basic Command Structure

Each command to the I2C Serial Communications block begins with a Control Byte. The bits inside this Control Byte are shown in Figure 1. After the Start bit, the first four bits are a control code, which can be set by the user in reg<xx:yy>.

The Block Address is the next three bits (A10, A9, A8), which will define the most significant bits in the addressing of thedata to be read ("1") or written ("0") by the command. This Control Byte will be followed by an Acknowledge bit (ACK).

With the exception of the Current Address Read command, all commands will have the Control Byte followed by the Word Address. The Word Address, in conjunction with the three address bits in the Control Byte, will define the specific at a byte to be read or written in the command. Figure 1 shows this basic command structure.

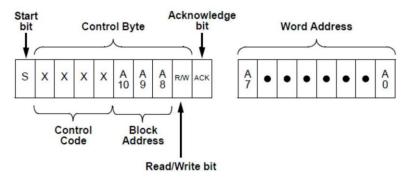


Figure 1. I2C Basic Command Structure

#### 2. I2C Serial General Timing

Shown in Figure 2 is the general timing characteristics for the I2C Serial Communications block.

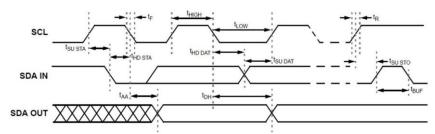


Figure 2. I2C Serial General Timing

#### 3. I2C Serial Communications: Read and Write Commands

Following the Start condition from the master, the Control Code [4 bits], the block address [3 bits] and the R/W bit (set to "0"), is placed onto the bus by the Bus Master. After the I2C Serial Communications block has provided an Acknowledgebit (ACK) the next byte transmitted by the master is the Word Address. The Block Address is the next three bits, and is the higher order addressing bits (A10, A9, A8), which when added to the Word Address will together set the internal address pointer in the SLG46533 to the correct data byte to be written. After the SLG46533 sends another Acknowledgebit, the Bus Master will transmit the data byte to be written into the addressed memory location. The SLG46533 again provides an Acknowledge bit and then the Bus Master generates a Stop condition. The internal write cycle for the data will take place at the time that the SLG46533 generates the Acknowledge bit.

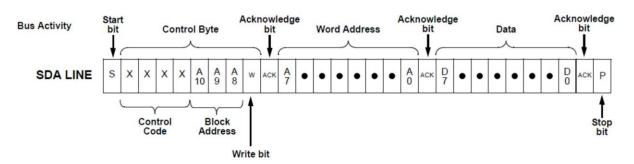


Figure 3. I2C Write Command

The Random Read command starts with a Control Byte (with R/W bit set to "0", indicating a write command) and Word Address to set the internal byte address, followed by a Start bit, and then the Control Byte for the read (exactly the sameas the Byte Write command). The Start bit in the middle of the command will halt the decoding of a Write command, but will set the internal address counter in preparation for the second half of the command. After the Start bit, the Bus Master issues a second control byte with the R/W bit set to "1", after which the SLG46533 issues an Acknowledge bit, followed by the requested eight data bits.

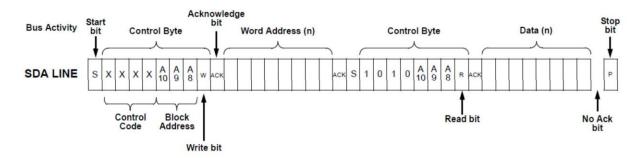


Figure 4. I2C Random Read Command

#### 4. CNT/DLY Settings

The CNT/DLY block registers can be used to change the individual delay times of the delay blocks by changing the control data and the frequency of the clock according to Equation 1. The clock frequency can also be changed by using a clock pre-divider in the OSC0 block.

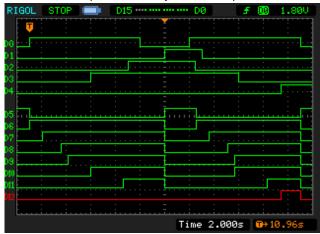
**Delay time**: [(Counter Control Data + 1 + variable) / Frequency], where 0 ≤ variable ≤ 1; Equation 1: CNT/DLY Time

Address Byte	Register Bit	Block	Function	Range
0xC0	reg<1543:1536>	DLY2	Counter data from 1 to 255 (default setting is 100)	0x01 to 0xFF
0xC1	reg<1543:1536>	DLY3	Counter data from 1 to 255 (default setting is 50)	0x01 to 0xFF
0xC2	reg<1559:1552>	DLY4	Counter data from 1 to 255 (default setting is 255)	0x01 to 0xFF
0xC3	reg<1567:1560>	CNT5	Counter data from 1 to 255 (default setting is 150)	0x01 to 0xFF

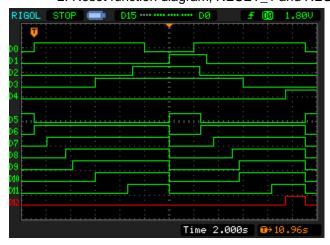
## **Functionality Waveforms**

- D0 PIN#20 (POWER\_ON)
- D1 PIN#3 (RESET\_1)
- D2 PIN#4 (RESET\_2)
- D3 PIN#5 (S1)
- D4 OUT0 internal signal, output I2C Serial Communication Block
- D5 PIN#19 (OFF)
- D6 PIN#18 (RAIL\_1)
- D7 PIN#17 (RAIL\_2)
- D8 PIN#16 (RAIL\_3)
- D9 PIN#15 (RAIL\_4)
- D10 PIN#14 (RAIL\_5)
- D11 PIN#13 (RAIL\_6)
- D12 PIN#12 (RAIL\_7)

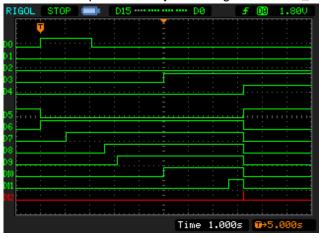
## 1. Chip functionality: Normal operation



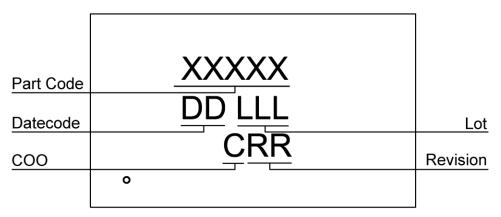
## 2. Reset function diagram, RESET\_1 and RESET\_2 are HIGH



- D0 PIN#20 (POWER\_ON)
- D1 PIN#3 (RESET\_1)
- D2 PIN#4 (RESET\_2)
- D3 PIN#5 (S1)
- D4 OUT0 internal signal, output I2C Serial Communication Block
- D5 PIN#19 (OFF)
- D6 PIN#18 (RAIL\_1)
- D7 PIN#17 (RAIL\_2)
- D8 PIN#16 (RAIL\_3)
- D9 PIN#15 (RAIL\_4)
- D10 PIN#14 (RAIL\_5)
- D11 PIN#13 (RAIL\_6)
- D12 PIN#12 (RAIL\_7)
  - 3. Chip functionality: Short signal POWER\_ON



# **Package Top Marking**



XXXXX - Part ID Field: identifies the specific device configuration

DD - Date Code Field: Coded date of manufacture

LLL - Lot Code: Designates Lot #

C - Assembly Site/COO: Specifies Assembly Site/Country of Origin

RR - Revision Code: Device Revision

Datasheet Revision	Programming Code Number	Locked Status	Part Code	Revision	Date
0.10	001	U			04/03/2017

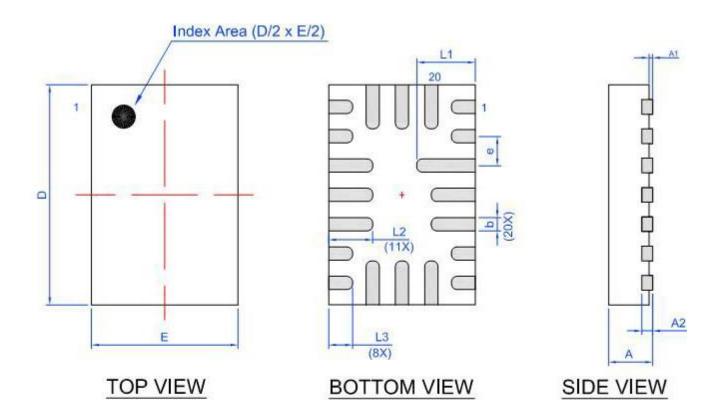
Lock coverage for this part is indicated by  $\sqrt{\ }$ , from one of the following options:

$\sqrt{}$	Unlocked
	Locked for read, bits <1535:0>
	Locked for write, bits <1535:0>
	Locked for read and write, bits <1535:0>

The IC security bit is locked/set for code security for production unless otherwise specified. Revisionnumber is not changed for bit locking.

# **Package Drawing and Dimensions**

## 20 Lead STQFN Package JEDEC MO-220, Variation WECE



Unit: mm

Symbol	Min	Nom.	Max	Symbol	Min	Nom.	Max
Α	0.50	0.55	0.60	D	2.95	3.00	3.05
A1	0.005		0.050	E	1.95	2.00	2.05
A2	0.10	0.15	0.20	L1	0.75	0.80	0.85
b	0.13	0.18	0.23	L2	0.55	0.60	0.65
е	0.40 BSC			L3	0.275	0.325	0.375

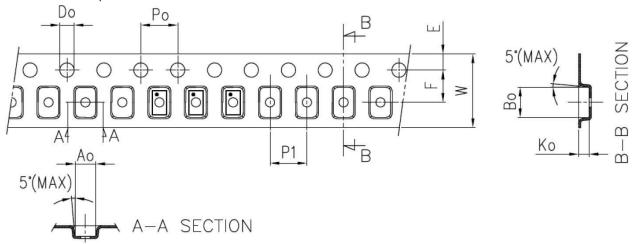
# **Tape and Reel Specification**

Package Type	# of	# of Pins Nominal Package Size (mm)	Max Units		Reel &	Trailer A		Leader B		Pocket (mm)	
	Pins		per reel	per box	Hub Size (mm)	Pockets	Length (mm)	Pockets	Length (mm)	Width	Pitch
STQFN 20L 2x3mm 0.4P Green	20	2x3x0.55	3000	3000	178/60	100	400	100	400	8	4

# **Carrier Tape Drawing and Dimensions**

Package Type	Pocket BTM Length (mm)	Pocket BTM Width (mm)	Pocket Depth (mm)	Index Hole Pitch (mm)	Pocket Pitch (mm)	Index Hole Diameter (mm)	Index Hole to Tape Edge (mm)	Index Hole to Pocket Center (mm)	Tape Width (mm)
	Α0	В0	K0	P0	P1	D0	E	F	w
STQFN 20L 2x3mm 0.4P Green	2.2	3.15	0.76	4	4	1.5	1.75	3.5	8

Refer to EIA-481 Specifications



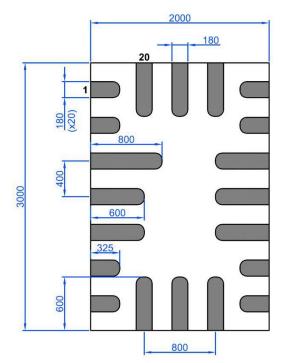
# **Recommended Reflow Soldering Profile**

Please see IPC/JEDEC J-STD-020: latest revision for reflow profile based on package volume of  $3.3 \ mm^3$  (nominal). More information can be found at  $\underline{www.jedec.org}$ .

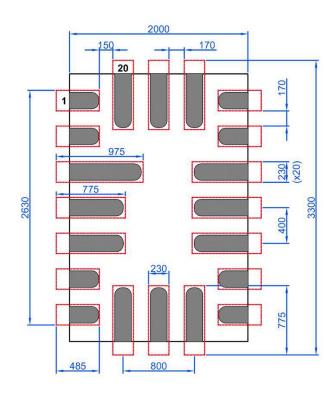
# **Recommended Land Pattern**



Units: μm







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TOYOSU FORESIA, 3-2-24 Toyosu, Koto-ku, Tokyo 135-0061, Japan www.renesas.com

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