Performance Comparison of IDT Tsi384™ and PLX PEX8114

80E1000_AN009_02

October 2, 2009

6024 Silver Creek Valley Road San Jose, California 95138

Telephone: (408) 284-8200 • FAX: (408) 284-3572

Printed in U.S.A.

1. Performance Comparison of IDT Tsi384 and PLX PEX8114

This report compares the data throughput of the IDT Tsi384 and the PLX PEX8114. The comparison data is based on tests performed in a PC environment for PCIe upstream transactions.

This document discusses the following:

Revision History

80E1000_AN009_02, Formal, October 2009

This document was rebranded as IDT. It does not include any technical changes.

80E1000_AN009_01, Formal, April 2009

This is the first version of the document.

1.1 Test Equipment Description

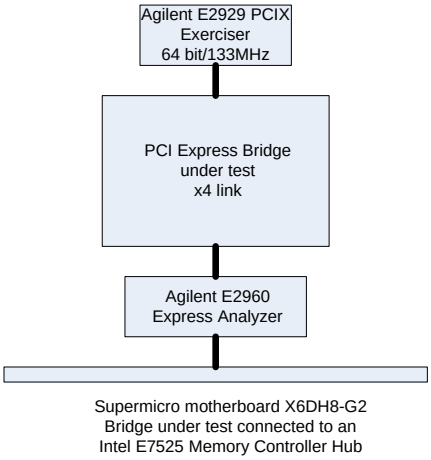
Tsi384 and PEX8114 data throughput is measured through the PCIe Root Complex in a Supermicro PC. This test platform was chosen because it is representative of a typical system using x4 PCIe plug-in cards (see Figure 1).

The Tsi384 PCIe bridge was tested using IDT's Tsi384 Evaluation Board. The PLX device was tested using the PEX8114 Forward Bridge RDK.

An Agilent E2929A PCI-X exerciser was used to initiate READ and WRITE transactions on the secondary side of the bridges.

An Agilent PCIe analyzer was used to measure data throughput and verify link parameters during the tests.

Figure 1: Test System Block Diagram



1.2 Test Equipment Configuration

1.2.1 Target Computer (Root Complex)

- Supermicro MBD-X6DH8-G2 motherboard
- Key features
  - Single Intel® 64-bit Xeon® up to 3.60 GHz, 800-MHz FSB
  - Intel® E7520 chipset
  - DDR2 400 SDRAM
- Tests performed in a x8 PCIe slot that connects to the Intel E7525 Memory Controller Hub (MCH)

1.2.2 Tsi384 Evaluation Board

- Revision E1000_AI001_05
- 100-MHz PCIe clock from PC
- 133.3-MHz PCI clock generated from the Tsi384
- Configuration:
  - Internal arbiter used
  - Default (power-up) configuration

1.2.3 PEX8114 RDK

- Populated with PEX8114BA
- 100-MHz PCIe clock from PC
- 133.3-MHz PCI clock generated from the bridge

- Configuration:
  - Internal arbiter used
  - Default (power-up) configuration

1.2.4 PCIe Analyzer

- Agilent E2947A Gen 1 (x4) passive Mid-bus probe board connected in computer's x8 slot
- Agilent N5305A Gen 1 I/O module and E2960 system for capturing data
- Agilent E2960 Protocol Analyzer software (Version 5.5.27.15), Release 6.14
- Measuring throughput with Realtime Statistic feature of the Protocol Analyzer software

1.2.5 PCI-X Exerciser

- Agilent E2929B PCI-X exerciser, 133.3 MHz, 64-bit
- Configured and controlled using various IDT-made test scripts

2. Upstream Write Throughput

In this test, data is transferred from the PCI-X exerciser into the PC's memory. The exerciser initiates posted write bursts to the bridge. For each test, one burst size is selected from 16 bytes to 4096 bytes. The writes are repeated continuously. The data throughput is measured on the PCIe links with the PCIe analyzer. The throughput measured represents the overall system performance.

Unfortunately, the PCI-X exerciser limits the system throughput significantly. For short burst writes, the exerciser cannot provide data to the bridge fast enough to exhibit the maximum capability of the device. In this case, the data throughput measured is actually the throughput of the test equipment, and not the bridge. The maximum data throughput of the bridge is reached when the burst size is large enough to compensate for the slow loop cycle of the exerciser. In this case, the bridge issues RETRY commands to the PCI-X exerciser, indicating that the device cannot transmit data fast enough to the PC memory.

The PCI signal traces in Figures 2 and 3 represent both burst size cases.

Figure 2: 256-Byte Burst Writes to Tsi384

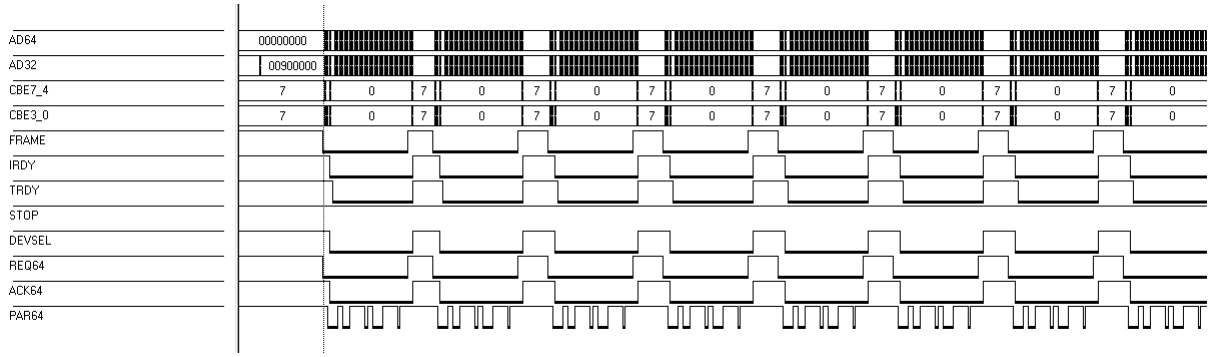
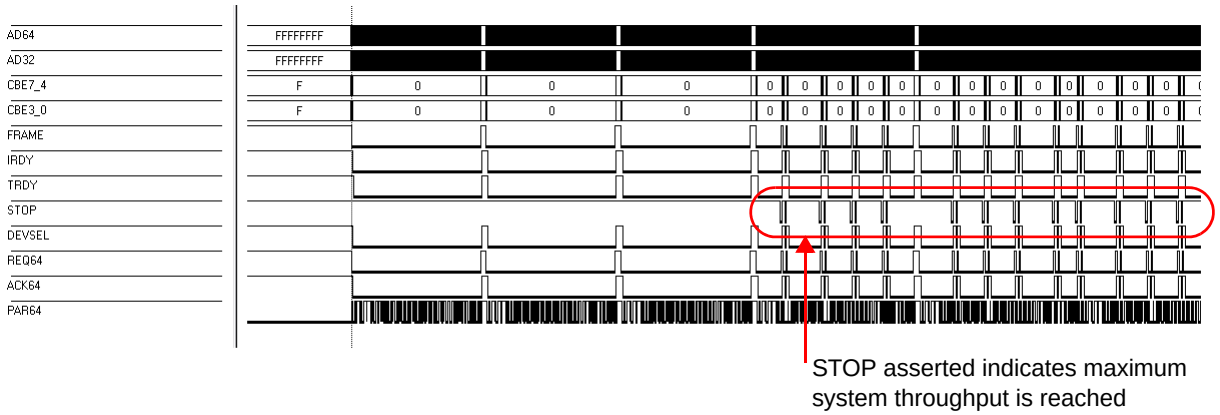


Figure 3: 2-KB Burst Writes to Tsi384



2.1 Test Results

Table 1 provides throughput measurement for the test system described in the previous sections:

- Data throughput is in Megabytes per second (1 MB = 1048576 bytes)
- Packet Size is limited to 128 bytes by the PC's MCH.
- Link Utilization is a comparison between the number of TLP and DLLP bytes and the total number of bytes.
- Link Efficiency is a comparison between the number of bytes in the payload and the number of bytes in TLPs and DLLPs.

Table 1: System Burst Write Throughput

Parameter	Bridge	
	Tsi384	PEX8114
Posted Writes 4096 Bytes		
Packet Size	128 Bytes	128 Bytes
Link Utilization	97.23%	92.56%
Link Efficiency	86.43%	86.42%
Data throughput (MBps)	801.53 MBps	762.95 MBps
Posted Writes 2048 Bytes		
Packet Size	128 Bytes	128 Bytes
Link Utilization	97.23%	92.56%
Link Efficiency	86.43%	86.42%
Data throughput (MBps)	801.53 MBps	762.95 MBps
Posted Writes 1024 Bytes		
Packet Size	128 Bytes	128 Bytes
Link Utilization	97.23%	92.56%
Link Efficiency	86.43%	86.42%
Data throughput (MBps)	801.53 MBps	762.95 MBps

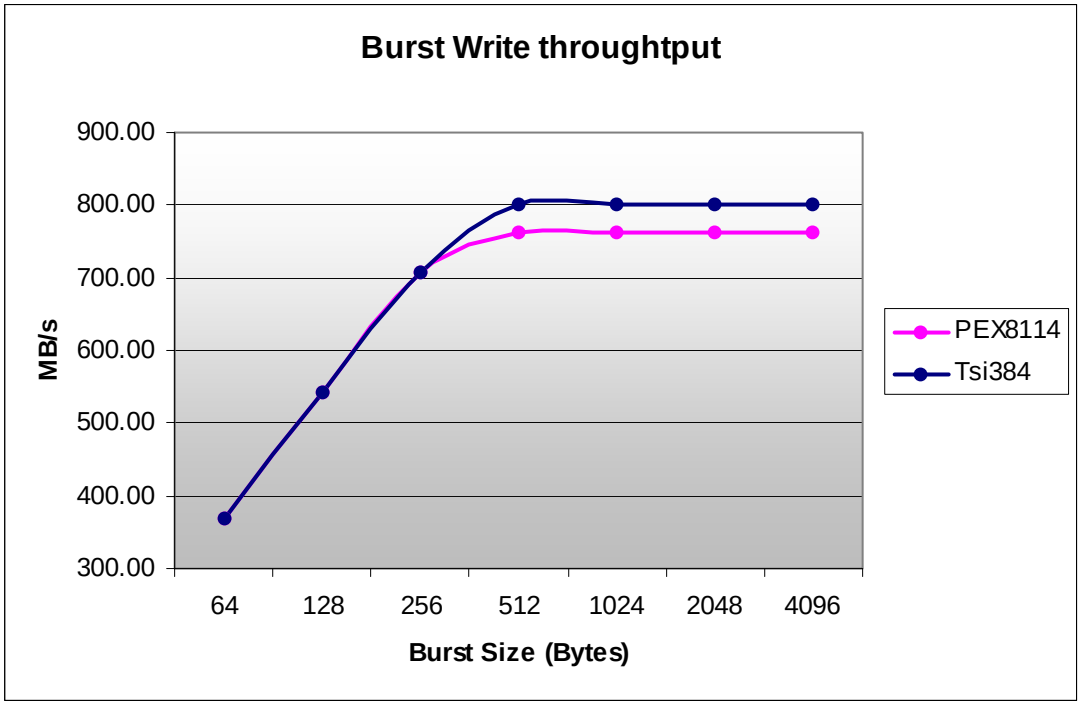
Table 1: System Burst Write Throughput *(Continued)*

Parameter	Bridge	
	Tsi384	PEX8114
Posted Writes 512 Bytes		
Packet Size	128 Bytes	128 Bytes
Link Utilization	97.23%	92.56%
Link Efficiency	86.43%	86.42%
Data throughput (MBps)	801.53 MBps	762.95 MBps
Posted Writes 256 Bytes		
Packet Size	128 Bytes	128 Bytes
Link Utilization	85.85%	85.86%
Link Efficiency	86.43%	86.42%
Data throughput (MBps)	707.66 MBps	707.66 MBps
Posted Writes 128 Bytes		
Packet Size	128 Bytes	128 Bytes
Link Utilization	65.83%	65.83%
Link Efficiency	86.41%	86.41%
Data throughput (MBps)	542.54 MBps	542.54 MBps
Posted Writes 64 Bytes		
Packet Size	64 Bytes	64 Bytes
Link Utilization	50.96%	50.96%
Link Efficiency	76.11%	76.11%
Data throughput (MBps)	369.91 MBps	369.91 MBps
Posted Writes 32 Bytes		
Packet Size	32 Bytes	32 Bytes
Link Utilization	31.56%	31.56%
Link Efficiency	61.43%	61.43%
Data throughput (MBps)	184.95 MBps	184.95 MBps

Table 1: System Burst Write Throughput *(Continued)*

Parameter	Bridge	
	Tsi384	PEX8114
Posted Writes 16 Bytes		
Packet Size	16 Bytes	16 Bytes
Link Utilization	24.05%	24.05%
Link Efficiency	44.34%	44.34%
Data throughput (MBps)	101.72 MBps	101.72 MBps

Figure 4: Tsi384 and PEX8114 Burst Writes Throughput



2.2 Test Conclusion

In the system described in this document, the bridge's maximum throughput is

- 801.53 MBps for the Tsi384
- 762.95 MBps for the PEX8114

The Tsi384 has about 5% more throughput than the PEX8114 in this test system.

3. Upstream Read Throughput

In this test, data is transferred from the PC's memory into the PCI-X exerciser. The exerciser initiates a read line command to the bridge. For each test, the read size is varied from 4 bytes to 4096 bytes in x2 increments. The read requests are repeated continuously. The data throughput is measured on the PCIe links with the PCIe analyzer. The throughput measured represents the overall system performance.

In most cases, the PCI-X exerciser can issue read requests faster than the PC can return the data. In this test, the data throughput measured is actually the throughput of the test system (PC, bridge, exerciser), rather than the bridge itself.

The Tsi384 can queue up to eight read requests before RETRY-ing the PCI-X bus. This feature helps improve throughput by reducing the delay between the completion of a first read and the start of a second read. The PEX8114 does not seem to queue read requests. The PCI-X bus is RETRY-ed on the second read request.

The PCI signal traces in Figures 5 and 6 represent read request queuing in the Tsi384 and PEX8114, respectively.

Figure 5: Tsi384 Read Request PCI-X Bus Cycles

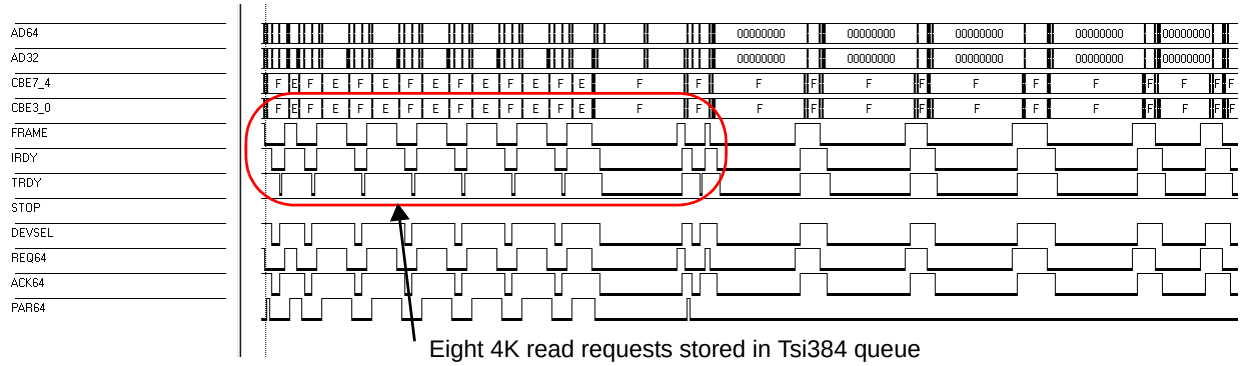
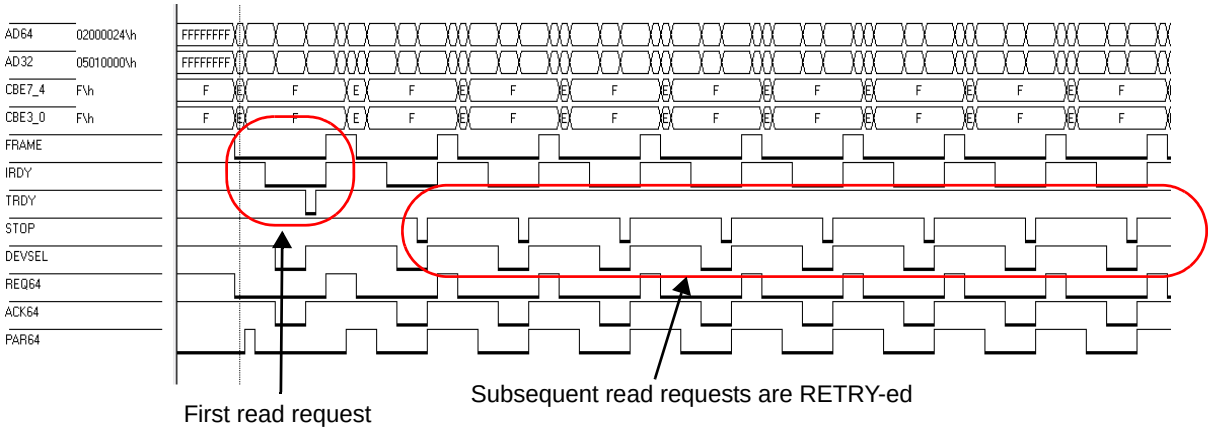


Figure 6: PEX8114 Read Request PCI-X Bus Cycles



3.1 Test Results

Table 2 provides throughput measurement for the test system described in the previous sections.

- Data throughput is in Megabytes per second (1 MB = 1048576 bytes).
- Packet size is limited to 64 bytes by the PC's MCH.
- Link Utilization is a comparison between the number of TLP and DLLP bytes and the total number of bytes.
- Link Efficiency is a comparison between the number of bytes in the payload and the number of bytes in TLPs and DLLPs.

Table 2: System Read Throughput

Parameter	Bridge	
	Tsi384	PEX8114
Memory Read 4096 Bytes		
Payload size	64 bytes	64 bytes
Link Utilization	99.34%	28.92%
Link Efficiency	73.70%	74.80%
Data throughput (MBps)	698.4 MBps	204.8 MBps
Memory Read 2048 Bytes		
Payload size	64 bytes	64 bytes
Link Utilization	99.32%	28.92%
Link Efficiency	73.88%	74.80%
Data throughput (MBps)	699.85 MBps	204.8 MBps
Memory Read 1024 Bytes		
Payload size	64 bytes	64 bytes
Link Utilization	99.36%	36.83%
Link Efficiency	74.20%	74.82%
Data throughput (MBps)	703.16 MBps	266.24 MBps
Memory Read 512 Bytes		
Payload size	64 bytes	64 bytes
Link Utilization	99.24%	34.55%
Link Efficiency	75.03%	74.98%
Data throughput (MBps)	710.19 MBps	245.76 MBps

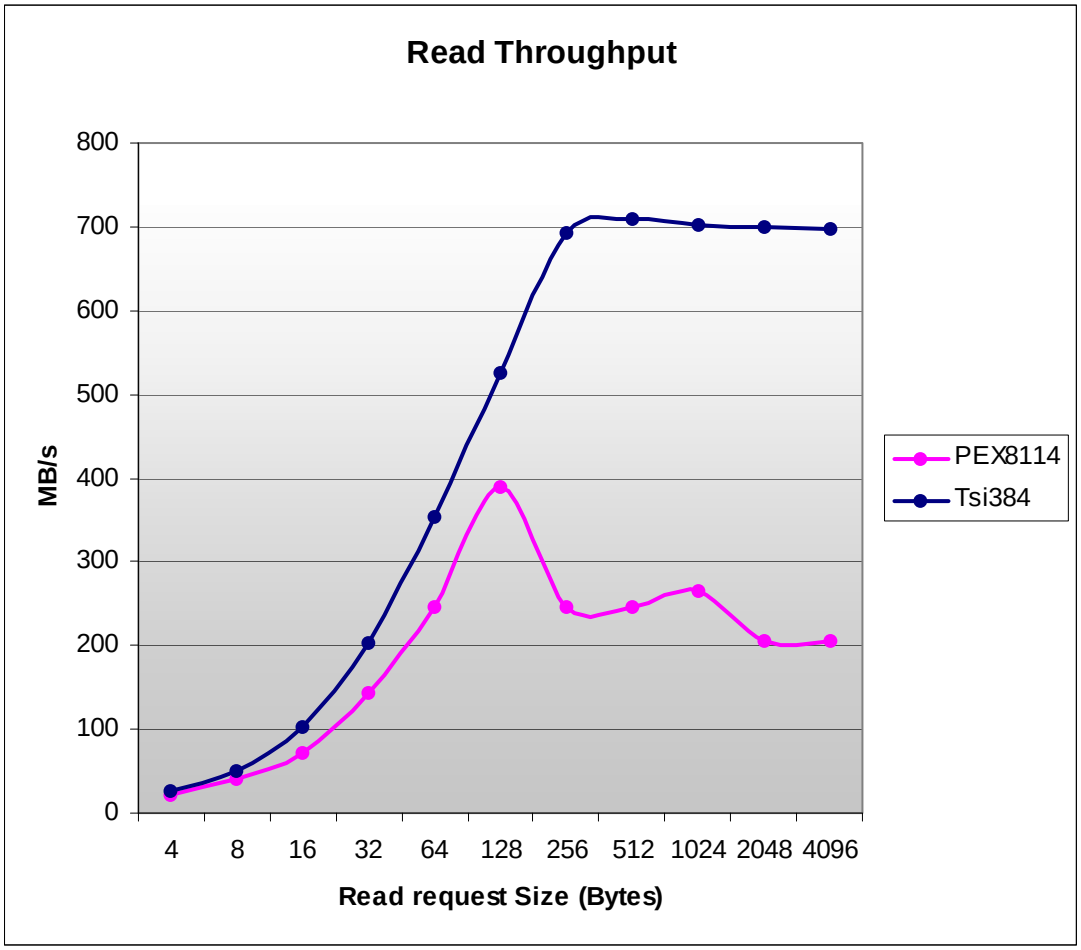
Table 2: System Read Throughput *(Continued)*

Parameter	Bridge	
	Tsi384	PEX8114
Memory Read 256 Bytes		
Payload size	64 bytes	64 bytes
Link Utilization	98.74%	33.72%
Link Efficiency	73.54%	73.71%
Data throughput (MBps)	692.61 MBps	245.76 MBps
Memory Read 128 Bytes		
Payload size	64 bytes	64 bytes
Link Utilization	77.43%	55.83%
Link Efficiency	71.09%	71.08%
Data throughput (MBps)	525.04 MBps	389.12 MBps
Memory Read 64 Bytes		
Payload size	64 bytes	64 bytes
Link Utilization	55.67%	36.58%
Link Efficiency	66.64%	66.63%
Data throughput (MBps)	353.83 MBps	245 MBps
Memory Read 32 Bytes		
Payload size	32 bytes	32 bytes
Link Utilization	42.68%	27.54%
Link Efficiency	49.97%	49.96%
Data throughput (MBps)	203.45 MBps	143.36 MBps
Memory Read 16 Bytes		
Payload size	16 bytes	16 bytes
Link Utilization	32.01%	21.35%
Link Efficiency	33.31%	33.30%
Data throughput (MBps)	101.72 MBps	71.68 MBps

Table 2: System Read Throughput *(Continued)*

Parameter	Bridge	
	Tsi384	PEX8114
Memory Read 8 Bytes		
Payload size	8 bytes	8 bytes
Link Utilization	26.68%	17.79%
Link Efficiency	19.98%	19.97%
Data throughput (MBps)	50.86 MBps	40.96 MBps
Memory Read 4 Bytes		
Payload size	4 bytes	4 bytes
Link Utilization	24.01%	16.01%
Link Efficiency	11.10%	11.09%
Data throughput (MBps)	25.43 MBps	20.48 MBps

Figure 7: Tsi384 and PEX8114 Read Throughput



3.2 Test Conclusion

The Tsi384 has better performance than PEX8114 mode for low-byte count and high-byte count read cycles in this test system. The Tsi384 provides a 340% performance improvements for high-byte count read requests.