Performance Comparison of IDT Tsi381 and TI XIO2000A

80E2000_AN005_02

October 1, 2009

6024 Silver Creek Valley Road San Jose, California 95138

Telephone: (408) 284-8200 • FAX: (408) 284-3572

Printed in U.S.A.

1. Performance Comparison of IDT Tsi381 and TI XIO2000A

This report compares the IDT Tsi381 versus the Texas Instruments XIO2000A. It highlights the performance advantages of using the Tsi381 over the XIO2000A.

This document discusses the following:

Terms

- Upstream transaction – In the context of a PCIe-to-PCI bridge, this transaction flow starts on a PCI bus and ends on a PCIe link.
- Downstream – In the context of a PCIe-to-PCI bridge, this transaction flow starts on a PCIe link and ends on a PCI bus.

Revision History

80E2000_AN005_02, Formal, October 2009

This document was rebranded as IDT. It does not include any technical changes.

80E2000_AN005_01, Formal, December 2008

This is the first version of the document.

1.1 Throughput Measurements

This section consists of a lab analysis comparison between the Tsi381 and the XIO2000A, as well as simulation throughput analysis of the Tsi381.

1.1.1 Lab Throughput Analysis

This section compares throughput measurements of the IDT Tsi381 and the TI XIO2000A. Please note that the throughput tests do not include bidirectional traffic. Each test is of a single direction of a particular size and type of transaction.

Unless noted, the default register settings for the devices were used.

1.1.1.1 PCI Upstream Reads

This test used an Agilent E2960 PCIe Exerciser connected to a PCI target/Analyzer (E2928) through a bridge. The Agilent E2960 was used as a root complex. The bridge card connected to the Agilent PCIe exerciser backplane. A PCI exerciser/analyzer is connected to the bridge card, and is used to initiate read request cycles. The Tsi381 was tested with its default configuration state and with pre-fetching/Short Term Caching enabled.

This test provides a relative performance comparison between the bridges, and is not a maximum throughput comparison. This is due to limitations in the response time of the PCIe target, as well as delays in the PCI exerciser initiating back-to-back cycles.

Payload Size (Bytes)	PCI Bus Speed (MHz)	Tsi381 Throughput (MBps)	TI XIO2000A Throughput (MBps)	IDT Performance Improvement
PCI Memory Read Multiple – "Without" Short-term Caching				
128	66	34.1	28.2	20.9%
64	66	18.3	14.9	22.8%
32	66	9.4	7.7	22.1%
16	66	4.8	3.8	26.3%
8	66	2.4	1.9	26.3%
PCI Memory Read Multiple – "With" Short-term Caching[a]				
128	66	86.8	N/A	N/A
64	66	59.3	N/A	N/A
32	66	32.9	N/A	N/A
16	66	17.4	N/A	N/A
8	66	8.9	N/A	N/A

a.The Tsi381's registers were configured as follows for the short-term caching test:

Prefetch Control Register (offset 0x0BC) = 0x03FFFFFF.

PCI Miscellaneous Control and Status Register (offset 0x044) = 0x7D9F_1900 (this sets the Short Term Caching Enable bit).

Summary

When the Tsi381's short-term caching is not enabled, the Tsi381 performance improvement over the XIO2000A increases according to the payload size. When the Tsi381's short-term caching feature is enabled, it can cause noticeable performance improvements for sequential transfers of a small payload size.

1.1.1.2 PCI Upstream Writes

This test used an Agilent E2960 PCIe Exerciser connected to a PCI-X Exerciser (E2929) through a 32-bit/66-MHz_64/133MHz PCI bridge card.

The hardware setup included an extra PCI-PCI bridge card that acted as a funnel for PCI data. The PCI exerciser used in the downstream test (Agilent E2928), however, cannot write data fast enough to saturate the bridge. In order to push as much data as possible through the bridge, a PCI-X exerciser running at 133 MHz was used to push data into the bridge faster than it can transfer it to the PCIe target. This resulted in retries on the PCI side of the bridge, and deemed it to be a good indication of the fastest upstream throughput.

Payload Size (Bytes)	PCI Bus Speed (MHz)	Tsi381 Throughput (MBps)	TI XIO2000A Throughput (MBps)	IDT Performance Improvement
128	66	212.3	206.1	3.0%
64	66	189.5	177.8	6.6%
32	66	153.1	142.9	7.1%
16	66	86.6	83.5	3.7%
8	66	45.3	42.8	5.8%

Summary

The Tsi381 device slightly outperformed the TI XIO2000A bridge for PCI upstream write transactions.

1.1.1.3 PCIe Downstream Reads

This test used an Agilent E2960 PCIe Exerciser connected to a PCI target/Analyzer (E2928) through a bridge. The Agilent E2960 was used as a root complex. The bridge card connects to the Agilent PCIe exerciser backplane. A PCI exerciser/analyzer is connected to the bridge card., and is used as a PCI target.

This test provides a relative performance comparison between the bridges, and is not a maximum throughput comparison. This is due to limitations in the response time of the PCI target, as well as delays in the PCIe exerciser initiating back-to-back cycles.

Payload Size (Bytes)	PCI Bus Speed (MHz)	Tsi381 Throughput (MBps)	TI XIO2000A Throughput (MBps)	IDT Performance Improvement
128	66	156.9	126.0	24.5%
64	66	93.9	73.4	27.9%
32	66	51.3	44.2	16.1%
16	66	27.7	22.5	23.1%
8	66	13.9	11.4	21.9%

Summary

The Tsi381 provides a 25% performance increase over the XIO2000A in downstream read performance.

1.2 Simulation Measurements

1.2.1 Test Setup

The Tsi381's simulation throughput was measured in the upstream and downstream directions for both read and write transactions. The results for both measurements are explained in the following sections, and indicates the maximum sustained throughput data that can be attained for the Tsi381 under optimal circumstances.

The test results were derived from simulation. The Tsi381's simulation environment consists of the Tsi381 device with bus functional models (BFMs) on both the PCI and PCIe interfaces. The BFMs were used to initiate read and write transactions through the Tsi381, as well as provide an ideal target response. The PCI bus frequency was equal to 66 MHz for all tests. This provides a test environment that measures maximum throughput for various types of transactions.

1.2.2 Test Results

1.2.2.1 Upstream Writes

PCI Burst Size (bytes)	Maximum Sustained Throughput (MBps)
32	147.1
64	183.3
128	208.9

1.2.2.2 Upstream Reads

PCI Burst Size (bytes)	Maximum Sustained Throughput (MBps)
32	128.7
64	159.3
128	162.2

1.2.2.3 Downstream Writes

PCIe Data Payload Size (bytes)	Maximum Sustained Throughput (MBps)
32	144.8
64	179.9
128	197.7

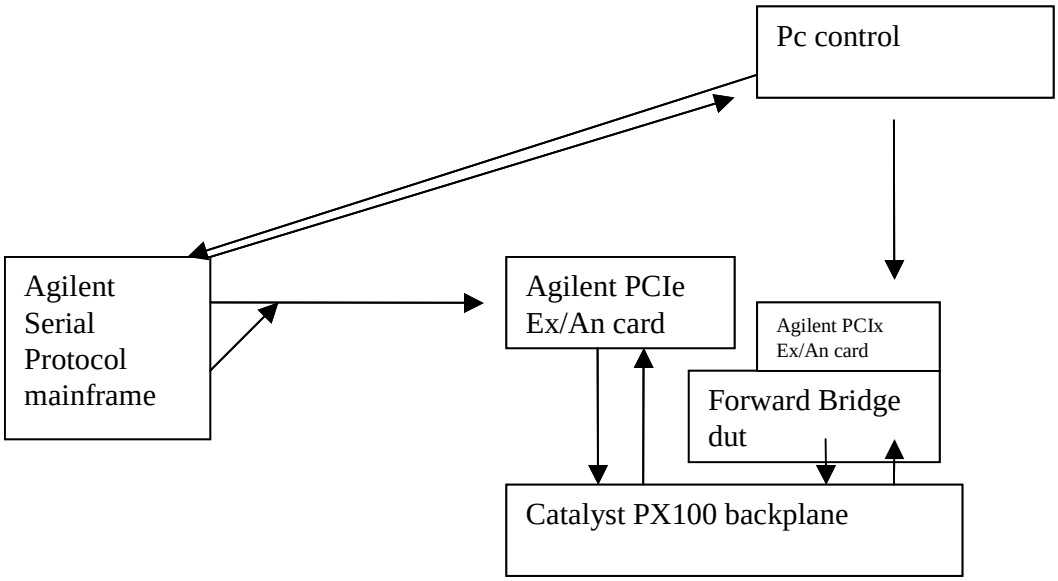
1.2.2.4 Downstream Reads

PCIe Data Payload Size (bytes)	Maximum Sustained Throughput (MBps)
32	110.9
64	159.4
128	193.9

1.3 Lab Throughput Test Setup

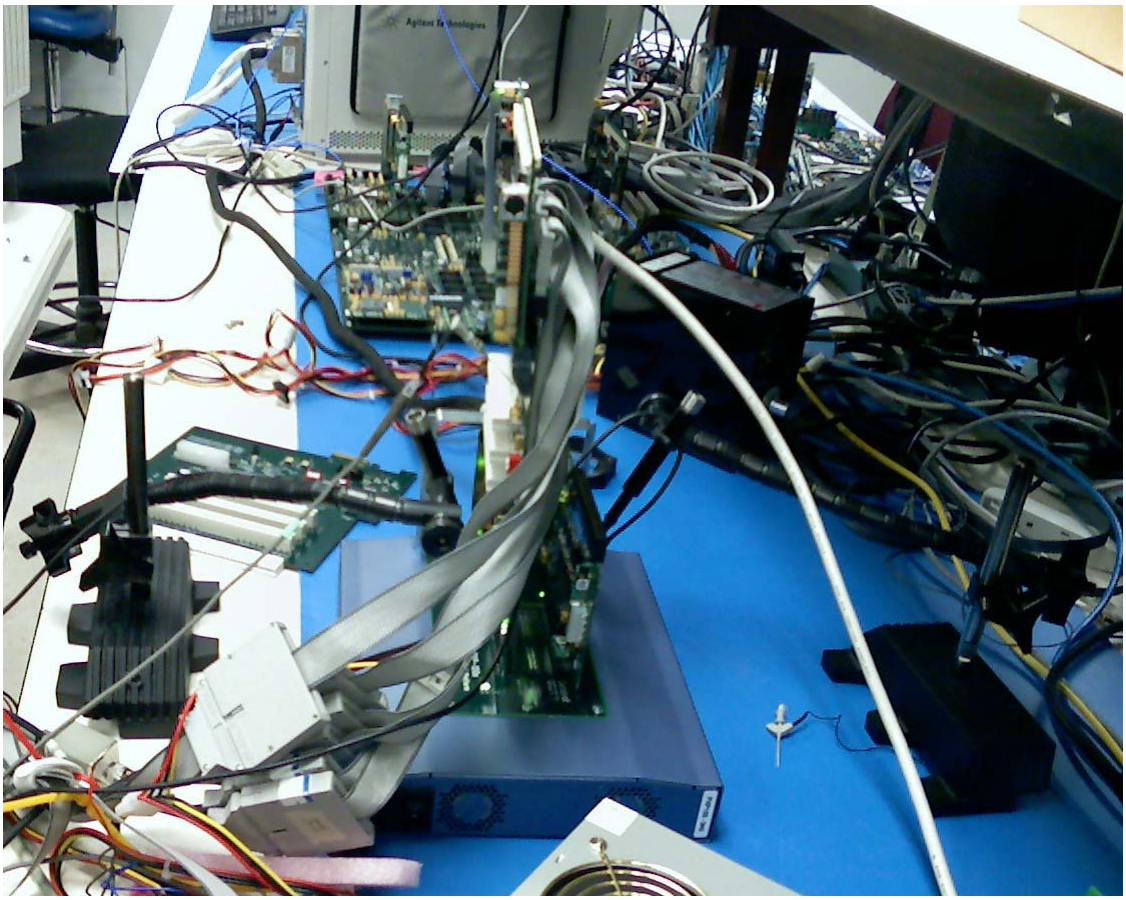
This section describes the hardware test environment.

Figure 1: System Setup



- A Catalyst two-slot backplane with model number PX100 was used.
- The appropriate (Tsi381, XIO2000A) evaluation board was connected directly into slot 1 of the Catalyst backplane.
- The Agilent E2928 PCI Exerciser/Analyzer card was plugged into the top slot of the evaluation board.
- An ATX power supply provided power to the PCI bus through a connector on the evaluation board.
- The Agilent PCIe Exerciser/Analyzer card was connected to slot 2 of the Catalyst backplane.
- The Catalyst backplane supplied power and reset to both boards, as well as clocking to the evaluation board.
- The Agilent PCIe Exerciser/Analyzer clock source was internal.
- The Agilent serial protocol mainframe was connected to the Agilent PCIe Exerciser/Analyzer card through the E2942A single probe Y-cable. This cable allowed the simultaneous use of one active probe board for the exerciser and analyzer (using two I/O modules).
- The Agilent Exerciser/Analyzer software operated on a Control PC. The PC was connected to the Agilent PCIe hardware through Ethernet.
- The Agilent PCI exerciser analyzer was connected to the Control PC through its proprietary fast-bus interface. The Control PC operated the Exerciser/Analyzer control software.
- The Control PC provided full control of stimulus and response of the PCIe and PCI sides of the bridge.

Figure 2: Complete Test Setup



PCIe Performance Measurement Method

Throughput was monitored using the Agilent E2960 Protocol Tester Realtime Statistics display. This display measures card performance in megabytes per second (MBps).

The actual measurement was taken from a TCL script provided by Agilent called PerformancePrint. This script was a text list of sequential measurements reported every second for 10 seconds.