PCIe 3.0 Retimer Frequently Asked Questions

89HT0832, 89HT0816, 89HT0808

This document provides answers to common questions about IDT PCIe 3.0 Retimer operation and system implementation. It is recommended as a starting point for design engineers who intend to use an IDT PCIe 3.0 Retimer. More detailed information about IDT Retimers is available in product datasheets, user manuals, and applications notes on the IDT website.

FAQ topics include the following:

Note: Unless explicitly stated otherwise, the following FAQ information applies to the 89HT0832, 89HT0816, and 89HT0808 PCIe 3.0 Retimers.

Architecture (System Application)

This section discusses questions on system-level architectures when using IDT PCIe 3.0 Retimers.

A1. Can the Retimer be used for smaller link widths, or to implement multiple links?

Yes. For example, the 8-lane T0816 has been designed specifically to support two 4-lane links controlled by the MERGE pin. The T0832 can support one 16-lane link, two 8-lane links, four 4-lane links, or one 8-lane plus two 4-lane links. Note that the 4-lane quad is the smallest increment for Retimer link configuration, and therefore the 8-lane T0816 cannot be configured for eight independent 1-lane links. Each Retimer automatically supports operation at a link width less than the maximum width, as determined by negotiation between the root complex (host) and endpoint. For example, a 4-lane link can operate as a 4-, 2- or 1-lane link depending on the endpoint/link partner.

A2. Can the Retimer be used in cascade (for example, at each end of a cable, or at both ends of a channel on blade servers)?

Yes. Cascading is a common system implementation and is fully supported by IDT Retimers.

A3. Can multiple Retimers be used in parallel for wider link widths?

No. PCIe3 Retimers cannot be used in parallel. IDT recommends selecting the correct Retimer width to match the maximum required link width; for example, a 4-lane (8-channel) Retimer for a 4-lane application, or a 16-lane (T0832) device for a 16-lane application.

A4. What happens if there is a Gen 1 or Gen 2 endpoint attached?

IDT PCIe 3.0 Retimers will match the actual rate of link operation as negotiated between the root complex and endpoint (that is, between the upstream and downstream link partners). For example, if a 5Gbps Gen 2 endpoint is inserted into an 8Gbps Gen 3 capable slot, the link will train to 5Gbps operation, and the Retimer will adjust appropriately for that data rate.

A5. Can the Retimer support link rate conversion?

No. For example, the IDT Retimers cannot provide an 8Gbps link on one side (upstream) and a 5Gbps link on the other (downstream). When a Retimer is inserted into the middle of a link to improve signal quality, the link is still formed between the upstream and downstream components that are enumerated within PCIe space. Both sides of the Retimer will operate at the data rate that is negotiated between those devices for communication.

A6. For 8Gbps PCIe 3.0 operation, what advantages does the Retimer offer over a re-driver?

A Retimer offers many advantages over a typical re-driver. For improving signal integrity a re-driver can only reduce Deterministic Jitter (Dj), but actually adds to the Random Jitter (Dj) it receives. A Retimer will eliminate Dj, and completely reset Rj (to a low value), so the transmitter signal is much cleaner giving better margins or enabling longer trace/cable. IDTs Retimers implement Decision Feedback Equalization, which is much more effective in correcting for non-linear signals distortions created by impedance discontinuities at connectors for the lowest Bit Error Rate (BER). IDT's Retimers have a reference clock and Clock Data Recovery (CDR) for converting the analog data signal into the digital domain, which allows for advanced features including automatic calibration, pattern generator/checker, and an on-die oscilloscope.

IDT's Retimers terminate the PCI SIG defined Equalization Procedure. This means that the device on the upstream side of the Retimer runs all phases, 0 through 3, of the Equalization Procedure with the upstream port of the Retimer, and similarly for the downstream port. The Equalization Procedure is required to optimize the equalization, both at the transmitter, and at the receiver, for each separate channel. A re-driver can interfere with the equalization procedure, especially phases 2 and 3 and can cause the link to fail the equalization procedure. This is only a partial list of IDT Retimer advantages.

A7. Can a PCIe Retimer and re-driver be used together on the channel in a series-cascade architecture?

No. A re-driver cannot terminate the Training Set data packets used by the Equalization Procedure for determining correct RX and TX operating parameters. If re-driver's RX and TX operation is not trained properly, the channel and link operation may be unreliable. An IDT PCIe3 Retimer fully executes all phases of the Equalization Procedure, independently on both sides, to ensure proper RX and TX configuration.

A8. Does an IDT Retimer support a repeater mode?

No. IDT offers Repeaters for data rates up to 6.25Gbps. At higher data rates, Retimers are strongly recommended for the improved jitter performance and other important features a Retimer can provide.

A9. IDT Retimers are "protocol aware." Does the Retimer offer control at the Data Link and Transaction Layers?

No. Data Link Layer (DLL) and Transaction Layer packets (TLP) pass through IDT Retimers without effect. IDT Retimers implement parts of the Physical Layer protocol and LTSSM training, including equalization training which is terminated at the Retimer, and link status and errors which are snooped by the Retimer. This is done to verify valid packets (at start up) and to keep its operation aligned with the root and endpoint.

A10. Why is equalization training terminated by the Retimer?

Placing a Retimer into the data path between link partners breaks the communication link into two completely independent physical segments, with one on either side of the Retimer (upstream and downstream segments). Each physical segment will typically have different channel electrical characteristics, requiring its own equalization optimization for 8Gbps operation, and is therefore performed between the Retimer and its link partner. Both segments are rarely identical (with the Retimer exactly in the middle of the link), so optimum equalization settings will be different for each side of the Retimer and its link partners.

Operation (Retimer IC)

This section discusses topics on specific features, capabilities, and hardware operation of IDT's PCIe 3.0 Retimers.

O1. What revision of the PCIe Base Specification is supported?

IDT Retimers are revision 3.0 compatible.

O2. Does the Retimer support DC balance?

Yes. IDT Retimers follow the PCIe 3.0 standard: Retimers can generate DC balance (it is under user control via register). The default setting enables DC balance. Retimers accept DC balance.

O3. Does the Retimer support Back Channel Equalization?

Yes. Note that the term Back Channel Equalization is used in earlier revisions of the standard, and was dropped in rev 0.71. The released PCIe 3.0 revision calls this the Equalization Procedure (often called automatic equalization procedure). Phase 2 and 3 of the Equalization Procedure defines a mechanism for requesting different presets or coefficients from the link partner – this is the "back channel", and is fully supported by IDT Retimers.

O4. What is the gain of the Retimer at 8Gbps?

The benefit of using an IDT Retimer is far more than simple linear gain. The DFE Rx equalizer and FIR Tx equalizer are powerful functions for correcting for non-linear distortions caused by impedance discontinuities from via, connectors, and PCB/cable changes that produce reflections and exaggerate ISI. So by itself, gain is an insufficient parameter to indicate the benefit of a Retimer. An IDT Retimer's gain is highly configurable and adaptable, at both the Rx and TX nodes, allowing for optimized system operation. However, as a very simple reference point considering minimum input swing and maximum output swing (into 50-Ohm loads), the Retimer gain is approximately 30dB.

O5. What is the Rx DFE tap architecture?

The Decision Feedback Equalizer is 5-taps. 4 taps are normal (N-1, N-2, N-3, N-4); one tap has pulse shaping, with programmable pulse shape. A single pulse shaped tap can compensate for linear loss in the channel. The normal taps are used for equalizing discontinuities.

O6. Is hot-plug supported?

Yes, when the PCIe standard for hot-plug system implementation is followed.

After initialization and during normal operation, the Retimer is a transparent device that simply passes messages (including those related to hot plug) back and forth. When the Retimer is placed on the mother-board in a typical application, and connects to the root complex (or switch) on the upstream port, and an open slot on the downstream port hot plug is supported as follows:

- When the system powers up and no card is present in the slot, the Retimer checks for Rx termination on the slot, via the standard defined Detect protocol. It will find no receivers present, and leave its Rx termination high Z on its upstream port. Thus the switch or root complex will see an open slot when it performs the detect protocol on the Retimer. When the card is plugged in, the Retimer will detect the card, and turn on its Rx impedance facing the switch/root complex, which will intern detect the card.
- When a card is removed the slot reset is asserted. The slot reset is connected to port reset on the Retimer, which forces the Rx impedance high on the port facing the switch/root complex, so that the switch/root complex will detect an open slot.

O7. Does the Retimer support loopback compliance mode for measuring system margins?

The Retimer offers proprietary loopback modes for checking between the Retimer and its upstream or downstream link partner. For PCIe "standard based" loopback, after the Retimer is properly configured it will pass the data through to the link partner and/or compliance board. The link partner acts as the slave loopback device. The Retimer acts as a wire for PCIe defined master/slave loopback.

O8. Does the Retimer support presets 7 and 8 in Phase 1?

Yes. IDT PCIe 3.0 Retimers support all standard presets, and the full transmitter coefficient matrix as defined by the *PCIe 3.0 Base Specification*.

O9. Can the Retimer accept the walking coefficient request in Phase 2/3 that supports margin characterization (this is important to system compatibility)?

Yes, this is required by the standard.

O10. How can I identify the loaded EEPROM firmware revision?

This is easily implemented via the I2C/SMB interface. There is a 32-bit debug register for defining TS1 test pattern in the Retimer. This register can be used to store the revision identifier (ID) of your EEPROM version and to read it via I2C/SMB access any time it is needed.

Note, that with a Retimer this is not a PCIe standard CFG read operation since a Retimer is not an enumerated device but is a non-participating device for most of the PCIe protocol point of view.

O11. What is the purpose of the DIR pin?

The DIR pin supports the Equalization Procedure of PCIe 3.0 and other aspects of link training. The link training procedure always begins at the upstream device (root complex). The DIR pin tells the Retimer which port is connected to the upstream device in order to facilitate proper link training. Note the polarity of this signal during design, so that it correctly matches the board architecture and implementation. This pin has a complimentary register bit so that the direction can be changed via firmware. Also note that the 89HT0808 does not provide a DIR pin, so orientation can only be changed via register.

Design (Schematic)

This section addresses questions about schematic design for IDT PCIe 3.0 Retimers.

D1. How should the preset and hint strapping pins be set?

This is very board specific based on channel lengths. IDT recommends that these pins go to a jumper block where they can be strapped either to VDD, open, or VSS. The pin values can be overwritten during EEPROM download. IDT can provide suggestions for setting the initial state of these pins on a specific board design.

D2. The Retimer has digital and analog VDD inputs both at 1.0V. Can the same supply be used for both?

Yes, the same power supply rail can be used for both 1.0V inputs. If one source is used, then ferrite beads are recommended to isolate the analog from digital. Signal conditioners work best with a clean power source and to achieve optimum performance using separate supplies that fully isolate a noisy digital power plane from the analog plane are recommended (as implemented on IDT's Evaluation Board reference designs). This can be very practical when multiple Retimers are used on a single PCB and the incremental cost and area are small. The best results will be obtained from a low noise power source.

D3. Is an EEPROM required?

Provisioning the PCB for a local Retimer EEPROM is highly recommended since an EEPROM is required for most applications. The EEPROM is used to configure 5Gbps operation (the PCIe standard does not define automatic equalization for gen-2) and for other optimizations. One advantage of implementing a local EEPROM is its quick speed in loading the Retimer before link training begins. A second advantage is that the Retimer firmware is then independent of BIOS and other unrelated system firmware. Note that a single EERPOM can support automatic configuration for up to eight Retimers.

The only case where a Retimer EEPROM may not be needed is if the Retimer can be loaded via I2C/SMB before any PCIe training begins. The designer must have full control over the system BIOS and a method for implementing and executing the appropriate Retimer code before link training begins.

Layout (PCB)

This section addresses questions relevant to PCB layout with IDT PCIe 3.0 Retimers.

L1. Does IDT supply layout models? For which tools?

Yes. IDT often uses Allegro for generating original source files. Models are available for OrCAD and other formats by request. Gerber files are also available for our reference evaluation boards.

L2. Can IDT provide a trace breakout and power decoupling recommendation?

Yes. These can be seen on the evaluation board documentation.

L3. Can P/N Rx inputs and P/N Tx outputs be independently swapped in the Retimer for easier routing? Can both input and output sides be swapped?

Yes, Retimers support polarity inversion. Either one side, or both sides of the Retimer signals can be inverted.

L4. Can lane Rx/Tx pin locations be reassigned in the Retimer to support easier routing?

No. IDT Retimers do not include a general crosspoint routing matrix for connecting any RX to any TX. The RX-to-TX path through the Retimer uses a fixed set of contacts. However, the ability to support lane reversal is provided by the Retimer, assuming both root complex and endpoint devices also support it (this is a normal PCIe requirement). The Retimer does not have an active role in lane reversal.

System (Power and other Implementation Considerations)

This section discusses implementation questions when using an IDT PCIe 3.0 Retimer, which are not specific to architecture, schematic, or layout.

S1. Is a heat sink required or recommended?

Determining if a heat sink is required is very specific to the individual system design, and needs to take into consideration ambient airflow and temperature, and heat from other adjacent components. Thermal characteristics for the Retimers can be referenced within the datasheet and can be used as part of the overall system level thermal analysis. An Application Note on thermal design for Retimers is also available from IDT.

IDT does not use a heat sink on its 4- and 8-lane Retimer evaluation boards which are typically used in an open chassis environment, but a wide variety of heat sinks are commercially available.

Utilities (Software and Tools)

This section addresses topics on IDT software, evaluation boards, and other tools that support IDT's PCIe 3.0 Retimers.

U1. Which device do you use for controlling the Retimer's I2C/SMB bus?

There are many devices available that provide I2C/SMB interface from a PC. IDT has had good success using the Aardvark I2C/SPI Embedded Systems Interface available from the Total Phase company. IDTs Windows Retimer configuration and on-die scope utilities are implemented and validated using the Aardvark. Including a header on your board design to allow for Aardvark attachment is recommended.

Miscellaneous (Simulation, Test, Quality, etc.)

This section addresses topics on simulation and modeling, testing, quality, documentation, and other topics relating to IDT's PCIe 3.0 Retimers.

M1. What tools are available for simulation?

IDT offers IBIS-AMI models for the Retimers.

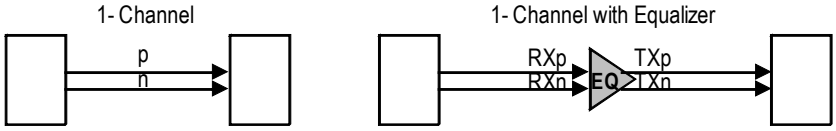
M2. How do I test and verify 8Gbps Gen 3 operation?

IDT offers system evaluation boards for testing the Retimer's operation. These evaluation boards have a form factor similar to a PCIe standard card and can plug into a PCIe slot in an open chassis, PCIe 3.0, desktop PC system board or server. A PCIe 3.0 endpoint adapter (SAS, Ethernet, Infiniband, etc.) is installed into the top of the evaluation board to create a compete signal/data path for testing interoperability. Lab instruments from Agilent, LeCroy, or Tektronix can be used to perform a more detailed analysis of 8Gbps Gen 3 Retimer operation in any design.

Glossary

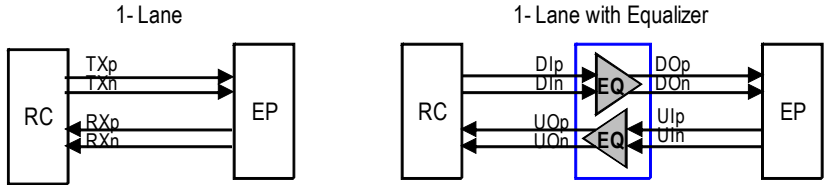
Terminology for signal conditioners has not been fully standardized by the industry, and confusion can sometimes result. To help clarify the information used in this document, the following terms are defined. These definitions are are with respect to multi-gigabit-per-second digital differential signaling. For a comprehensive list of PCIe terms, see “Terms and Acronyms” in the *PCI Express Base Specification*.

Term	Definition
Channel	A differential pair of signals (p & n) connecting two components (for example, root complex to endpoint). A channel is a connection providing unidirectional communication (or simplex). IDT defines a one-channel signal conditioner as having four data signal pins total (input and output). IDT part numbers for signal conditioner products specify the number of serial-differential channels provided.



When an active signal conditioner (equalizer) is placed in the channel as shown above, the channel is split into two physical segments, with one set of signals on each side of the repeater/retimer (often called upstream and downstream). In this diagram the signals are labeled with respect to the equalizer, receiver inputs RX(p:n), and transmitter outputs TX(p:n).

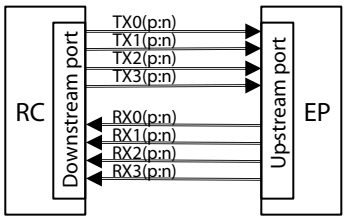
DFE	Decision Feedback Equalizer. A powerful equalization technique that combines digital pattern dependent gain, evaluated across multiple UI periods, to a received signal to compensate for ISI, reflections, and non-linear distortions.
Equalizer	A filter circuit or device with frequency dependent input-to-output gain. Passive or active, and both analog or digital equalizers, are all in common use. Equalizer circuits are the key element in most Signal Conditioners, and the term Equalizer is often used interchangeably (synonymous) with Signal Conditioner.
FIR	Finite Impulse Response (filter). A simple, deterministic filter circuit design used by PCIe in the transmitter circuit to pre-compensate a transmitted signal for channel distortion.
ISI	Inter-Symbol Interference. One type of Deterministic Jitter resulting from the non-ideal wire characteristic of having greater impedance at higher frequencies, which spreads the signal energy and causes dynamic variations in slew rate and switching amplitude, resulting in bit-to-bit overlap of a high speed signal.
Jitter	Jitter is the undesired time variance of a signal. Jitter has many causes, including deviations in source clock timing, from thermal noise, EMI and crosstalk, power variations, etc. Total Jitter (Tj) has components of Random Jitter (Rj) and Deterministic Jitter (Dj). Tj=Rj+Dj.
Lane	A set of differential signal pairs, one pair for transmission and one pair for reception. A pair of channels in an upstream/ downstream configuration (that is, dual-simplex). A by-N Link is composed of N Lanes. A signal conditioner for one lane would have 8-wires total, as displayed below (downstream: DI(p:n), DO(p:n) and upstream: UI(p:n), UO(p:n).



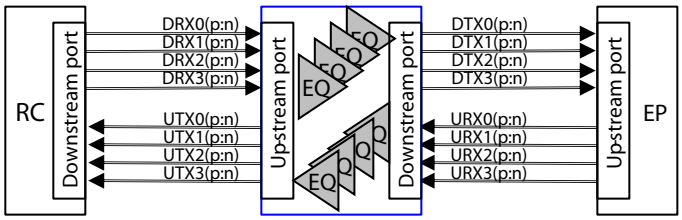
Link

The collection of two ports and their interconnecting lanes. A link is dual-simplex communications path between two components. A 4-lane link is displayed below.

4-Lane Link



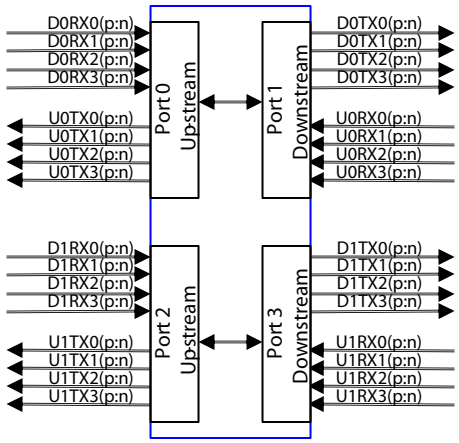
4-Lane Link with Equalizer



Port

A group of Transmitters and Receivers located on the same component that operate together. Two ports form the ends of a serial communications link. A four-port Retimer that supports two independent links, each with 4 lanes, is diagrammed below.

4-Port Device
(for 2-links of 4-lanes each)



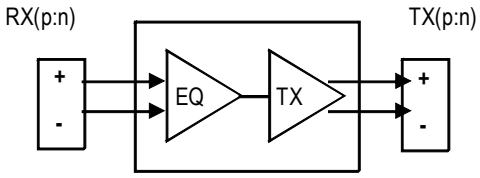
Re-driver

An equivalent term synonymous with IDT's definition of Repeater. Repeaters and re-drivers generally feature equivalent functions and capabilities. See Repeater.

Repeater

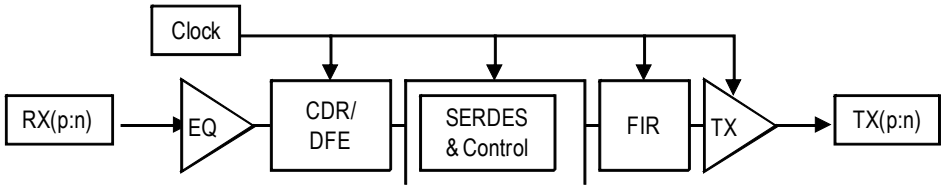
An active signal conditioner, featuring a low-latency analog data path from input to output (RX to TX). Repeaters can correct for some Deterministic Jitter (Dj) and Inter-Symbol Interference (ISI), and can restore a signal's amplitude to correct for channel attenuation.

IDT's repeaters provide active receiver equalization and output gain, and can be thought of as having two major functional blocks as displayed below. The RX equalizer is a programmable Continuous Time Linear Equalizer (CTLE) that can correct linear channel distortion. The TX transmitter provides programmable de-emphasis to pre-compensate for channel losses (a type of equalization).



Retimer

An active signal conditioner, featuring a Clock Data Recovery circuit that retimes the transmitter output to a reference clock. A Retimer eliminates input Deterministic jitter (Dj) and resets Random Jitter (Rj) to a low value. Retimers provide the best signal margins over longer traces, but add system clock delay latency.



The RX receiver stage of IDT Retimers feature a sensitive analog front end (AFE) and CTLE equalizer for linear distortion (similar to a Repeater's), which is followed by a CDR and DFE stage. The CDR converts the input into the digital domain allowing for packet snooping, sophisticated analysis, and enhanced features such as an on-die scope. The DFE function enables correction of non-linear input signal distortion.

The TX transmitter stage uses a reference clock input for re-timing the output data, while the FIR stage supports eight programmable output levels including TX signal boost and pre-shoot levels.

Signal Conditioner

An Active Signal Conditioner (aka, Equalizer) is an amplifier with frequency dependent input-to-output gain, which can correct for signal distortion created in the communication channel. Its purpose is to enable longer communication distances by restoring the signal quality.

Signal conditioners can be categorized as either repeaters or retimers, having either an analog or digital internal data path, respectively, as determined by whether a Clock Data Recovery (CDR) circuit has been implemented.

Note the term signal conditioner is also commonly used to describe amplifiers for low-speed analog sensors, which are significantly different in design (and market application) than IDT Retimers.

CORPORATE HEADQUARTERS
6024 Silver Creek Valley Road
San Jose, CA 95138

for SALES:
800-345-7015 or 408-284-8200
fax: 408-284-2775
www.idt.com

for Tech Support:
email: ssphelp@idt.com