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Renesas Electronics Corporation

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Renesas Technology Corp.
Customer Support Dept.
April 1, 2003

M16C/30 Group

Usage Notes Reference Book

Renesas 16-BIT SINGLE-CHIP MICROCOMPUTER
M16C FAMILY / M16C/30 SERIES

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Preface

This book describes the M16C/30 group's precautions for use, which contains paragraphs describing precautions of the user's manual and technical news relevant to these paragraphs. Please refer to this book when developing your systems. However, all of precautions are not contained in this book, please perform sufficient evaluation under systems development.

1.1 Precautions for Interrupts

1.1 Precautions for Interrupts

1.1.1 Reading address 00000₁₆

When maskable interrupt is occurred, CPU reads the interrupt information (the interrupt number and interrupt request level) in the interrupt sequence.

The interrupt request bit of the certain interrupt written in address 00000₁₆ will then be set to "0".

Even if the address 00000₁₆ is read out by software, "0" is set to the enabled highest priority interrupt source request bit. Therefore interrupt can be canceled and unexpected interrupt can occur.

Do not read address 00000₁₆ by software.

1.1.2 Setting the stack pointer

The value of the stack pointer immediately after reset is initialized to 0000₁₆. Accepting an interrupt before setting a value in the stack pointer may become a factor of runaway. Be sure to set a value in the stack pointer before accepting an interrupt. When using the $\overline{\text{NMI}}$ interrupt, initialize the stack pointer at the beginning of a program. Concerning the first instruction immediately after reset, generating any interrupts including the $\overline{\text{NMI}}$ interrupt is prohibited.

1.1.3 The $\overline{\text{NMI}}$ interrupt

1. The $\overline{\text{NMI}}$ interrupt can not be disabled. Be sure to connect $\overline{\text{NMI}}$ pin to Vcc via a pull-up resistor if unused. Be sure to work on it.
2. The $\overline{\text{NMI}}$ pin also serves as P85, which is exclusively input. Reading the contents of the P8 register allows reading the pin value. Use the reading of this pin only for establishing the pin level at the time when the $\overline{\text{NMI}}$ interrupt is input.
3. Do not attempt to go into stop mode with the input to the $\overline{\text{NMI}}$ pin being in the "L" state. With the input to the $\overline{\text{NMI}}$ being in the "L" state, the CM10 is fixed to "0", so attempting to go into stop mode is turned down.
4. Do not attempt to go into wait mode with the input to the $\overline{\text{NMI}}$ pin being in the "L" state. With the input to the $\overline{\text{NMI}}$ pin being in the "L" state, the CPU stops but the oscillation does not stop, so no power is saved. In this instance, the CPU is returned to the normal state by a later interrupt.
5. Signals input to the $\overline{\text{NMI}}$ pin require "L" level and "H" level of 2 clock +300ns or more, from the operation clock of the CPU.

1.1.4 External interrupt

1. Either an "L" level or an "H" level of at least 250 ns width is necessary for the signal input to pins $\overline{\text{INT}}_0$ through $\overline{\text{INT}}_2$ regardless of the CPU operation clock.
2. When the polarity of the $\overline{\text{INT}}_0$ to $\overline{\text{INT}}_2$ pins is changed, the interrupt request bit is sometimes set to "1". After these changes were made, set the interrupt request bit to "0". Figure 1.1.1 shows the procedure for changing the $\overline{\text{INT}}$ interrupt generate factor.

1.1 Precautions for Interrupts

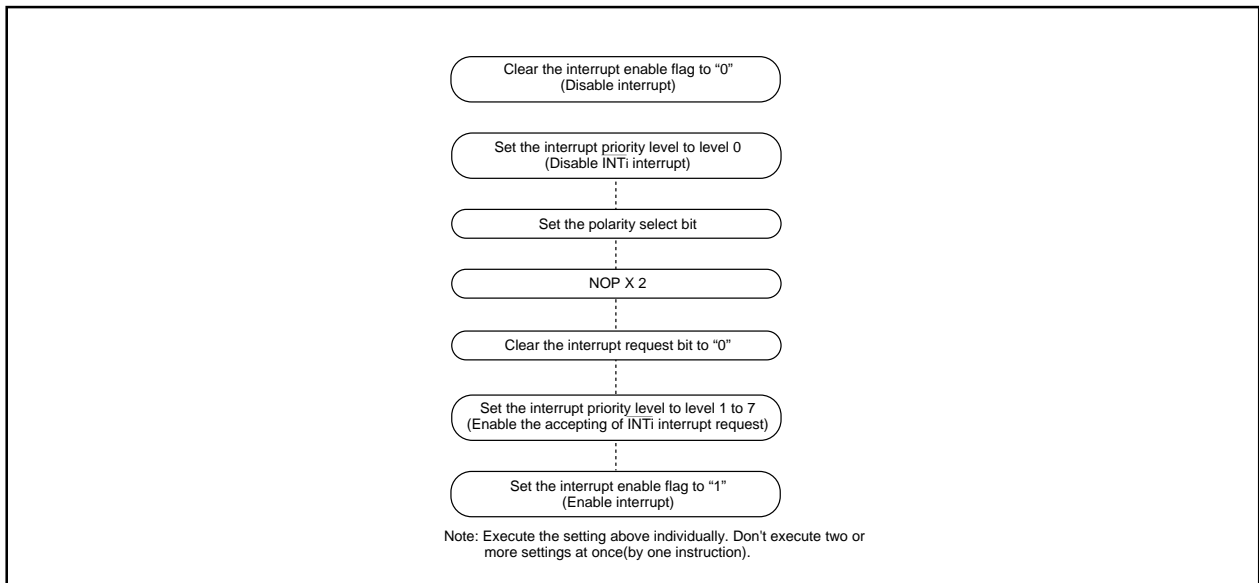


Figure 1.1.1. Switching condition of INT interrupt request

1.1 Precautions for Interrupts

1.1.5 Rewrite the interrupt control register

To rewrite the interrupt control register, do so at a point that does not generate the interrupt request for that register. If there is possibility of the interrupt request occur, rewrite the interrupt control register after the interrupt is disabled. The program examples are described as follow:

Example 1:

```
INT_SWITCH1:
  FCLR  I           ; Disable interrupts.
  AND.B #00h, 0055h ; Clear TA0IC int. priority level and int. request bit.
  NOP                               ; Four NOP instructions are required when using HOLD function.
  NOP
  FSET  I           ; Enable interrupts.
```

Example 2:

```
INT_SWITCH2:
  FCLR  I           ; Disable interrupts.
  AND.B #00h, 0055h ; Clear TA0IC int. priority level and int. request bit.
  MOV.W MEM, R0     ; Dummy read.
  FSET  I           ; Enable interrupts.
```

Example 3:

```
INT_SWITCH3:
  PUSHC FLG        ; Push Flag register onto stack
  FCLR  I           ; Disable interrupts.
  AND.B #00h, 0055h ; Clear TA0IC int. priority level and int. request bit.
  POPC  FLG        ; Enable interrupts.
```

The reason why two NOP instructions (four when using the HOLD function) or dummy read are inserted before FSET I in Examples 1 and 2 is to prevent the interrupt enable flag I from being set before the interrupt control register is rewritten due to effects of the instruction queue.

When changing an interrupt control register in a state of interrupts being disabled, please read the following precautions on instructions used before changing the register.

(1) Changing a non-interrupt request bit

If an interrupt request for an interrupt control register is generated during an instruction to rewrite the register is being executed, there is a case that the interrupt request bit is not set and consequently the interrupt is ignored. This will depend on the instruction. If this creates problems, use the below instructions to change the register.

Instructions : AND, OR, BCLR, BSET

(2) Changing the interrupt request bit

When attempting to clear the interrupt request bit of an interrupt control register, the interrupt request bit is not cleared sometimes. This will depend on the instruction. If this creates problems, use the below instructions to change the register.

Instructions : MOV

1.2 Precautions for Protect

1.2 Precautions for Protect

The write-enable bit of port 9 direction register goes to “0” when the next write instruction is executed after write-enabled state is readied. Make changes in input/output immediately after the instruction that sets “1” in the write-enable bit of port P9 direction register (avoid causing an interrupt). Also take measures to prevent DMA transfer from being executed.

1.3 Precautions for Timer A

Precautions for Timer A

1.3.1 Precautions for Timer A (timer mode)

1. After reset, the count start flag is set to "0". Set a value in the timer Ai register, then set the flag to "1".
2. Reading the timer Ai register while a count is in progress allows reading, with arbitrary timing, the value of the counter. Reading the timer Ai register with the reload timing shown in Figure 1.3.1 gets "FFFF₁₆". Reading the timer Ai register after setting a value in the timer Ai register with a count halted but before the counter starts counting gets a proper value.

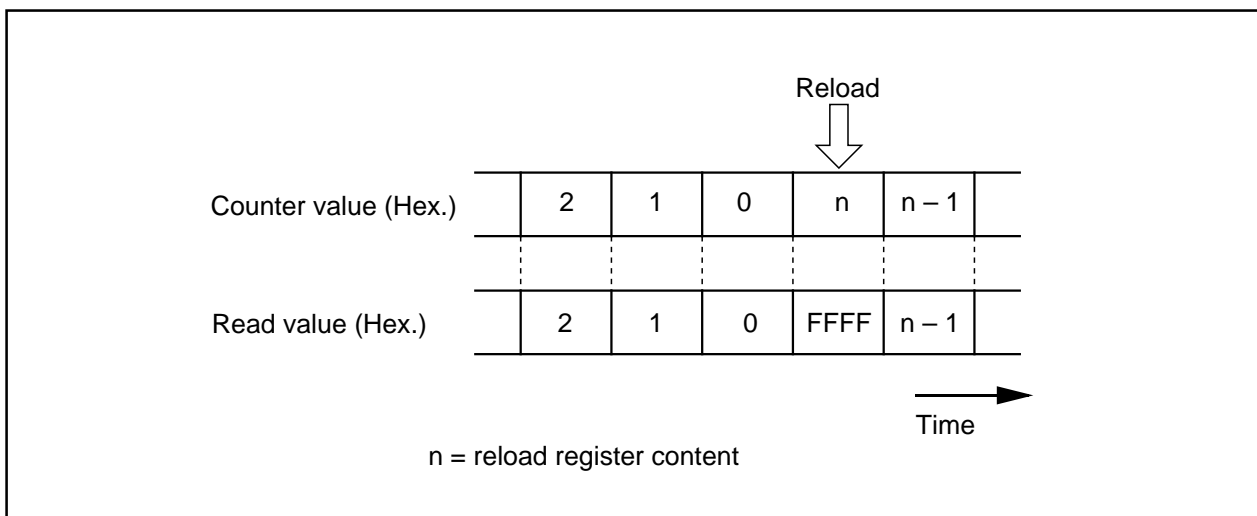


Figure 1.3.1. Reading timer Ai register

1.3 Precautions for Timer A

1.3.2 Precautions for Timer A (event counter mode)

1. After reset, the count start flag is set to "0". Set a value in the timer Ai register, then set the flag to "1".
2. Reading the timer Ai register while a count is in progress allows reading, with arbitrary timing, the value of the counter. Reading the timer Ai register with the reload timing shown in Figure 1.3.2 gets "FFFF₁₆" by underflow or "0000₁₆" by overflow. Reading the timer Ai register after setting a value in the timer Ai register with a count halted but before the counter starts counting gets a proper value.
3. Please note the standards for the differences between the 2 pulses used in the 2-phase pulse signals input signals to the TA2IN pin and TA2OUT pin, as shown in Figure 1.3.3.
4. When free run type is selected, if count is stopped, set a value in the timer Ai register again.
5. In the case of using as "Free-Run type", the timer register contents may be unknown when counting begins. If the timer register is set before counting has started, then the starting value will be unknown.
 - **In the case where the up/down count will not be changed.**
Enable the "Reload" function and write to the timer register before counting begins. Rewrite the value to the timer register immediately after counting has started. If counting up, rewrite "0000₁₆" to the timer register. If counting down, rewrite "FFFF₁₆" to the timer register. This will cause the same operation as "Free-Run type" mode.
 - **In the case where the up/down count has changed.**
First set to "Reload type" operation. Once the first counting pulse has occurred, the timer may be changed to "Free-Run type".

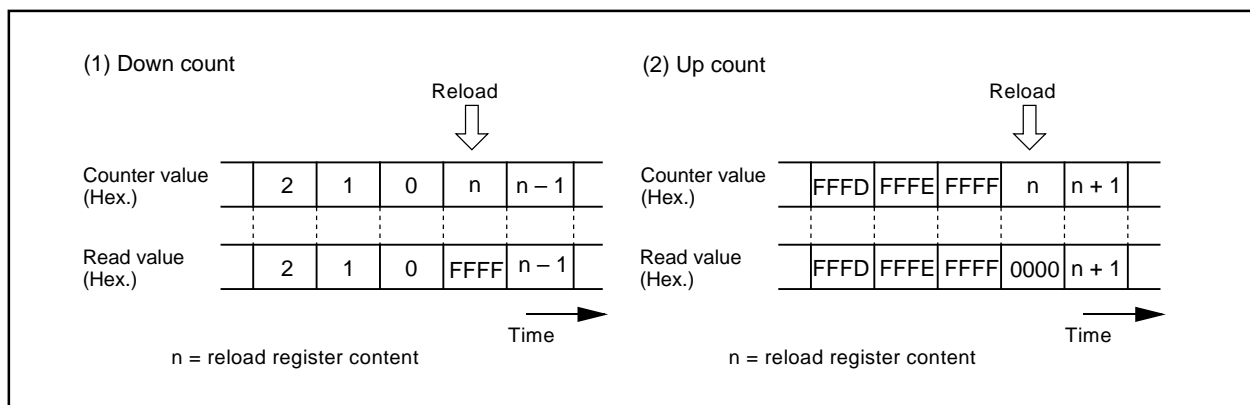


Figure 1.3.2. Reading timer Ai register

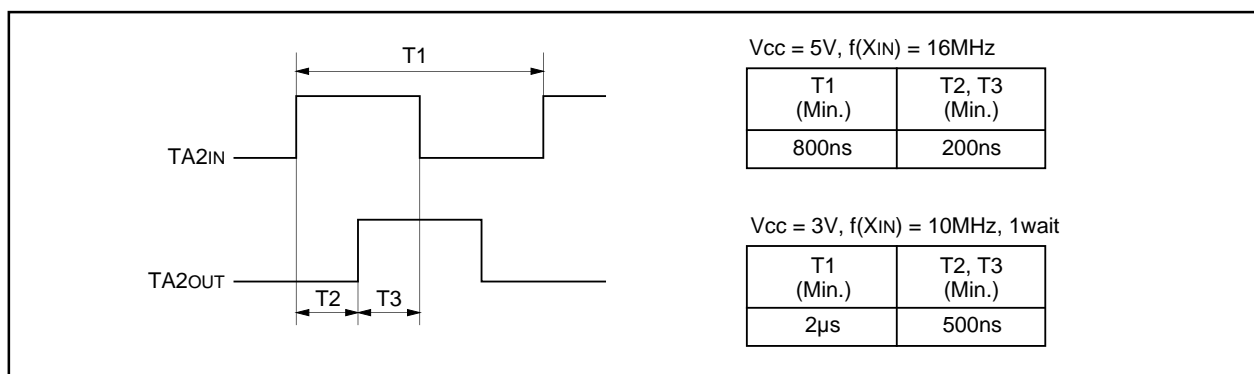


Figure 1.3.3. Standard of 2-phase pulses

1.3 Precautions for Timer A

1.3.3 Precautions for Timer A (one-shot timer mode)

1. After reset, the count start flag is set to "0". Set a value in the timer Ai register, then set the flag to "1".
2. Setting the count start flag to "0" while a count is in progress causes as follows:
 - The counter stops counting and a content of reload register is reloaded.
 - The TAIOUT pin outputs "L" level.
 - The timer Ai interrupt request bit becomes "1" after 1 cycle of BCLK.

Therefore, set the count start flag to "0" first and then execute two NOP instructions. After that set the timer Ai interrupt request bit to "0".

3. The output from the one-shot timer synchronizes with the count source generated internally. Therefore, when an external trigger has been selected, a delay of one cycle of the maximum count source occurs between the trigger input to the TAIIN pin and the one-shot timer output (Figure 1.3.4).
4. The timer Ai interrupt request bit goes to "1" if the timer's operation mode is set using any of the following procedures:
 - Selecting one-shot timer mode after reset.
 - Changing operation mode from timer mode to one-shot timer mode.
 - Changing operation mode from event counter mode to one-shot timer mode.
 Therefore, to use timer Ai interrupt (interrupt request bit), set timer Ai interrupt request bit to "0" after the above listed changes have been made.

5. If a trigger occurs while a count is in progress, after the counter performs one down count following the reoccurrence of a trigger, the reload register contents are reloaded, and the count continues. To generate a trigger while a count is in progress, generate the second trigger after an elapse longer than one cycle of the timer's count source after the previous trigger occurred.

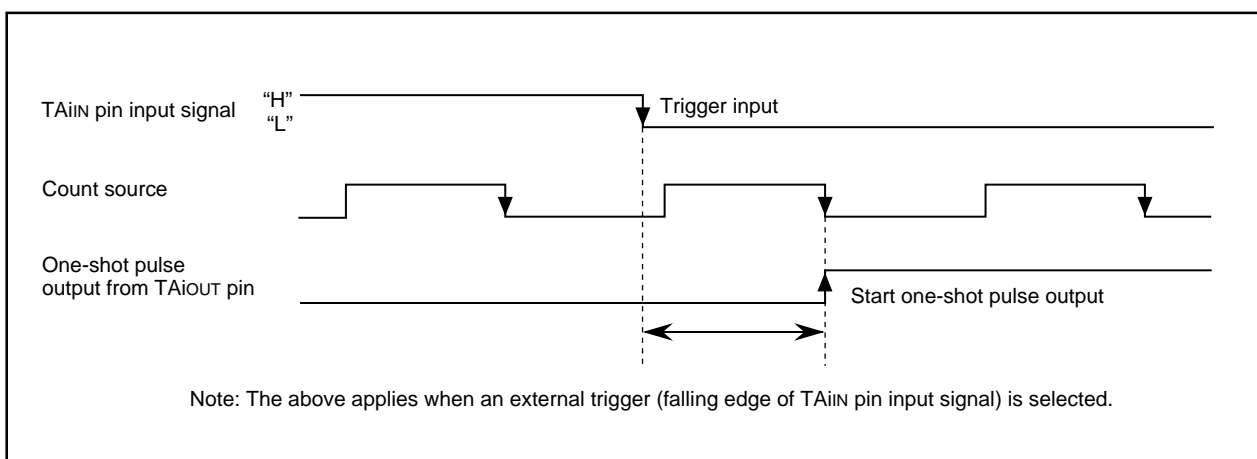


Figure1.3.4. One-shot timer delay

1.3 Precautions for Timer A

1.3.4 Precautions for Timer A (pulse width modulation mode)

1. After reset, the count start flag is set to "0". Set a value in the timer Ai register, then set the flag to "1".
2. The timer Ai interrupt request bit becomes "1" if setting operation mode of the timer in compliance with any of the following procedures:
 - Selecting PWM mode after reset.
 - Changing operation mode from timer mode to PWM mode.
 - Changing operation mode from event counter mode to PWM mode.Therefore, to use timer Ai interrupt (interrupt request bit), set timer Ai interrupt request bit to "0" after the above listed changes have been made.
3. Setting the count start flag to "0" while PWM pulses are being output causes the counter to stop counting. If the TAIOUT pin is outputting an "H" level in this instance, the output level goes to "L", and the timer Ai interrupt request bit goes to "1". If the TAIOUT pin is outputting an "L" level in this instance, the level does not change, and the timer Ai interrupt request bit does not becomes "1".

1.4 Precautions for Timer B

1.4 Precautions for Timer B

1.4.1 Precautions for Timer B (timer mode, event counter mode)

1. After reset, the count start flag is set to "0". Set a value in the timer Bi register, then set the flag to "1".
2. Reading the timer Bi register while a count is in progress allows reading, with arbitrary timing, the value of the counter. Reading the timer Bi register with the reload timing shown in Figure 1.4.1 gets "FFFF₁₆". Reading the timer Bi register after setting a value in the timer Bi register with a count halted but before the counter starts counting gets a proper value.

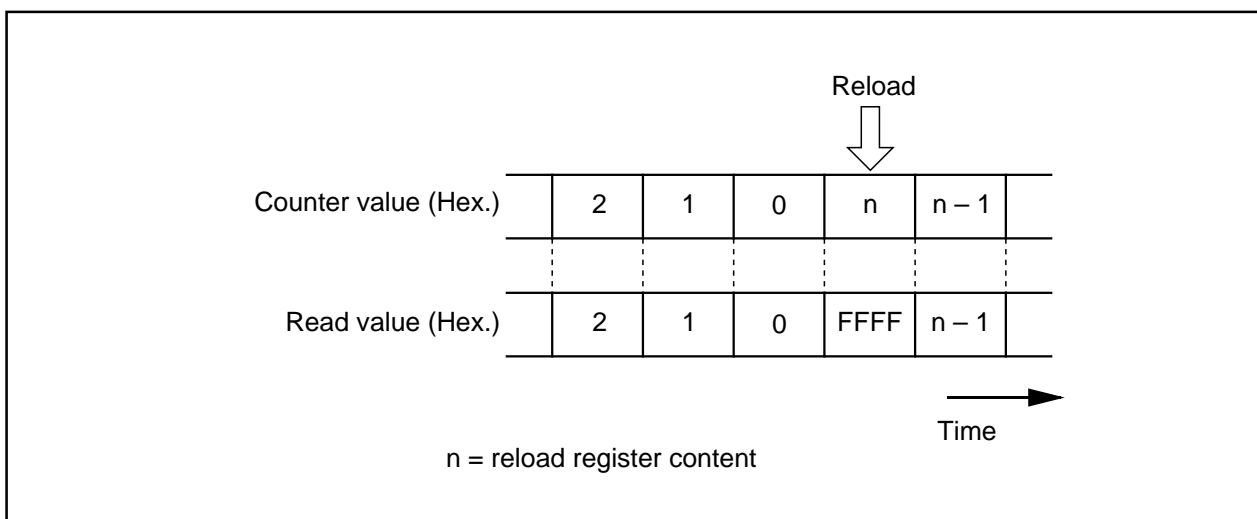


Figure 1.4.1. Reading timer Bi register

1.4 Precautions for Timer B

1.4.2 Precautions for Timer B (pulse period/pulse width measurement mode)

1. The timer Bi interrupt request bit goes to "1" when an effective edge of a measurement pulse is input or timer Bi is overflowed. The factor of interrupt request can be determined by use of the timer Bi overflow flag within the interrupt routine.
2. If the timer overflow occurs simultaneously with the input of a measurement pulse, and if the interrupt factor cannot be determined from the timer Bi overflow flag, connect the timers and count the number of overflows.
3. After reset, the timer Bi overflow flag is indeterminate. After setting the count start flag to "1", if a value is written to the timer Bi mode register after the count timing of count source, then the timer Bi overflow flag becomes "0".
4. Use the timer Bi interrupt request bit to detect only overflows. Use the timer Bi overflow flag only to determine the interrupt factor within the interrupt routine.
5. When the first effective edge is input after a count is started, an indeterminate value is transferred to the reload register. At this time, timer Bi interrupt request is not generated.
6. The value of the counter is indeterminate at the beginning of a count. Therefore, the timer Bi overflow flag may go to "1" and timer Bi interrupt request may be generated during the interval between a count start and an effective edge input.
7. If changing the measurement mode select bits are set after a count is started, the timer Bi interrupt request bit goes to "1". Note that the timer Bi interrupt request bit does not change if the same value as before is written to the measurement mode select bits.
8. If the input signal to the TBiIN pin is affected by noise, precise measurement may not be performed in some cases. It is recommended to see that measurements fall within a specific range by use of software.
9. For pulse width measurement, pulse widths are successively measured. Use software to check whether the measurement result is an "H" level width or an "L" level width.

1.5 Precautions for Clock-Synchronous Serial I/O

1.5 Precautions for Serial I/O (in clock-synchronous serial I/O)

1.5.1 Transmission/reception

With an external clock selected, and choosing the $\overline{\text{RTSi}}$ function, the output level of the $\overline{\text{RTSi}}$ pin goes to “L” when the data-receivable status becomes ready, which informs the transmission side that the reception has become ready. The output level of the $\overline{\text{RTSi}}$ pin goes to “H” when reception starts. So if the $\overline{\text{RTSi}}$ pin is connected to the $\overline{\text{CTSi}}$ pin on the transmission side, the circuit can transmission and reception data with consistent timing. With the internal clock, the $\overline{\text{RTSi}}$ function has no effect. Figure 1.5.1 shows an example of wiring.

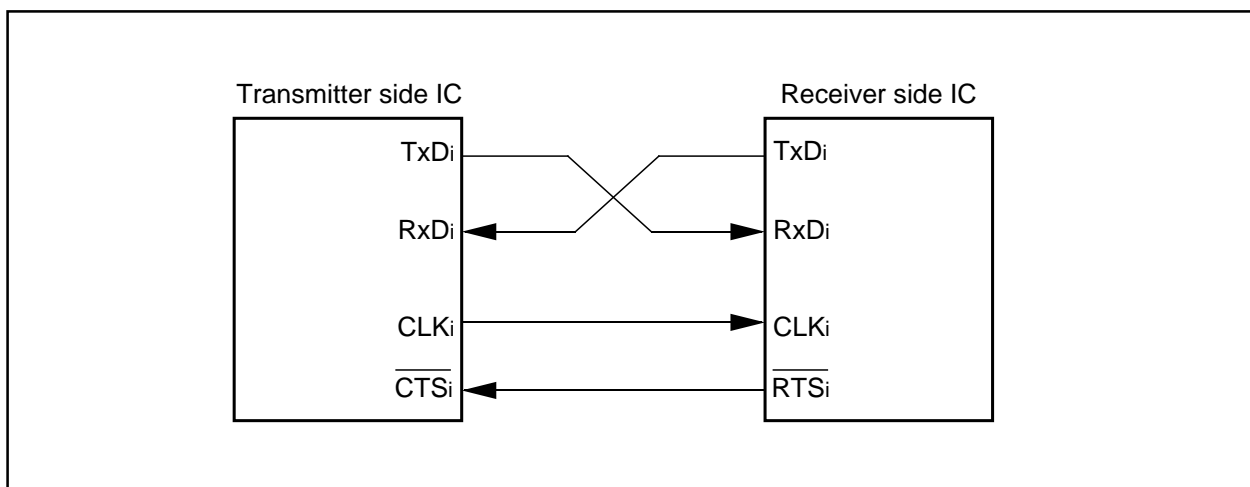


Figure 1.5.1. Example of wiring

1.5 Precautions for Clock-Synchronous Serial I/O

1.5.2 Transmission

With an external clock selected, perform the following set-up procedure with the CLKi pin input level = "H" if the CLK polarity select bit = "0" or with the CLKi pin input level = "L" if the CLK polarity select bit = "1":

- (1) Set the transmit enable bit (to "1")
- (2) Write transmission data to the UARTi transmit buffer register
- (3) "L" level input to the $\overline{\text{CTS}}_i$ pin (when the $\overline{\text{CTS}}$ function is selected)

1.5.3 Reception

1. In operating the clock-synchronous serial I/O, operating a transmitter generates a shift clock. Fix settings for transmission even when using the device only for reception. Dummy data is output to the outside from the TxDi pin (transmission pin) when receiving data.
2. With the internal clock selected, setting the transmit enable bit to "1" (transmission-enabled status) and setting dummy data in the UARTi transmission buffer register generates a shift clock. With the external clock selected, a shift clock is generated when the transmit enable bit is set to "1", dummy data is set in the UARTi transmit buffer register, and the external clock is input to the CLKi pin.
3. In receiving data in succession, an overrun error occurs when the next reception data is made ready in the UARTi receive register with the receive complete flag set to "1" (before the content of the UARTi receive buffer register is read), and overrun error flag is set to "1". In this instance, the next data is written to the UARTi receive buffer register, so handle with this problem by writing programs on transmission side and reception side so that the previous data is transmitted again. If an overrun error occurs, the UARTi receive interrupt request bit does not change.
4. To receive data in succession, set dummy data in the lower-order byte of the UARTi transmit buffer register every time reception is made.
5. With an external clock selected, perform the following set-up procedure with the CLKi pin input level = "H" if the CLK polarity select bit = "0" or with the CLKi pin input level = "L" if the CLK polarity select bit = "1":
 - (1) Set receive enable bit (to "1")
 - (2) Set transmit enable bit (to "1")
 - (3) Write dummy data to the UARTi transmit buffer register
6. Output from the $\overline{\text{RTS}}_i$ pin goes to "L" level as soon as the receive enable bit is set to "1". This is not related to the content of the transmit buffer empty flag or the content of the transmit enable bit. Output from the $\overline{\text{RTS}}_i$ pin goes to "H" level when reception starts, and goes to "L" level when reception is completed. This is not related to the content of the transmit buffer empty flag or the content of the receive complete flag.

1.6 Precautions for A-D Converter

1.6 Precautions for A-D Converter

1. Write to each bit (except bit 6) of A-D control register 0, to each bit of A-D control register 1, and to bit 0 of A-D control register 2 when A-D conversion is stopped (before a trigger occurs). In particular, when the Vref connection bit is changed from 0 to 1, start A-D conversion after an elapse of 1 μ s or longer.
2. To reduce conversion error due to noise, connect a voltage to the AVcc pin and to the Vref pin from an independent source. It is recommended to connect a capacitor between the AVss pin and the AVcc pin, between the AVss pin and the Vref pin, and between the AVss pin and the analog input pin (ANi). Figure 1.6.1 shows the an example of connecting the capacitors to these pins.

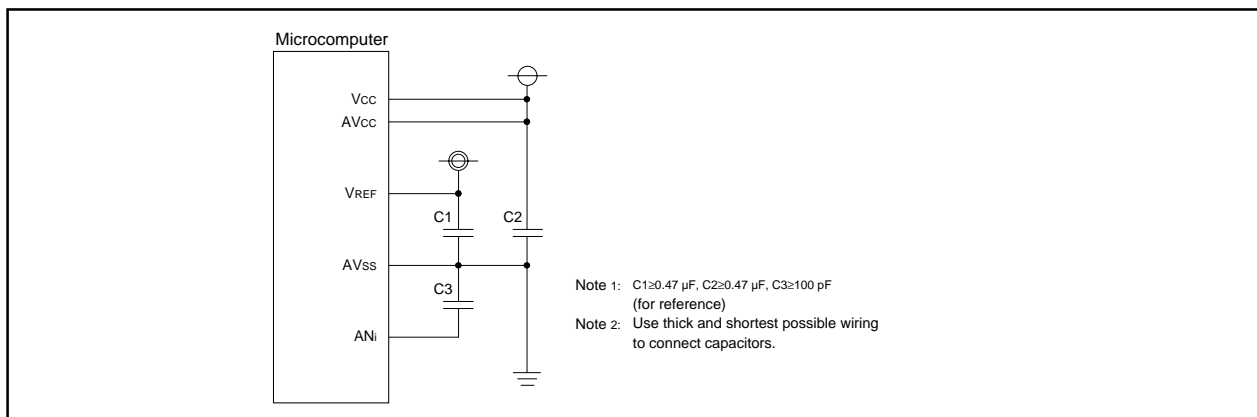


Figure 1.6.1. Use of capacitors to reduce noise

3. Set the direction register of the following ports to input: the port corresponding to a pin to be used as an analog input pin and external trigger input pin (P97).
4. In using a key-input interrupt, none of the 4 pins (AN4 through AN7) can be used as an A-D conversion port (if the A-D input voltage goes to "L" level, a key-input interrupt occurs).
5. Divide the f_{AD} if $f(X_{IN})$ exceeds 10MHz, and make AD operation clock frequency (ϕ_{AD}) equal to or lower than 10MHz. And divide the f_{AD} if VCC is 2.7V to 4.0V, and make AD operation clock frequency (ϕ_{AD}) equal to or lower than $f_{AD}/2$, selected 8-bit mode and without sample and hold function.
6. Confirm that A-D conversion is complete before reading the A-D register. (Note: When A-D conversion interrupt request bit is set, it shows that A-D conversion is completed.)
7. A case without sample and hold function, set the AD operation clock frequency (ϕ_{AD}) into 250 kHz or more. A case with sample & hold function, set the AD operation clock frequency (ϕ_{AD}) into 1MHz or more.

1.7 Precautions for Power Control

1.7 Precautions for Power Control

1. The processor does not switch to stop mode when the $\overline{\text{NMI}}$ pin is at “L” level.
2. When returning from stop mode by hardware reset, $\overline{\text{RESET}}$ pin must be set to “L” level until main clock oscillation is stabilized.
3. When switching to either wait mode or stop mode, instructions occupying four bytes either from the WAIT instruction or from the instruction that sets the all clock stop control bit to “1” within the instruction queue are prefetched and then the program stops. So put at least four NOPs in succession either to the WAIT instruction or to the instruction that sets the all clock stop control bit to “1”.
4. Before the count source for BCLK can be changed from XIN to XCIN or vice versa, the clock to which the count source is going to be switched must be oscillating stably. Allow a wait time in software for the oscillation to stabilize before switching over the clock.

5. Suggestions to reduce power consumption

(a) Ports

The processor retains the state of each programmable I/O port even when it goes to wait mode or to stop mode. A current flows in active I/O ports. A pass current flows in input ports that float. When entering wait mode or stop mode, set non-used ports to input and stabilize the potential.

(b) A-D converter

A current always flows in the VREF pin. When entering wait mode or stop mode, set the Vref connection bit to “0” so that no current flows into the VREF pin.

(c) Stopping peripheral functions

In wait mode, stop non-used peripheral functions using the WAIT peripheral function clock stop bit. However, peripheral function clock fc32 does not stop so that the peripherals using fc32 do not contribute to the power saving. When the MCU running in low-speed or low power dissipation mode, do not enter WAIT mode with this bit set to “1”.

(d) Switching the oscillation-driving capacity

Set the driving capacity to “LOW” when oscillation is stable.

(e) External clock

When using an external clock input for the CPU clock, set the main clock stop bit to “1”. Setting the main clock stop bit to “1” causes the XOUT pin not to operate and the power consumption goes down (when using an external clock input, the clock signal is input regardless of the content of the main clock stop bit).

1.8 Precautions for External Buses

1.8 Precautions for External Bus

1. The external ROM version can operate only in the microprocessor mode, so be sure to perform the following:
 - Connect the CNVss pin to Vcc.
2. When the CNVss pin is reset at "H" level, the contents of internal ROM cannot be read out.

MSC TECHNICAL NEWS

No.M16C-09-9705

Note on using the A-D converter of the M16C/60 series MCU

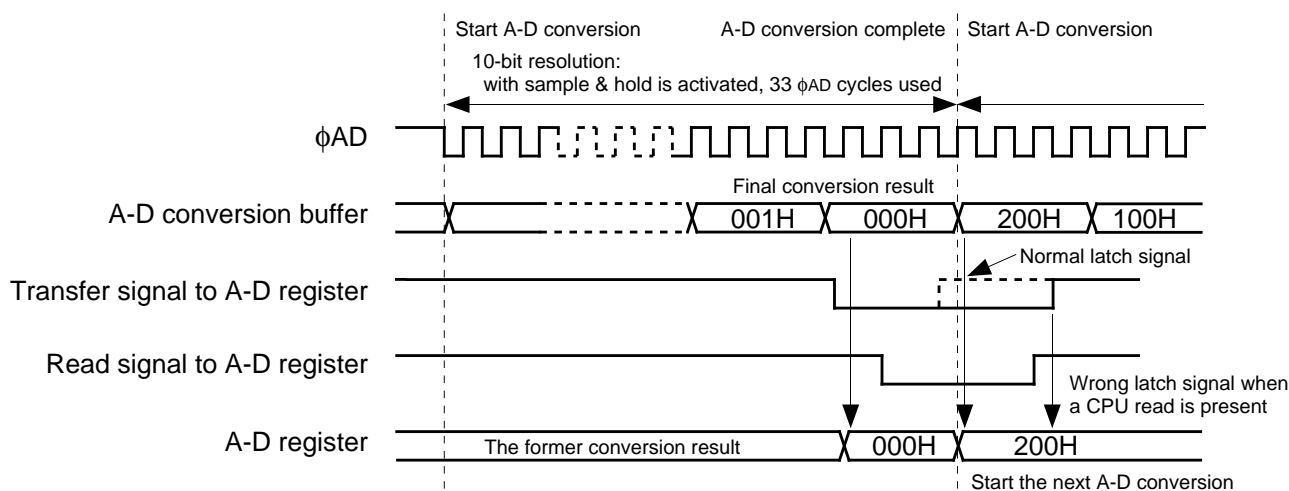
1. Related devices

M16C/60 series

2. Symptoms

After A-D conversion is complete, if the CPU reads the A-D register at the same time as the A-D conversion result is being saved to A-D register, wrong A-D conversion value is saved into the A-D register. This happens when the internal CPU clock is selected from divided main clock or sub-clock.

(When connected an A-D input port and GND)



Normally, A-D conversion value is saved at the rising edge (dashed rising edge) of the latch signal. However, when the CPU is doing a read to A-D register at this time, the A-D register latch signal is delayed, and wrong value is stored at A-D conversion register.

3. Precaution

(1) When using the one-shot or single sweep mode

Confirm that A-D conversion is complete before reading the A-D register.

(Note: When A-D conversion interrupt request bit is set, it shows that A-D conversion is completed.)

(2) When using the repeat mode or repeat sweep mode 0 or 1

Use the undivided main clock as the internal CPU clock.

MESC TECHNICAL NEWS

No.M16C-11-9710

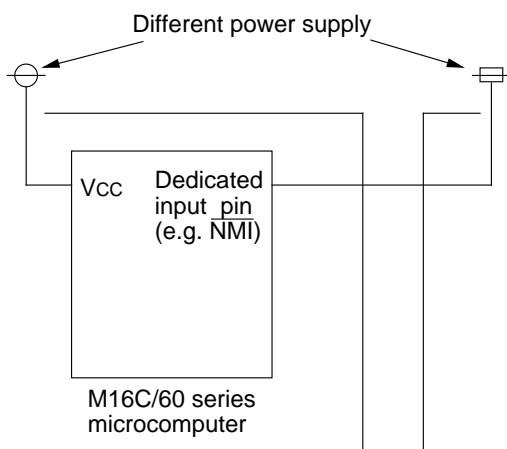
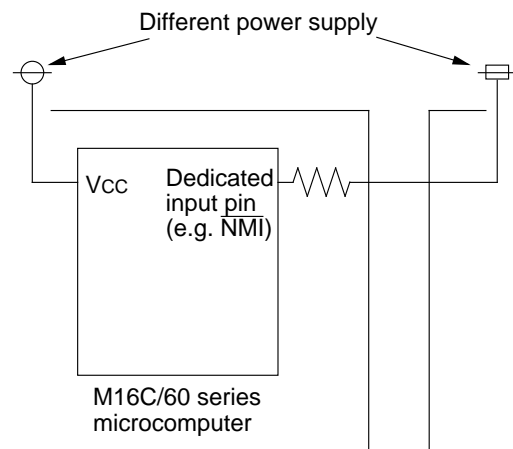
Note on dedicated input pin of the M16C/60 series MCU

1. Related devices

M16C/60 series

2. Note on dedicated input pin

When different power supplied to the system as shown in figure 1, and input voltage of unused dedicated input pin is larger than voltage of VCC pin, do not connect dedicated input pin and power supply directly. Connect to VCC via resistor (approximately 1kohm) as shown in figure 2. This note is also applicable when V_{INPUT} exceeds V_{CC} during power-up.

**Figure 1. Circuit diagram****Figure 2. Improved circuit diagram**

* The resistor is not necessary when VCC pin voltage is same or larger than dedicated input pin voltage.

3. Cause

When dedicated input pin voltage is larger than VCC pin voltage, latch up occurs.

MESC TECHNICAL NEWS

No. M16C-13-9802

Supplemental Description of DMAC for the M16C/60, M16C/61 and M16C/62 Group MCUs

1. Related devices

M16C/60, M16C/61 and M16C/62 groups

2. DMA enable bit

The DMA enable bit is bit 3 of both DMA0 and DMA1 control registers.

When the DMA enable bit is set to "1" the DMAC is in an active state and the following occurs:

- a. The value of whichever of the source or destination pointer that is set up as the forward pointer is reloaded into the forward address pointer.
- b. The value in the transfer counter reload register is reloaded into the transfer counter.

Therefore, the DMAC will start from the initial conditions once again if the DMA enable bit is set to "1" while in the active state.

3. DMA request bit

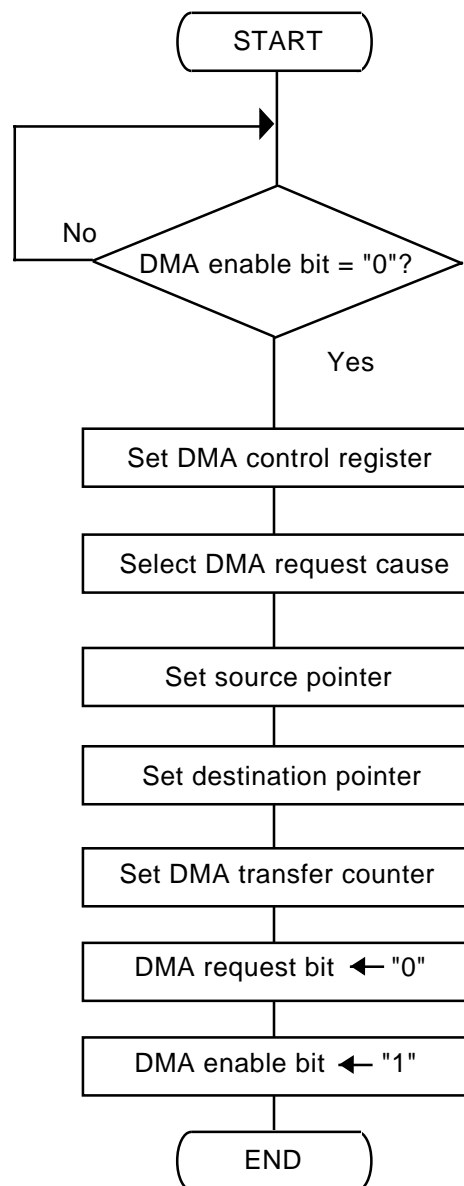
The DMA request bit is bit 2 of both DMA0 and DMA1 control registers.

Regardless of the DMAC status (enable bit set or clear), the request bit is set to "1" when a request signal for a DMA transfer occurs, based on the DMA request factor. The bit is cleared to "0" when data transfer begins. Further, the user can clear ("0") the DMA request bit but not set it.

It is possible that the DMA request bit may become "1" due to the DMA request cause select bits being changed. Therefore the DMA request bit should be cleared ("0") after changing the DMA request cause select bits.

If DMAC is in the active state (enable bit set) when the request bit becomes "1", the data transfer begins immediately. That in turn immediately causes the DMA request bit to be cleared ("0"). Therefore, to best judge the state of the DMAC, the DMA enable bit should be read instead of the request bit.

4. Initialization of DMA-related registers



MESC TECHNICAL NEWS

No. M16C-14-9805

Precautions Regarding Writing to M16C/60, M16C/61, M16C/62 and M16C/63 Group MCUs Interrupt Control Registers

1. Related devices

M16C/60, M16C/61, M16C/62 and M16C/63 groups

With the M16C/60 series MCU, setting the interrupt priority level and clearing the interrupt request bit in the interrupt control registers should be done with interrupt disabled.

Executing these operations while interrupt is enabled may result in unintended CPU operations.

2. Symptom

Changing the Interrupt priority LeVeL select bit (ILVL) and clearing the Interrupt Request bit (IR) in the Interrupt Control Registers (ICRs) while the Interrupt enable FLAG (I-FLAG) is "1" may result in unintended operations, such as BRK and other interrupts being generated.

3. Considerations for writing new program

It is recommended that the interrupts must be disabled by clearing the I-FLAG, before setting ILVL or clearing the IR bit in the ICRs.

In order to avoid the influence of the CPU pipeline, a certain number of instructions (eg. NOP) should be inserted between writing to the ICRs and setting the I-FLAG.

The number of instructions (NOPs) required is shown in TABLE.

4. Conditions to be checked for program already written

Please confirm that at least one condition is met for both actions listed below. If any one of the conditions is met, the symptom will not occur.

(1) When changing ILVL

- I-FLAG is "0". (Interrupt disabled) (*Note)
- The processor interrupt priority level (IPL) in the flag register is "7".
- The ILVL changes from a lower level than IPL to a higher level.
- The ILVL before and after the change is lower than IPL.
- The ILVL before and after the change is higher than IPL.
- It is obvious that the corresponding interrupt will not occur while changing the ILVL.

(2) When clearing the IR

- I-FLAG is "0". (Interrupt disabled) (*Note)
- The IPL in the flag register is "7".
- The ILVL during the operation is "0".
- The ILVL is lower than IPL.
- It is obvious that the corresponding interrupt will not occur while clearing the IR.

Note: In order to avoid the influence of the CPU pipeline, a certain number of instructions (eg. NOP) should be inserted between writing to ICRs and setting the I-FLAG.

The number of instructions required is showed in the TABLE.

| | When not using HOLD function | When using HOLD function |
|-----------|---|--------------------------------|
| Example 1 | Two NOP instructions required | Four NOP instructions required |
| Example 2 | No NOP instruction required (because there is dummy read) | |
| Example 3 | No NOP instruction required | |

5. Program examples

The program examples are described as follow:

(1) For assembler

Example 1:

```
INT_SWITCH1:
    FCLR    I                ; Disable interrupts.
    AND.B  #00h, 0055h ; Clear TA0IC int. priority level and int. request bit.
    NOP
    NOP                ; Four NOP instructions are required when using HOLD function.
    FSET    I                ; Enable interrupts.
```

Example 2:

```
INT_SWITCH2:
    FCLR    I                ; Disable interrupts.
    AND.B  #00h, 0055h ; Clear TA0IC int. priority level and int. request bit.
    MOV.W  MEM, R0        ; Dummy read.
    FSET    I                ; Enable interrupts.
```

Example 3:

```
INT_SWITCH3:
    PUSHC  FLG            ; Push Flag register onto stack
    FCLR    I                ; Disable interrupts.
    AND.B  #00h, 0055h ; Clear TA0IC int. priority level and int. request bit.
    POPC   FLG            ; Enable interrupts.
```

The reason why two NOP instructions (four when using the HOLD function) or dummy read are inserted before FSET I in Examples 1 and 2 is to prevent the interrupt enable flag I from being set before the interrupt control register is rewritten due to effects of the instruction queue.

(2) For C language

```
#pragma ASM
INT_SWITCH:
    FCLR    I
#pragma ENDASM
    TA0IC  & =00 ; /* Clear TA0IC int. priority level and int. request bit. */
#pragma ASM
    NOP
    NOP                ; Four NOP instructions are required when using HOLD function.
    FSET    I
#pragma ENDASM
```

MESC TECHNICAL NEWS No.M16C-17-9902

M16C/60 Group, M16C/61 Group, M16C/62 Group Precautions For Power Control State Transitions

1. Related devices

M16C/60 group, M16C/61 group, M16C/62 group

2. Precautions

Power control state transition is shown on the next page.

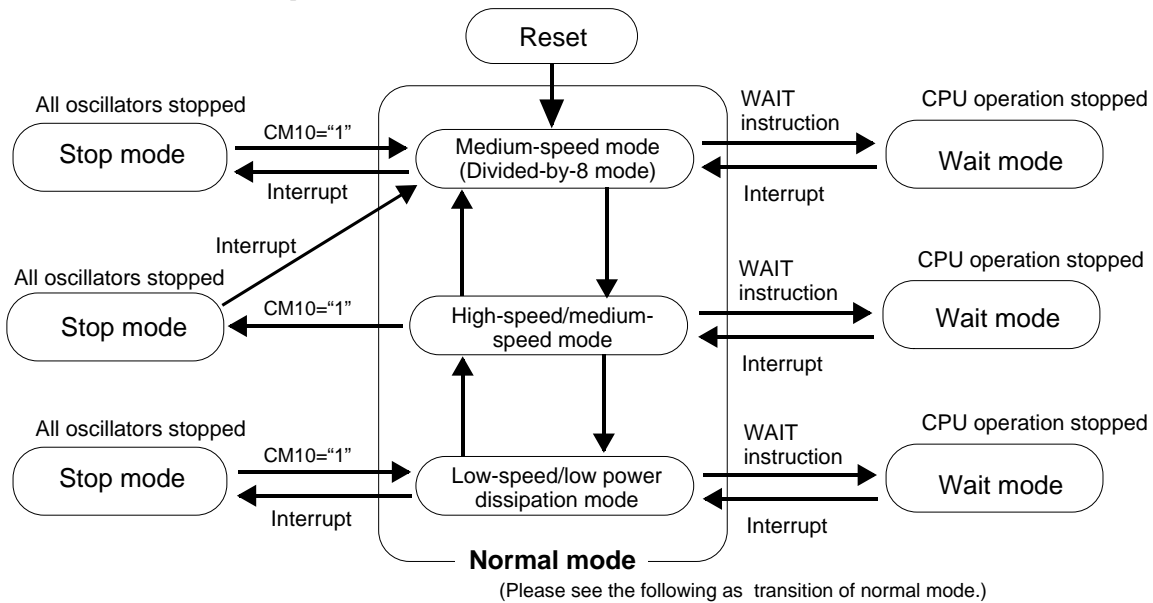
Please change modes according to a directions of arrows.

When count source of BCLK is changed from clock A to clock B (XIN to XCIN or XCIN to XIN), clock B needs to be stable before changing.

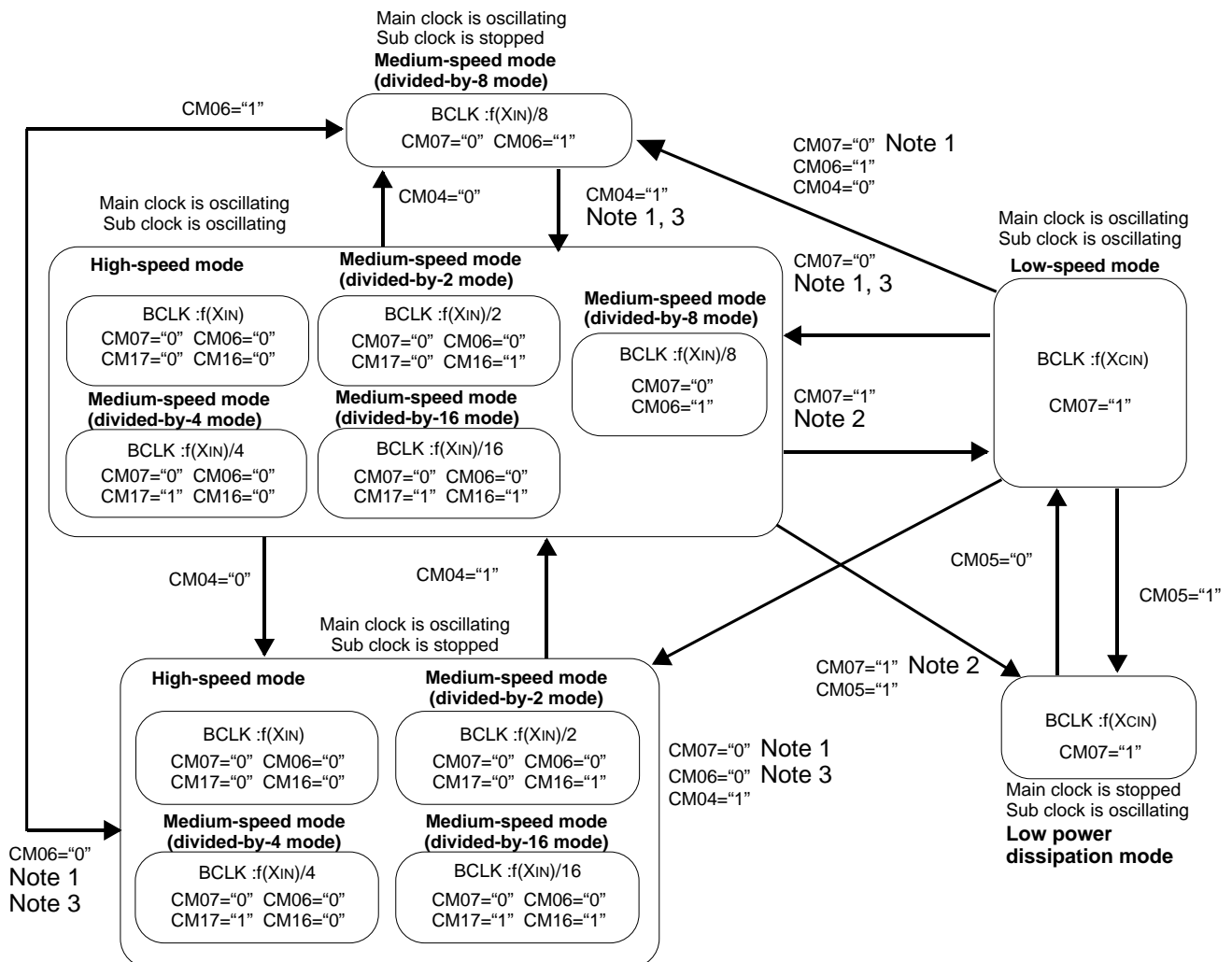
Please wait to change modes until after oscillation has stabilized.

The delay time is depends on the oscillator. Please refer to the oscillator manufacture's specifications.

Transition of stop mode, wait mode



Transition of normal mode



Note 1: Switch clocks after oscillation of main clock is fully stable.
 Note 2: Switch clocks after oscillation of sub clock is fully stable.
 Note 3: Change CM17 and CM16 before CM06.
 Note 4: Please change according to a direction of an arrow.

MESC TECHNICAL NEWS No.M16C-19-9903

MESC TECHNICAL NEWS 'No.M16C-16-9902' replace

MESC TECHNICAL NEWS 'No.M16C-16-9902' has an error, so we will correct.
Please replace old Technical News 'No.M16C-16-9902' to corrected Technical News 'M16C/60,
M16C/61, M16C/62 Group Precautions for Setting Pull-up Resistors'.

[Attached]

Corrected Technical News 'No.M16C-19-9903'
'M16C/60, M16C/61, M16C/62 Group Precautions for Setting Pull-up Resistors' 1 page

MESC TECHNICAL NEWS

No. M16C-19-9903

M16C/60, M16C/61, M16C/62 Group Precautions for Setting Pull-up Resistors

1. Related devices

M16C/60 group, M16C/61 group, M16C/62 group

2. Precautions

Ports P0 to P10 can be set to apply a pull-up resistor by using the pull-up control registers.

(1) M16C/60 Group, M16C/61 Group

In Memory expansion mode or Microprocessor mode, the settings of pull-up control registers for ports P0 to P5 are invalid.

In Memory expansion mode or Microprocessor mode, ports P0, P1, P31 to P37 and P4 can be used as input ports, but internal pull-up resistors can not be connected.

(2) M16C/62 Group

In Memory expansion mode or Microprocessor mode, the settings of pull-up control registers for P0 to P3, P40 to P43 and P5 are invalid.

In Memory expansion mode or Microprocessor mode, ports P0, P1, P31 to P37 and P40 to P43 can be used as input ports, but internal pull-up resistors can not be connected.

(In Memory expansion mode or Microprocessor mode, P44 to P47 can be used as general input ports, and pull-up control register can be used to connect the internal pull-up resistors.)

MESOC TECHNICAL NEWS No. M16C-25-9905

M16C/60 , M16C/20 Series

Precautions for Wait and Stop modes

1. Related devices

M16C/60 Series , M16C/20 Series

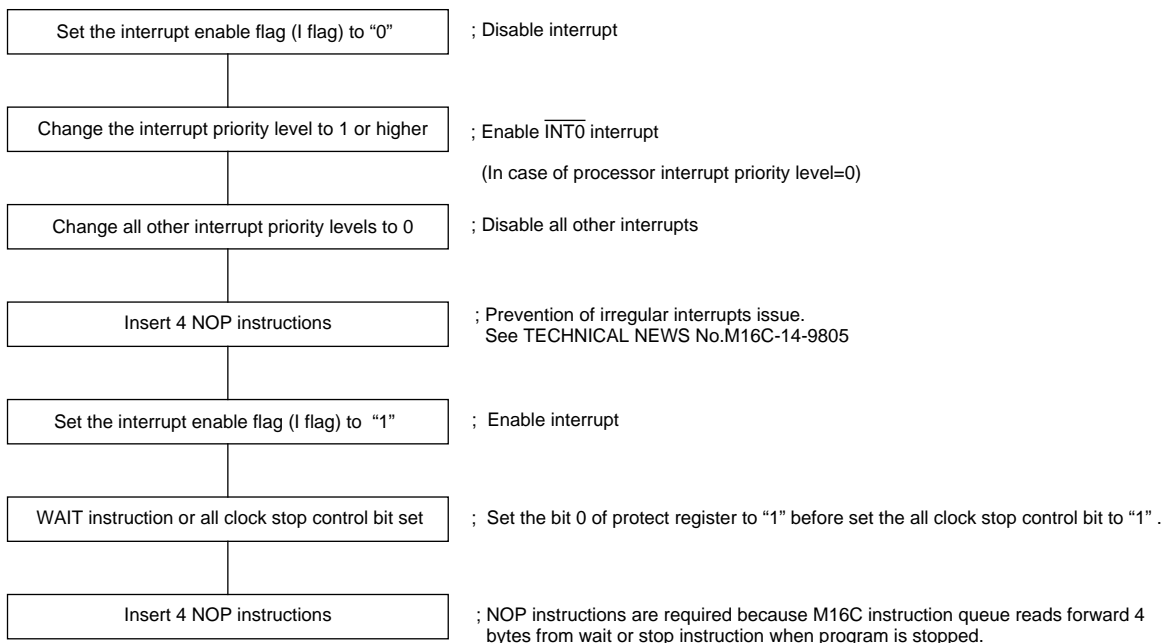
2. Precautions

The M16C has both WAIT and STOP modes. These modes can be used to reduce power consumption when the CPU is not required to perform any work. To return to normal operating mode after issuing a WAIT instruction or setting the all clock stop control bit, perform a hardware reset or use an interrupt. The interrupts for canceling the WAIT and STOP modes must be enabled before entering either mode. The priority level of the interrupts not used for these modes should be set to 0 before switching into the WAIT or STOP modes. Also, if only hardware reset or $\overline{\text{NMI}}$ interrupts are used for canceling the WAIT or STOP modes, all interrupt priority level should be set to 0 before switching into the WAIT or STOP mode.

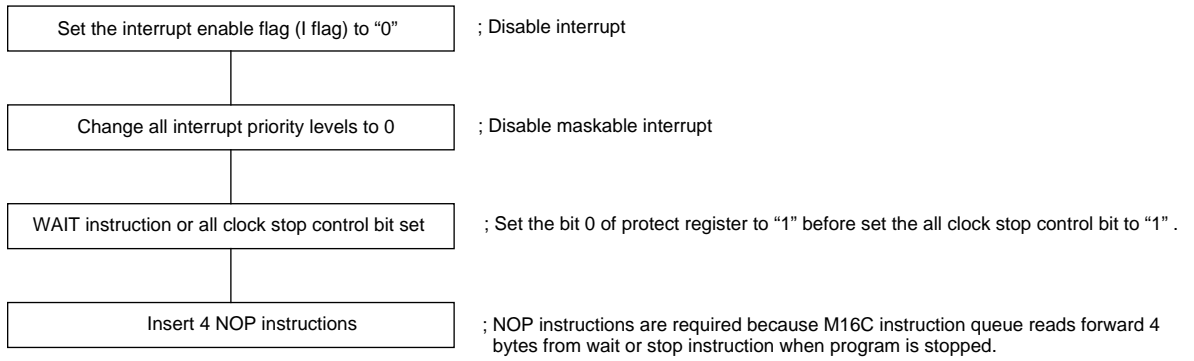
3. Examples

3.1 Use the following algorithm to enter the WAIT or STOP modes when an interrupt is used to cancel either mode.

- **Hardware reset, $\overline{\text{NMI}}$ interrupt, and $\overline{\text{INT0}}$ interrupt is used to cancel either mode**



3.2 When using only hardware reset or $\overline{\text{NMI}}$ interrupt to cancel the STOP or WAIT modes, use the following algorithm to enter the STOP or WAIT modes.



MESOC TECHNICAL NEWS No. M16C-26-9905

M16C/61 , M16C/62 Group Precautions for UART2

1. Related devices

M16C/61 Group, M16C/62 Group

2. Precautions

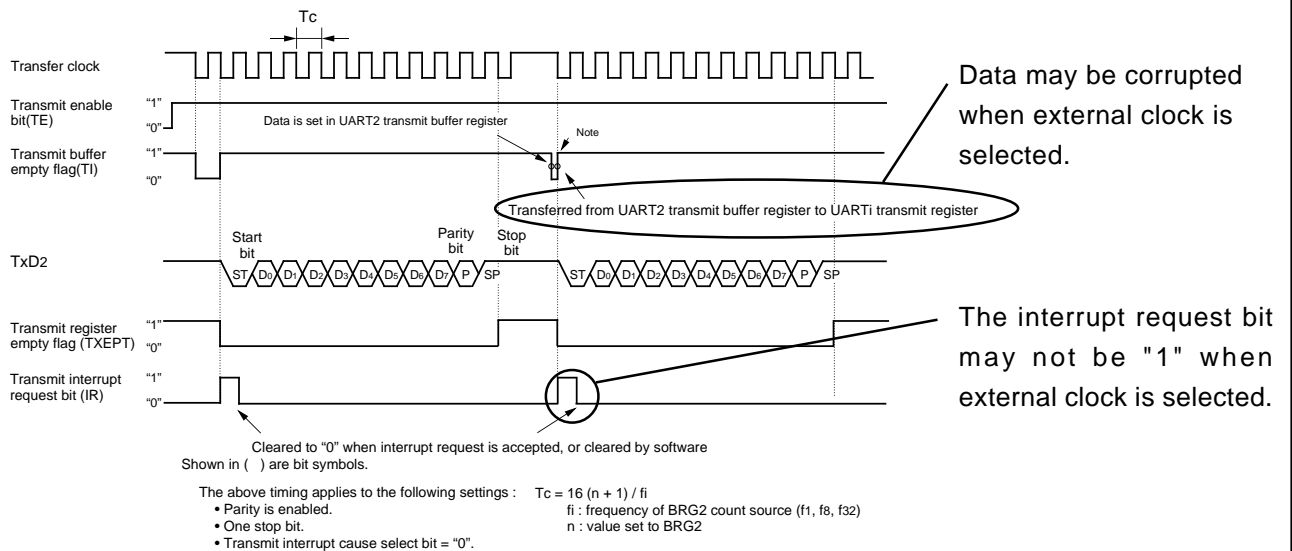
When using UART2 in clock asynchronous serial I/O (UART) mode choose internal clock. If UART2 in clock asynchronous mode is used with external clock, then one of the following may occur;

2.1 The interrupt may not be issued at the end of data transmission when the hardware transfers the data from the transmit buffer register to the transmit register.

2.2 Data may be corrupted when the hardware transfers the data from the transmit buffer register to the transmit register.

This precaution only applies to the UART2 asynchronous serial I/O mode and does not apply to UART0 or UART1. It does not apply to any UART when used in the synchronous clocked serial I/O mode.

Example of transmit with UART mode, Transfer data 8 bits long.



Note: The transmit is started with overflow timing of BRG after having written in a value at the transmit buffer in the above timing.

MESC TECHNICAL NEWS

No. M16C-32-9908

M16C/60 Series

Precautions for Address Match Interrupt

1. Related devices

M16C/60 Series

2. Precautions

When using the address match interrupt, please observe the following usage conditions.

- (1) Address match interrupt for internal address.
- (2) Address match interrupt for external address and 16-bit bus.

When external address and 8-bit bus, you can not use the address match interrupt for external address.

MESC TECHNICAL NEWS

No. M16C-39-9911

M16C Family

Cautions for “Event counter mode” with Timer A

1. Affected devices

- M16C/80 Group, M16C/60 Group, M16C/61 Group, M16C/62 Group (Included 3V version)
- M16C/62A Group (Included 3V version), M16C/6N Group, M16C/6K Group, M16C/6V Group
- M16C/6H Group, M16C/21 Group, M16C/24 Group

2. Cautions

In the case of using “Event counter mode” as “Free-Run type” for timer A, the timer register contents may be unknown when counting begins. If the timer register is set before counting has started, then the starting value will be unknown.

This issue will occur only for the “Event counter mode” operating as “Free-Run type”. The value of the timer register will not be unknown during counting.

3. Countermeasure

(1) In the case where the up/down count will not be changed.

Enable the “Reload” function and write to the timer register before counting begins. Rewrite the value to the timer register immediately after counting has started.

If counting up, rewrite “0000₁₆” to the timer register.

If counting down, rewrite “FFFF₁₆” to the timer register.

This will cause the same operation as “Free-Run type” mode.

(2) In the case where the up/down count has changed.

First set to “Reload type” operation. Once the first counting pulse has occurred, the timer may be changed to “Free-Run type”.

MESC TECHNICAL NEWS No. M16C-49-0004

M16C/80 Series, M16C/60 Series

Cautions for Using Memory Expansion Mode or Microprocessor Mode

1. Affected devices

- M16C/80 Series
- M16C/60 Series

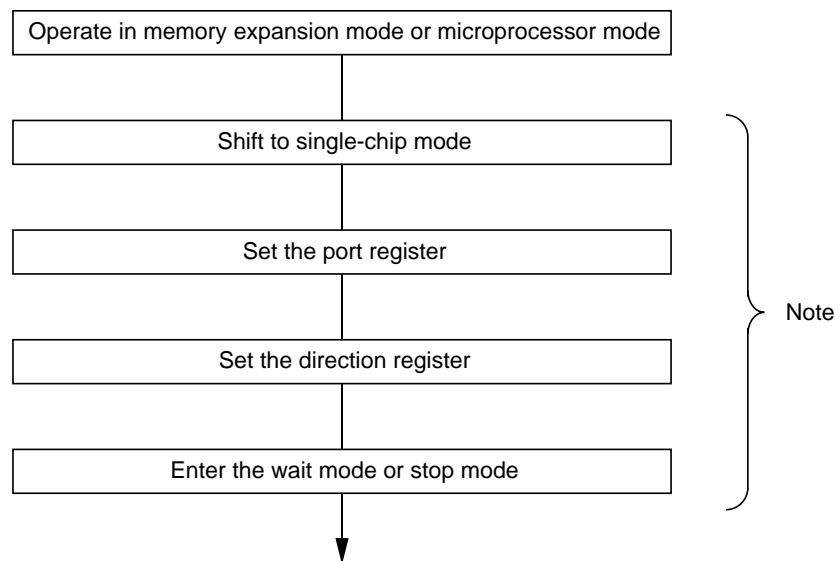
2. Cautions

When the MCU enters wait mode while operating in memory expansion mode or microprocessor mode, a pin functioning as part of the address or data bus retains its state on the bus before wait mode is entered. Shift to single-chip mode and output an arbitrary value in order to reduce current consumption. By shifting to single-chip mode, a pin which was functioning as part of the bus becomes a general-purpose port and can output an arbitrary value. Set the port registers and direction registers after shifting to single-chip mode (this implies that any control pins (CS, WR, RD, etc..) being used for access of an external device be changed as well).

If the port registers and direction registers are set while in memory expansion mode or microprocessor mode, the operation will be ignored.

This is similar when entering stop mode.

Setting procedure is following.



Note: This program does not work in external area. Transfer a program to internal RAM and work on internal RAM.

MESOC TECHNICAL NEWS No. M16C-55-0006

M16C Family

Cautions Using Data Registers that Include Write Only Bits

1. Affected devices

- M16C Family

2. Cautions

The registers shown in the table on the following page contain bits that will result in unknown data when read.

If performing a read-modify-write sequence of instructions to a register with write only bits, please reset the write only bits to their previous values before writing back to the register.

If your software accesses these registers frequently, please use a temporary RAM area to change the value, and then transfer it to the register.

Figure 1 shows an example of a register structure. If you execute a 'Read Modify Write' instruction like BSET, BCLR, AND or OR, the values of bits 5-7 may change. (Please see Figure 2)

'Table 10' show instruction table for Read Modify Write.

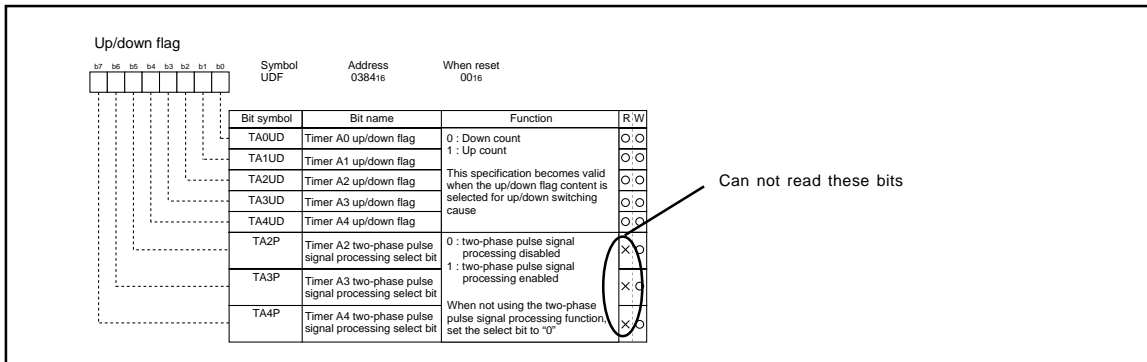


Figure 1. Example of a register structure

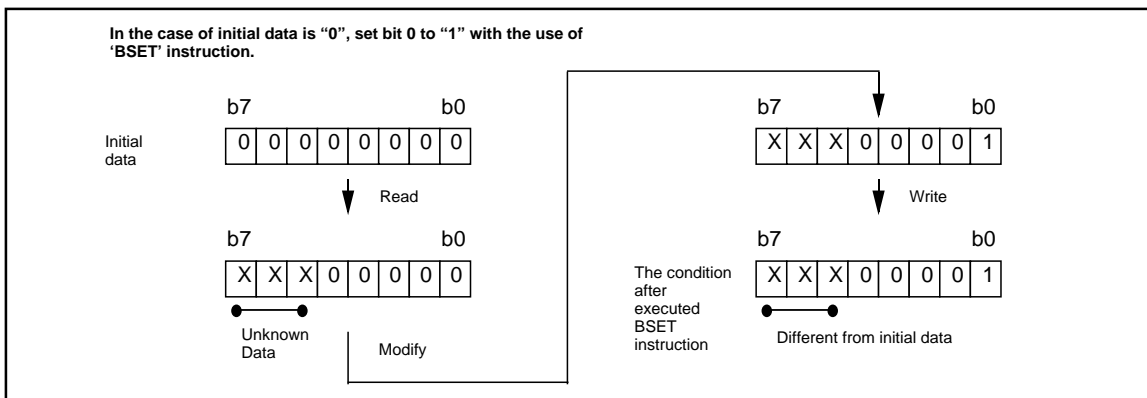


Figure 2. Example of a register change

Table 1. Affected register (M16C/80 group)

| Register name | Symbol | Address |
|--|--------|---|
| UART4 bit rate generator | U4BRG | 02F9 ₁₆ |
| UART4 transmit buffer register | U4TB | 02FB ₁₆ , 02FA ₁₆ |
| Dead time timer | DTT | 030C ₁₆ |
| Timer B2 interrupt occurrences frequency set counter | ICTB2 | 030D ₁₆ |
| UART3 bit rate generator | U3BRG | 0329 ₁₆ |
| UART3 transmit buffer register | U3TB | 032B ₁₆ , 032A ₁₆ |
| UART2 bit rate generator | U2BRG | 0339 ₁₆ |
| UART2 transmit buffer register | U2TB | 033B ₁₆ , 033A ₁₆ |
| Up/down flag | UDF | 0344 ₁₆ |
| Timer A0 register (Note) | TA0 | 0347 ₁₆ , 0346 ₁₆ |
| Timer A1 register (Note) | TA1 | 0349 ₁₆ , 0348 ₁₆ |
| Timer A2 register (Note) | TA2 | 034B ₁₆ , 034A ₁₆ |
| Timer A3 register (Note) | TA3 | 034D ₁₆ , 034C ₁₆ |
| Timer A4 register (Note) | TA4 | 034F ₁₆ , 034E ₁₆ |
| UART0 bit rate generator | U0BRG | 0361 ₁₆ |
| UART0 transmit buffer register | U0TB | 0363 ₁₆ , 0362 ₁₆ |
| UART1 bit rate generator | U1BRG | 0369 ₁₆ |
| UART1 transmit buffer register | U1TB | 036B ₁₆ , 036A ₁₆ |

Note: It is affected only in one-shot timer mode and pulse width modulation mode.

Table 2. Affected register (M16C/61 group)

| Register name | Symbol | Address |
|--------------------------------|--------|---|
| UART2 bit rate generator | U2BRG | 0379 ₁₆ |
| UART2 transmit buffer register | U2TB | 037B ₁₆ , 037A ₁₆ |
| Up/down flag | UDF | 0384 ₁₆ |
| Timer A0 register (Note) | TA0 | 0387 ₁₆ , 0386 ₁₆ |
| Timer A1 register (Note) | TA1 | 0389 ₁₆ , 0388 ₁₆ |
| Timer A2 register (Note) | TA2 | 038B ₁₆ , 038A ₁₆ |
| Timer A3 register (Note) | TA3 | 038D ₁₆ , 038C ₁₆ |
| Timer A4 register (Note) | TA4 | 038F ₁₆ , 038E ₁₆ |
| UART0 bit rate generator | U0BRG | 03A1 ₁₆ |
| UART0 transmit buffer register | U0TB | 03A3 ₁₆ , 03A2 ₁₆ |
| UART1 bit rate generator | U1BRG | 03A9 ₁₆ |
| UART1 transmit buffer register | U1TB | 03AB ₁₆ , 03AA ₁₆ |

Note: It is affected only in one-shot timer mode and pulse width modulation mode.

Table 3. Affected register (M16C/62 group)

| Register name | Symbol | Address |
|--|--------|---|
| Dead time timer | DTT | 034C ₁₆ |
| Timer B2 interrupt occurrences frequency set counter | ICTB2 | 034D ₁₆ |
| SI/O3 bit rate generator | S3BRG | 0363 ₁₆ |
| SI/O4 bit rate generator | S4BRG | 0367 ₁₆ |
| UART2 bit rate generator | U2BRG | 0379 ₁₆ |
| UART2 transmit buffer register | U2TB | 037B ₁₆ , 037A ₁₆ |
| Up/down flag | UDF | 0384 ₁₆ |
| Timer A0 register (Note) | TA0 | 0387 ₁₆ , 0386 ₁₆ |
| Timer A1 register (Note) | TA1 | 0389 ₁₆ , 0388 ₁₆ |
| Timer A2 register (Note) | TA2 | 038B ₁₆ , 038A ₁₆ |
| Timer A3 register (Note) | TA3 | 038D ₁₆ , 038C ₁₆ |
| Timer A4 register (Note) | TA4 | 038F ₁₆ , 038E ₁₆ |
| UART0 bit rate generator | U0BRG | 03A1 ₁₆ |
| UART0 transmit buffer register | U0TB | 03A3 ₁₆ , 03A2 ₁₆ |
| UART1 bit rate generator | U1BRG | 03A9 ₁₆ |
| UART1 transmit buffer register | U1TB | 03AB ₁₆ , 03AA ₁₆ |

Note: It is affected only in one-shot timer mode and pulse width modulation mode.

Table 4. Affected register (M16C/6H group)

| Register name | Symbol | Address |
|---|--------|---|
| Display RAM address control register | CA | 0203 ₁₆ , 0202 ₁₆ |
| Font RAM address control register | FA | 0207 ₁₆ , 0206 ₁₆ |
| SYRAM address control register | YA | 020B ₁₆ , 020A ₁₆ |
| Slice RAM address control register | SA | 020F ₁₆ , 020E ₁₆ |
| VBIRAM address control register | EA | 0213 ₁₆ , 0212 ₁₆ |
| Address control register for expansion register | DA | 0217 ₁₆ , 0216 ₁₆ |
| SI/O3 bit rate generator | S3BRG | 0363 ₁₆ |
| SI/O4 bit rate generator | S4BRG | 0367 ₁₆ |
| UART2 bit rate generator | U2BRG | 0379 ₁₆ |
| UART2 transmit buffer register | U2TB | 037B ₁₆ , 037A ₁₆ |
| Up/down flag | UDF | 0384 ₁₆ |
| Timer A0 register (Note) | TA0 | 0387 ₁₆ , 0386 ₁₆ |
| Timer A1 register (Note) | TA1 | 0389 ₁₆ , 0388 ₁₆ |
| Timer A2 register (Note) | TA2 | 038B ₁₆ , 038A ₁₆ |
| Timer A3 register (Note) | TA3 | 038D ₁₆ , 038C ₁₆ |
| Timer A4 register (Note) | TA4 | 038F ₁₆ , 038E ₁₆ |
| UART0 bit rate generator | U0BRG | 03A1 ₁₆ |
| UART0 transmit buffer register | U0TB | 03A3 ₁₆ , 03A2 ₁₆ |
| UART1 bit rate generator | U1BRG | 03A9 ₁₆ |
| UART1 transmit buffer register | U1TB | 03AB ₁₆ , 03AA ₁₆ |

Note: It is affected only in one-shot timer mode and pulse width modulation mode.

Table 5. Affected register (M16C/6K group)

| Register name | Symbol | Address |
|--------------------------------|--------|---|
| SI/O3 bit rate generator | S3BRG | 0363 ₁₆ |
| SI/O4 bit rate generator | S4BRG | 0367 ₁₆ |
| UART2 bit rate generator | U2BRG | 0379 ₁₆ |
| UART2 transmit buffer register | U2TB | 037B ₁₆ , 037A ₁₆ |
| Up/down flag | UDF | 0384 ₁₆ |
| Timer A0 register (Note) | TA0 | 0387 ₁₆ , 0386 ₁₆ |
| Timer A1 register (Note) | TA1 | 0389 ₁₆ , 0388 ₁₆ |
| Timer A2 register (Note) | TA2 | 038B ₁₆ , 038A ₁₆ |
| Timer A3 register (Note) | TA3 | 038D ₁₆ , 038C ₁₆ |
| Timer A4 register (Note) | TA4 | 038F ₁₆ , 038E ₁₆ |
| UART0 bit rate generator | U0BRG | 03A1 ₁₆ |
| UART0 transmit buffer register | U0TB | 03A3 ₁₆ , 03A2 ₁₆ |
| UART1 bit rate generator | U1BRG | 03A9 ₁₆ |
| UART1 transmit buffer register | U1TB | 03AB ₁₆ , 03AA ₁₆ |
| Comparator control register | CMPCON | 03DE ₁₆ |

Note: It is affected only in one-shot timer mode and pulse width modulation mode.

Table 6. Affected register (M16C/6N group)

| Register name | Symbol | Address |
|--|--------|---|
| Dead time timer | DTT | 01CC ₁₆ |
| Timer B2 interrupt occurrences frequency set counter | ICTB2 | 01CD ₁₆ |
| SI/O3 bit rate generator | S3BRG | 01E3 ₁₆ |
| UART2 bit rate generator | U2BRG | 01F9 ₁₆ |
| UART2 transmit buffer register | U2TB | 01FB ₁₆ , 01FA ₁₆ |
| Up/down flag | UDF | 0384 ₁₆ |
| Timer A0 register (Note) | TA0 | 0387 ₁₆ , 0386 ₁₆ |
| Timer A1 register (Note) | TA1 | 0389 ₁₆ , 0388 ₁₆ |
| Timer A2 register (Note) | TA2 | 038B ₁₆ , 038A ₁₆ |
| Timer A3 register (Note) | TA3 | 038D ₁₆ , 038C ₁₆ |
| Timer A4 register (Note) | TA4 | 038F ₁₆ , 038E ₁₆ |
| UART0 bit rate generator | U0BRG | 03A1 ₁₆ |
| UART0 transmit buffer register | U0TB | 03A3 ₁₆ , 03A2 ₁₆ |
| UART1 bit rate generator | U1BRG | 03A9 ₁₆ |
| UART1 transmit buffer register | U1TB | 03AB ₁₆ , 03AA ₁₆ |

Note: It is affected only in one-shot timer mode and pulse width modulation mode.

Table 7. Affected register (M16C/6V group)

| Register name | Symbol | Address |
|--------------------------------|--------|---|
| Processor mode register 1 | PM1 | 0005 ₁₆ |
| OSD reserved register 3 | OR3 | 027B ₁₆ |
| UART2 bit rate generator | U2BRG | 0379 ₁₆ |
| UART2 transmit buffer register | U2TB | 037B ₁₆ , 037A ₁₆ |
| Up/down flag | UDF | 0384 ₁₆ |
| Timer A0 register (Note 1) | TA0 | 0387 ₁₆ , 0386 ₁₆ |
| Timer A1 register (Note 1) | TA1 | 0389 ₁₆ , 0388 ₁₆ |
| Timer A2 register (Note 2) | TA2 | 038B ₁₆ , 038A ₁₆ |
| Timer A3 register (Note 2) | TA3 | 038D ₁₆ , 038C ₁₆ |
| Timer A4 register (Note 1) | TA4 | 038F ₁₆ , 038E ₁₆ |
| UART0 bit rate generator | U0BRG | 03A1 ₁₆ |
| UART0 transmit buffer register | U0TB | 03A3 ₁₆ , 03A2 ₁₆ |
| Port P6 register | P6 | 03EC ₁₆ |
| Port P8 register | P8 | 03F0 ₁₆ |
| Port P9 register | P9 | 03F1 ₁₆ |

Note 1: It is affected only in one-shot timer mode.

Note 2: It is affected only in one-shot timer mode and pulse width modulation mode.

Table 8. Affected register (M30201 group)

| Register name | Symbol | Address |
|--------------------------------|--------|---|
| Up/down flag | UDF | 0384 ₁₆ |
| Timer A0 register (Note) | TA0 | 0387 ₁₆ , 0386 ₁₆ |
| Timer X0 register (Note) | TX0 | 0389 ₁₆ , 0388 ₁₆ |
| Timer X1 register (Note) | TX1 | 038B ₁₆ , 038A ₁₆ |
| Timer X2 register (Note) | TX2 | 038D ₁₆ , 038C ₁₆ |
| UART0 bit rate generator | U0BRG | 03A1 ₁₆ |
| UART0 transmit buffer register | U0TB | 03A3 ₁₆ , 03A2 ₁₆ |
| UART1 bit rate generator | U1BRG | 03A9 ₁₆ |
| UART1 transmit buffer register | U1TB | 03AB ₁₆ , 03AA ₁₆ |

Note: It is affected only in one-shot timer mode and pulse width modulation mode.

Table 9. Affected register (M30218 group)

| Register name | Symbol | Address |
|--------------------------------|--------|---|
| Up/down flag | UDF | 0384 ₁₆ |
| Timer A0 register (Note) | TA0 | 0387 ₁₆ , 0386 ₁₆ |
| Timer A1 register (Note) | TA1 | 0389 ₁₆ , 0388 ₁₆ |
| Timer A2 register (Note) | TA2 | 038B ₁₆ , 038A ₁₆ |
| Timer A3 register (Note) | TA3 | 038D ₁₆ , 038C ₁₆ |
| Timer A4 register (Note) | TA4 | 038F ₁₆ , 038E ₁₆ |
| UART0 bit rate generator | U0BRG | 03A1 ₁₆ |
| UART0 transmit buffer register | U0TB | 03A3 ₁₆ , 03A2 ₁₆ |
| UART1 bit rate generator | U1BRG | 03A9 ₁₆ |
| UART1 transmit buffer register | U1TB | 03AB ₁₆ , 03AA ₁₆ |

Note: It is affected only in one-shot timer mode and pulse width modulation mode.

Table 10. Instruction table for Read Modify Write

| Function | Mnemonic |
|------------------|---|
| Bit manipulation | BCLR, BNOT, BSET, BTSTC, BTSTS |
| Shift | ROL, ROR, ROT, SHA, SHL |
| Arithmetic | ABS, ADC, ADCF, ADD, DEC, EXTS, INC, MUL, MULU, NEG, SBB, SUB |
| Logical | AND, NOT, OR, XOR |
| Jump | ADJNZ, SBJNZ |

3. C language programming

Figure 3 shows an example using C programming

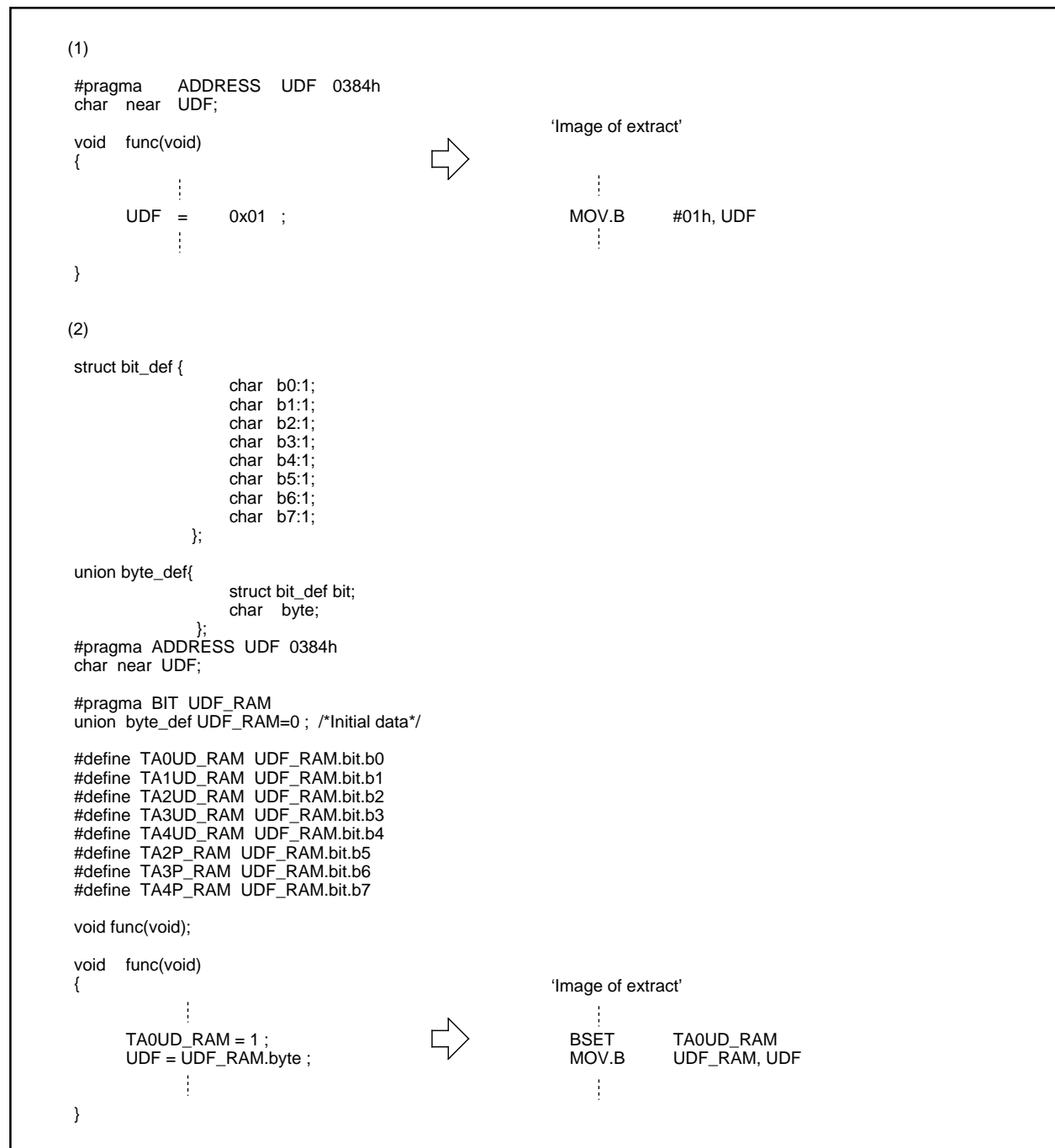
**Figure 3. Example for C programming**

Table 11. Affected register (M16C/30 group)

| Register name | Symbol | Address |
|--------------------------------|--------|---|
| UART2 bit rate generator | U2BRG | 0379 ₁₆ |
| UART2 transmit buffer register | U2TB | 037B ₁₆ , 037A ₁₆ |
| Up/down flag | UDF | 0384 ₁₆ |
| Timer A0 register (Note) | TA0 | 0387 ₁₆ , 0386 ₁₆ |
| Timer A1 register (Note) | TA1 | 0389 ₁₆ , 0388 ₁₆ |
| Timer A2 register (Note) | TA2 | 038B ₁₆ , 038A ₁₆ |
| UART0 bit rate generator | U0BRG | 03A1 ₁₆ |
| UART0 transmit buffer register | U0TB | 03A3 ₁₆ , 03A2 ₁₆ |
| UART1 bit rate generator | U1BRG | 03A9 ₁₆ |
| UART1 transmit buffer register | U1TB | 03AB ₁₆ , 03AA ₁₆ |

Note: It is affected only in one-shot timer mode and pulse width modulation mode.

MAEC TECHNICAL NEWS No. M16C-69-0104

Supplemental Description for WAIT Peripheral Function Clock Stop Bit

Classification

Corrections and supplementary explanation of document

Notes

Knowhow

✓ Others

Products Affected

M16C/60 Series

M16C/20 Series

1. Supplemental Description

The WAIT peripheral function clock stop bit (CM02) is used to halt peripheral operations during WAIT mode. When the WAIT peripheral function clock stop bit is set to "1", all the peripheral clocks generated from main clock will stop. When the MCU running in low-speed or low power dissipation mode, do not enter WAIT mode with this bit(CM02) set to "1".

We plan to add this information to the following data sheets in future.

M16C/60 Series

- M16C/62 group (M16C/62, M16C/62A)
- M16C/6H group
- M16C/6K group
- M16C/6N group
- M16C/6V group

M16C/20 Series

- M30201 group
- M30218 group
- M30220 group
- M30221 group

Attached are the corresponding pages from the M16C/62A Group data sheet to be used as reference. The underlined text represents the additional comments.

Attached: M16C/62A Group data sheet (3 pages)

MAEC TECHNICAL NEWS No. M16C-71-0105

Setting procedure of processor mode bits

Classification

Corrections and supplementary explanation of document

- ✓ Notes
- Knowhow
- Others

Products Effected

M16C/80 Series
M16C/60 Series

1. Precautions

Processor mode bits are allocated to bits 1 and 0 of the processor mode register 0. Regardless of the level of the CNVss pin, changing the processor mode bits selects the mode. Therefore, never change the processor mode bits when changing the contents of other bits. Do not change the processor mode bits simultaneously with other bits when changing the processor mode bits "012" or "112". Change the processor mode bits after changing the other bits.

Figure 1 shows the processor mode register 0 of M16C/62A group, and figure 2 shows the setting procedure of processor mode bits.

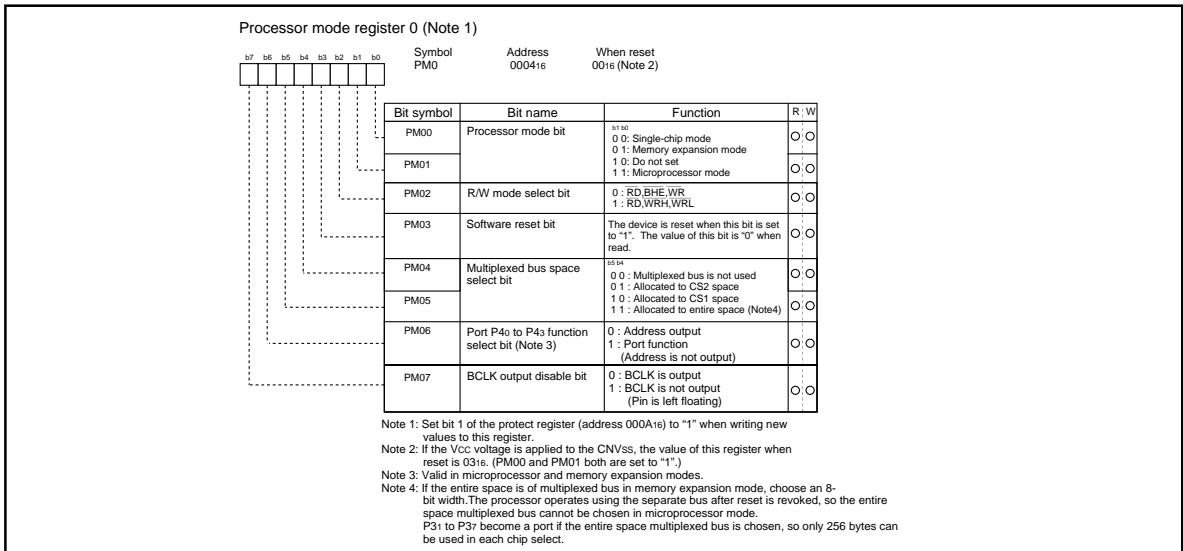


Figure 1. Processor mode register 0

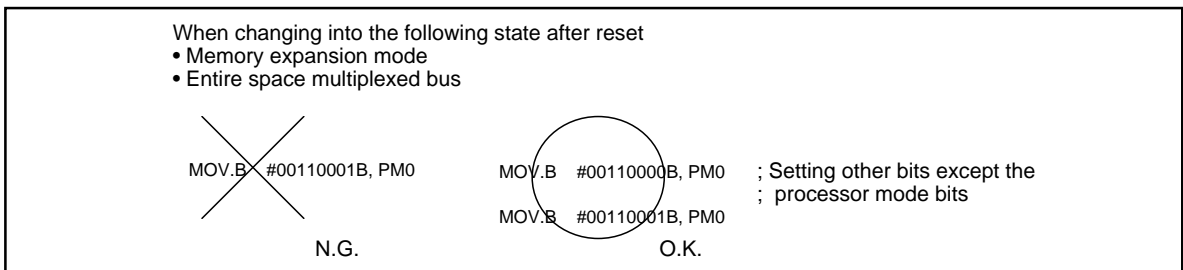


Figure 2. Setting procedure

MAEC TECHNICAL NEWS No. M16C-85-0204

M16C Family

Usage Precautions when Clearing Interrupt Request Bit

Classification

Corrections and supplementary explanation of document

✓Notes

Knowhow

Others

Products Effected

M16C/80 Series

M16C/60 Series

M16C/20 Series

Usage Precautions

When clearing an interrupt request bit of the interrupt control register, depending on the instruction used, an interrupt request bit may not get cleared.

Please use an MOV instruction to clear an interrupt request bit by modifying the interrupt control register.

When modifying the interrupt control register of M16C/60 and M16C/20 series microcontrollers (MCU), ensure that you only modify the interrupt control register when interrupt is disabled or a location in code where an interrupt will not generated.

Program examples of clearing interrupt request bit of M16C/60 series MCU:

Example 1: Modifying the interrupt control register

```

FCLR    I                ; Disable interrupts
MOV.B   #00H,0055H      ; Clear Timer A0 interrupt request bit
MOV.W   MEM,R0          ; Dummy read
FSET    I                ; Enable interrupts
    
```

Example 2: Clearing the interrupt request bit

```

FCLR    I                ; Disable interrupts
MOV.B   0055H,R0L        ; Read Timer A0 interrupt request bit
AND.B   #0F7H,R0L        ; Clear Timer A0 interrupt request bit
MOV.B   R0L,0055H        ; Write to Timer A0 interrupt request bit
MOV.W   MEM,R0          ; Dummy read
FSET    I                ; Enable interrupts
    
```

The reason why a dummy read is inserted before "FSET I" in Examples 1 and 2, is to prevent the interrupt enable flag I from being set before the interrupt control register is rewritten due to the effects of the instruction queue.

Moreover, please also refer to the interrupt precautions described in the manual.

**MITSUBISHI SEMICONDUCTORS
USAGE NOTES REFERENCE BOOK
M16C/30 Group**

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M16C/30 Group Usage Notes Reference Book



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