

To our customers,

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## Old Company Name in Catalogs and Other Documents

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Renesas Electronics Corporation

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# Low-Voltage CMOS Logic HD74LV\_A/LVC Series

## Symbols and Terms Defined

### 1. Symbols Used in Electrical Characteristics and Recommended Operating Conditions



#### 1.1 DC Characteristics

Symbol	Term	Description
$V_{IH}$	High level input voltage	High level input voltage to ensure that a logic element operates under some constraint
$V_{IL}$	Low level input voltage	Low level input voltage to ensure that a logic element operates under some constraint
$V_{OL}$	Low level output voltage	Output voltage in effect when, under the input conditions bringing the output low, the rated output current $I_{OL}$ (for example the max. current supposing max. fan outs) is allowed to flow to the output terminal
$V_{OH}$	High level output voltage	Output voltage in effect when, under the input conditions bringing the output high, the rated output current $I_{OH}$ (for example the max. current supposing max. fan outs) is allowed to flow from the output terminal.
$I_{IH}$	High level input current	The current from an input when a rated high level voltage is applied to the input
$I_{IL}$	Low level input current	The current from an input when a rated low level voltage is applied to the input
$I_{OH}$	High level output current	The current from an output when a rated high level voltage $V_{OH}$ is applied to the output
$I_{OL}$	Low level output current	The current into an output when a rated low level voltage $V_{OL}$ is applied to the output
$I_{OZ}$	Off-state (high-impedance) output current	The current at a three-state output under the input conditions bringing the output high-impedance state
$I_I$	Input leakage current	The current into an input when the rated maximum input voltage is applied to the input
$I_{CC}$	Supply current	The current into the voltage supply pin ( $V_{CC}$ )
$\Delta I_{CC}$	Change of supply current under rated level input	Change of supply current per input pin when a rated input voltage is applied

## 1.2 AC Characteristics

Symbol	Term	Description
f <sub>max</sub>	Maximum clock frequency	Maximum clock frequency that maintains the stable changes in output logic level in the rated sequence under the I/O condition allowing clock pulses to change the output state
t <sub>PLH</sub>	Output rise propagation delay time	Delay time between the rated voltage levels of an I/O voltage waveform under a defined load condition, with the output changing from low level to high level
t <sub>PHL</sub>	Output fall propagation delay time	Delay time between the rated voltage levels of an I/O voltage waveform under a defined load condition, with the output changing from high level to low level
t <sub>HZ</sub>	3-state output disable time (high level)	Delay time between the rated voltage levels of an I/O voltage waveform under a defined load condition, with the 3-state output changing from high level to the high-impedance state
t <sub>LZ</sub>	3-state output disable time (low level)	Delay time between the rated voltage levels of an I/O voltage waveform under a defined load condition, with the 3-state output changing from low level to the high-impedance state
t <sub>ZH</sub>	3-state output enable time (high level)	Delay time between the rated voltage levels of an I/O voltage waveform under a defined load condition, with the 3-state output changing from the high-impedance state to high level
t <sub>ZL</sub>	3-state output enable time (low level)	Delay time between the rated voltage levels of an I/O voltage waveform under a defined load condition, with the 3-state output changing from the high-impedance state to low level
t <sub>w</sub>	Pulse width	Duration of time between the rated levels from a leading edge to a trailing edge of pulse waveform
t <sub>h</sub>	Hold time	Duration the specified input terminal must hold data after a change at another related input terminal (e.g., clock input)
t <sub>SU</sub>	Setup time	Duration the specified input terminal must set up and keep data before a change at another related input terminal (e.g., clock input)
t <sub>rec</sub>	Recovery time	Duration between the time when data at the specified input terminal is released and the time when another related input terminal (e.g., clock input) can be changed

## 2. Symbols Used in Function Tables

Symbol	Description
H	High level (in steady state; written "H" or H level in sentences)
L	Low level (in steady state; written "L" or L level in sentences)
↑	Transition from L level to H level
↓	Transition from H level to L level
X	Either H or L
Z	3-state output off (high impedance)
a.....h	Input level of steady state for each of inputs A-H
Q <sub>0</sub>	Q level immediately before the indicated input condition is established
$\overline{Q_0}$	Complement of Q <sub>0</sub>
Q <sub>n</sub>	Q level immediately before the latest active change (↑ or ↓) occurs
	Single H level pulse
	Single L level pulse
TOGGLE	Each output is changed to the complement of the preceding state by an active input change (↑ or ↓)

### Revision Record

Rev.	Date	Description	
		Page	Summary
1.00	Jul.09.04	—	First edition issued

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