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April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (<http://www.renesas.com>)

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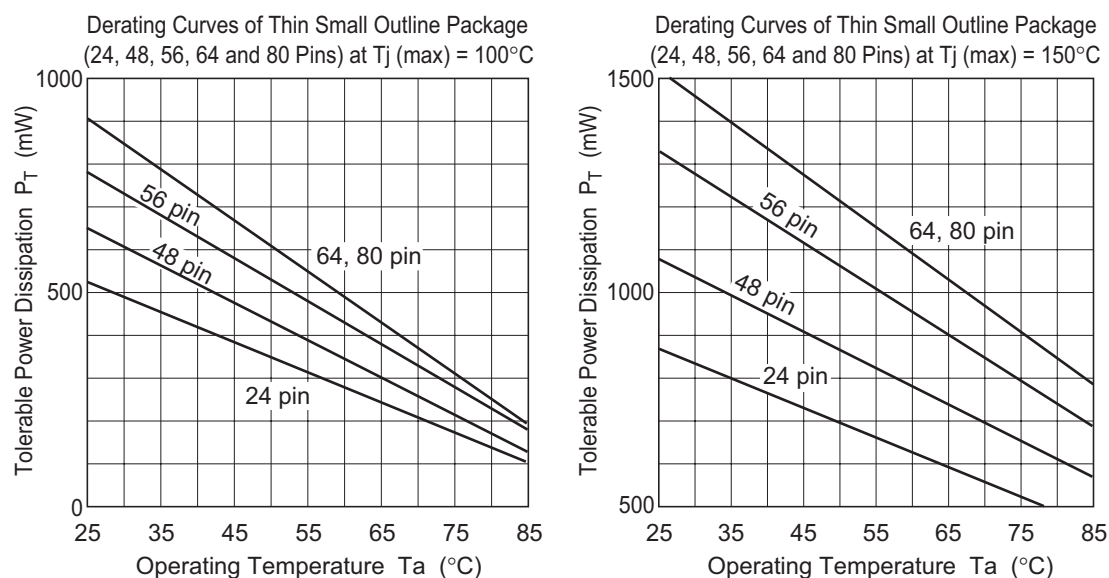
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Low-Voltage CMOS Logic HD74ALVC Series

Package Thermal Resistance

1. Thermal Resistance of TSSOP

Figure 1 shows the derating curve of TSSOP with HD74ALVC devices, table 1 shows the thermal resistance (θ_{j-a}) and figure 2 shows the mounting method.

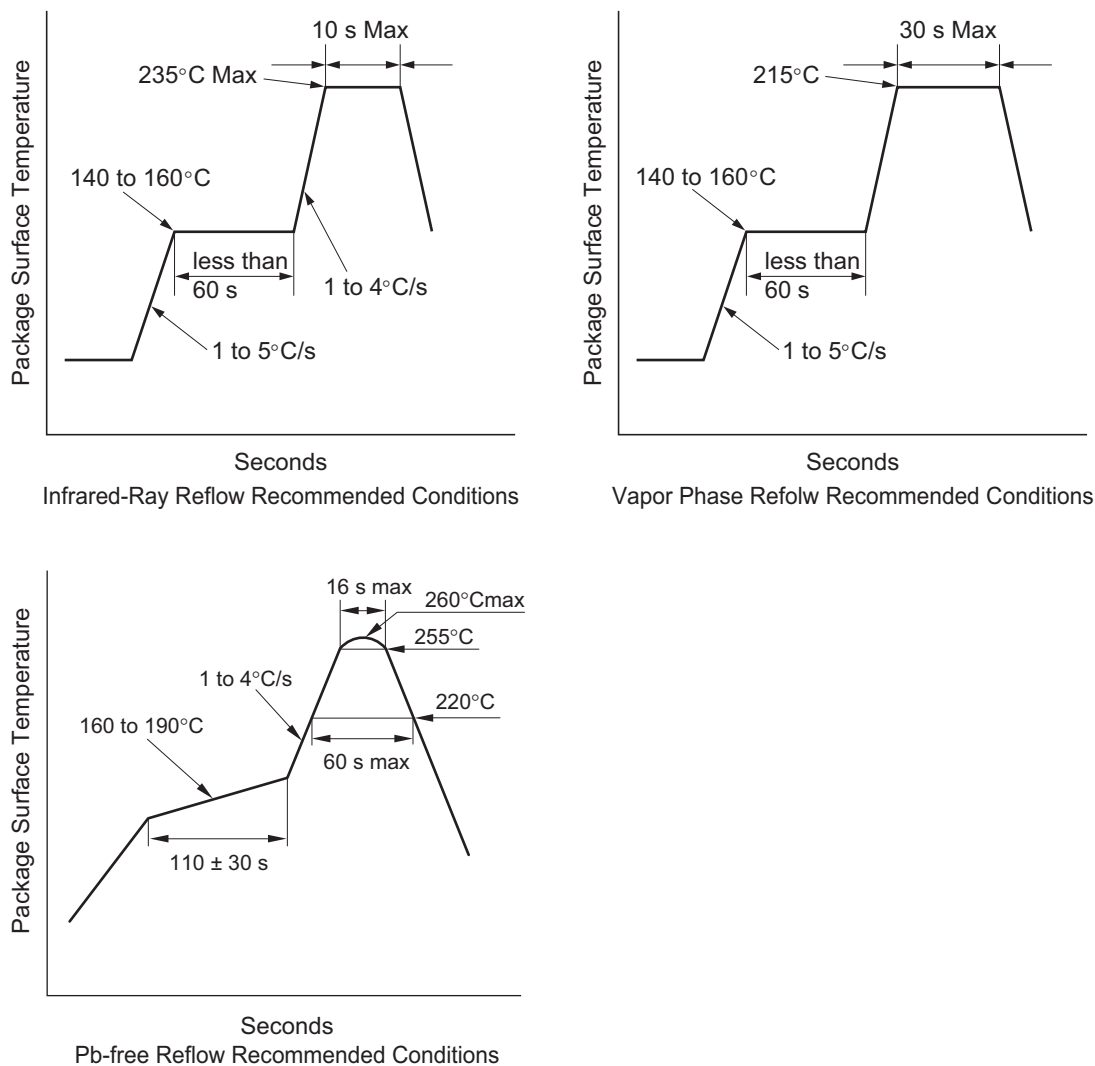


Note: For the ambient temperature less than 25°C, the power dissipation at 25°C is applied. The data above are measured by ΔV_{BE} method mounting on glass epoxy board (40 × 40 × 1.6 mm) with 10% of wiring density. In the actual application, using conditions, ambient temperature and forced air-cooling conditions should be sufficiently examined.

Figure 1 Derating Curve of TSSOP

Table 1 Thermal Resistance of TSSOP Package

Pin Count	Wind Speed	Derating Factor	Thermal Resistance	Tolerable Power Dissipation	
				at Tj (max) = 150°C	at Tj (max) = 100°C
24	0 m/s	6.9 mW/°C	145°C/W	862 mW	518 mW
48	0 m/s	8.7 mW/°C	115°C/W	1087 mW	652 mW
56	0 m/s	10.5 mW/°C	95°C/W	1316 mW	790 mW
64	0 m/s	12.1 mW/°C	82°C/W	1512 mW	907 mW
80	0 m/s	12.1 mW/°C	82°C/W	1512 mW	907 mW

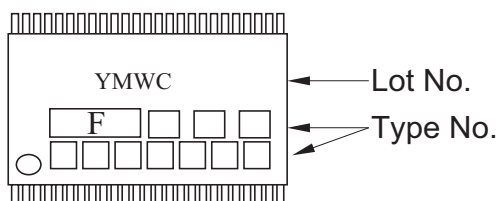


Note: As mounting methods for TSSOP (24, 48, 56, 64 and 80 pins), Renesas recommends the infraredray reflow, vapor phase reflow and Pb-free reflow. (Solder-dip is not recommended.)

Figure 2 Mounting Method of TSSOP

2. Marking on Package

Thin Shrink Small outline Package 24, 48, 56, 64 and 80 pins



Note: F: Family name (ALVC, SSTV and CDC series)
 Y: Year code (the last digit of year)
 M: Month code
 W: Week code
 C: Control code
 Type No: delete HD74 and package code (T) from device name

Revision Record

Rev.	Date	Description	
		Page	Summary
1.00	Jul.09.04	—	First edition issued

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