

HIGH SPEED ADC INPUT INTERFACE SOLUTIONS

ISL55210

**ADDING A LOW POWER, VERY
HIGH DYNAMIC RANGE LAST STAGE
INTERFACE TO HIGH SPEED ADC'S**

intersilTM

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SIMPLY SMARTERTM

ISL55210 Front Page of Data Sheet

Wideband, Low-Power, Ultra-High Dynamic Range Differential Amplifier

ISL55210

The ISL55210 is a very wide band, Fully Differential Amplifier (FDA) intended for high dynamic range ADC input interface applications. This voltage feedback FDA design includes an independent output common mode voltage control.

Intended for very high dynamic range ADC interface applications, at the lowest quiescent power (115mW), the ISL55210 offers a 4.0GHz Gain Bandwidth Product with a very low input noise of $0.85\text{nV}/\sqrt{\text{Hz}}$. In a balanced differential I/O configuration, with $2\text{V}_{\text{P-P}}$ output into a 200Ω load configured for a gain of 15dB, the IM3 terms are $<-100\text{dBc}$ through 110MHz. With a minimum operating gain of $2\text{V}/\text{V}$ (6dB), the ISL55210 supports a wide range of higher gains with minimal BW or SFDR degradation. Its ultra high differential slew rate of $5,600\text{V}/\mu\text{s}$ ensures clean large signal SFDR performance or a fast settling step response.

The ISL55210 requires only a single 3.3V (max 4.2V) power supply with 35mA typical quiescent current. This industry leading low current solution can be further reduced when needed using the optional power shutdown to $<0.4\text{mA}$ supply current. External feedback and gain setting resistors give maximum flexibility and accuracy. A companion device, the ISL55211, includes on-chip feedback and 3 possible gain setting connections where an internally fixed gain solution is

Features

- Gain Bandwidth Product 4.0GHz
- Input Voltage Noise $0.85\text{nV}/\sqrt{\text{Hz}}$
- Differential Slew Rate $5,600\text{V}/\mu\text{s}$
- $2\text{V}_{\text{P-P}}$, 2-tone IM3 (200Ω) 100MHz -109dBc
- Supply Voltage Range 3.0V to 4.2V
- Quiescent Power (3.3V Supply) 115mW

Applications

- Low Power, High Dynamic Range ADC Interface
- Differential Mixer Output Amplifier
- SAW Filter Pre/Post Driver
- Differential Comms-DAC Output Driver

Related Products

- *Coming Soon:* ISL55211 - Fixed Gain Version of the ISL55210
- [ISLA112P50](#) - 12-bit, 500MSPS ADC ($<500\text{mW}$)
- *Coming Soon:* ISLA214P50 - 14-bit, 500MSPS ADC ($<850\text{mW}$)

ISL55210 – Low Power, Wideband FDA

Differential I/O, Voltage Feedback, with output Common mode control.

- 3.0V to 4.5V supply voltage range
- 35mA on 3.3V supply (production trimmed) , 115mW power
- 4.0GHz gain bandwidth product, 5600V/usec slew rate
- 0.85nV/ $\sqrt{\text{Hz}}$ input voltage noise, 5pA/ $\sqrt{\text{Hz}}$ input current noise
- Default output common mode voltage at 1.2V on single 3.3V supply

Significant loop gain at lower frequencies

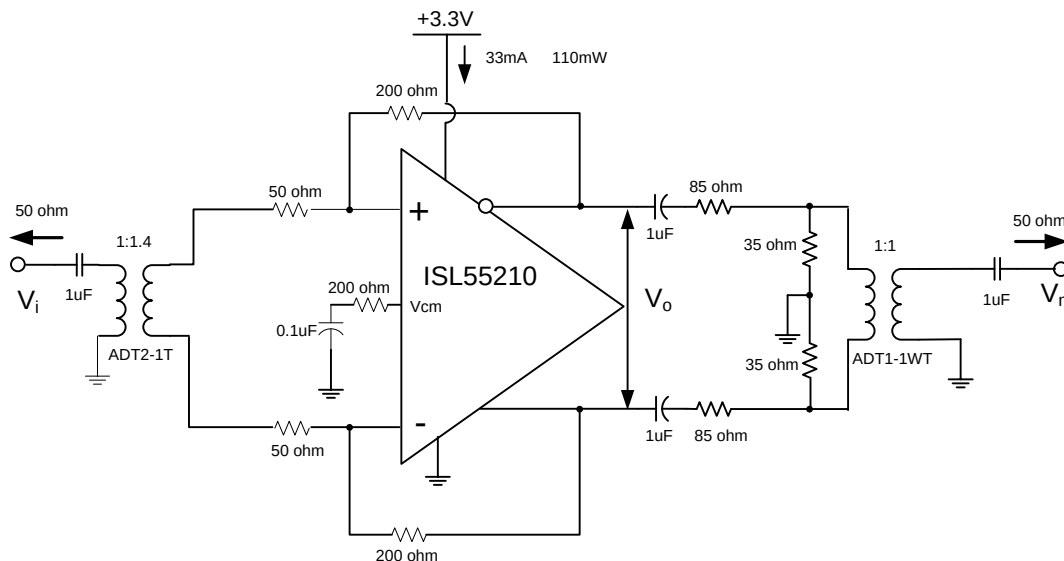
- Intended to hold > 100dBc SFDR to >100MHz frequencies.

While the device can operate DC coupled (with a negative supply voltage), most data has been taken with a specific apps circuit that offers considerable even order distortion suppression.

ISL55210 – 100kHz ->200Mhz Apps Circuit

Focusing first on the input side of the solution to the amplifier Rg elements, we do most of the characterization with the following applications circuit. This circuit is available on our Eval board.

- AC coupled input to a broadband 1:1.4 turns ratio transformer – the ADT2-1T is setting the bandwidth to 100kHz to 400Mhz in this circuit.
- Gain resistors act as input termination. Their sum, 100ohm to the virtual ground nodes of the differential op amp, reflect to the input side as a 50Ω input termination.
- Total gain $V_o/V_i = 1.4*4 = 5.2V/V$ (15dB)
- Output is AC coupled into a 200ohm differential load – 1:1 transformer is only for measurement purposes – would not normally be used in an ADC interface design.



Building Towards a Full ADC Interface Solution

While we need to provide the whole solution, we normally break this into pieces looking first at the amplifier by itself then combining it with various interstage circuits from the amplifier to the ADC to get a combined solution.

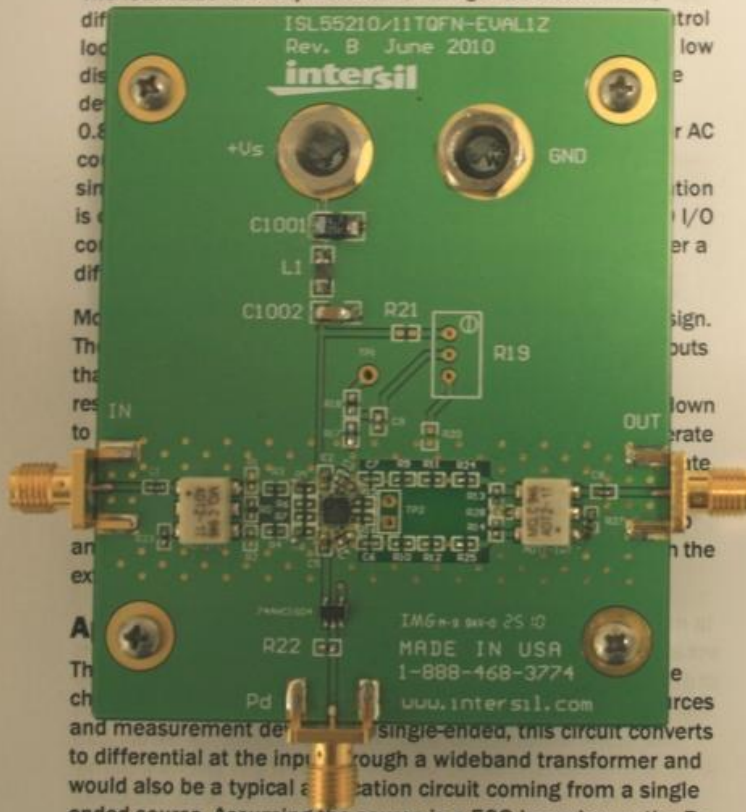
- Most of the data has been with this 200ohm load getting out through a 1:1 transformer while presenting a 50ohm source to our spectrum analyzers. This introduces about a 17dB insertion loss from the amplifier outputs to the single ended output from the transformer.
- This is what we call the ISL55210 Eval board. That board also includes the option to insert a differential RLC interface with ADC input R & C to test filter performance
- Adding the required elements to drive into an Intersil ADC leads to various ADC daughterboard designs where we can also insert various interstage filter designs and take FFT data.
- Before we get to those ADC daughterboard results, let's look at some amplifier only issues and measured data.
- The ISL55210 also has a fixed gain version, ISL55211 offering 3 internal gain settings.

ISL55210/11 Eval Board

Applications

Basic Operation

The ISL55210 is a very wideband, voltage feedback based,



and measurement device. This circuit converts to differential at the input through a wideband transformer and would also be a typical application circuit coming from a single ended source. Assuming the source is a 50Ω impedance, the R_G resistors are set to provide both the input termination and the gain. Since the inverting summing nodes act as virtual ground

FIGURE 27. SUPPLY CURRENT vs SUPPLY VOLTAGE

values. Since the ISL55210 is a VFA design, increasing the feedback resistor to get higher gain does not directly reduce the bandwidth as it would with a CFA based design. This gives increased flexibility in the input turns ratio and overall gain setting (while holding a matched input impedance) over alternate solutions.

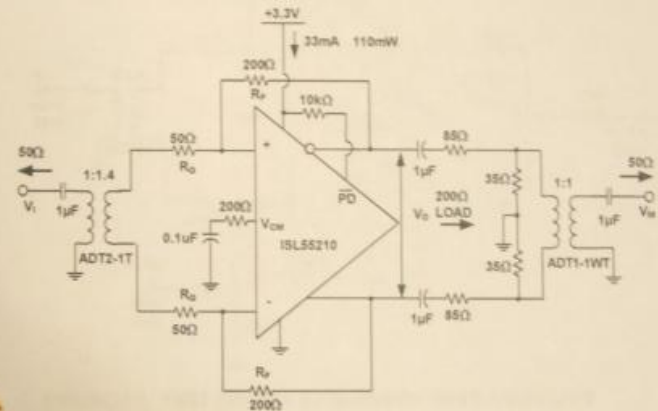


FIGURE 28. TEST CIRCUIT #1

Working with a transformer coupled input as shown in Figure 28, or with two DC blocking caps from a differential source, means the output common mode voltage set by either the default internal V_{CM} setting, or a voltage applied to the V_{CM} control pin, will also appear as the input common mode voltage. This provides a very easy way to control the ISL55210 I/O common mode operating voltages for an AC coupled signal path. The internal common mode loop holds the output pins to V_{CM} and, since there is no DC path for an I_{CM} current back towards the input in Figure 28, that V_{CM} setting will also appear as the input common mode voltage. It is useful, for this reason, to leave any input transformer secondary center tap unconnected. The

Amplifier only testing on the Rev. C EVM board

Since the IM3 can usually not be filtered, most of the design and early characterization effort was focused on the IM3. Below is some recently measured data. The differential structure of the amplifier stage does a good job of suppressing even order distortion, but with IM3 this low, HD2 it is in fact now the limiting issue in the interface.

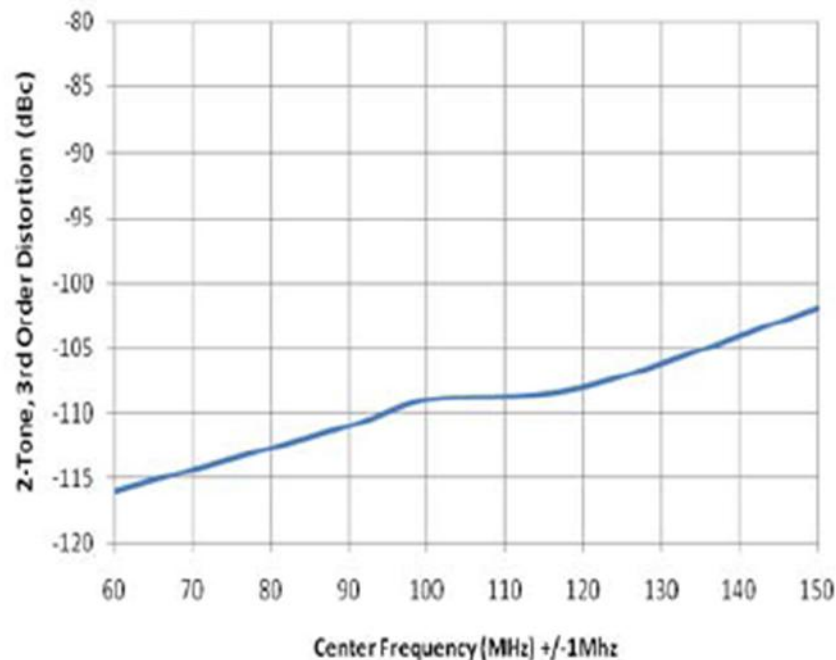
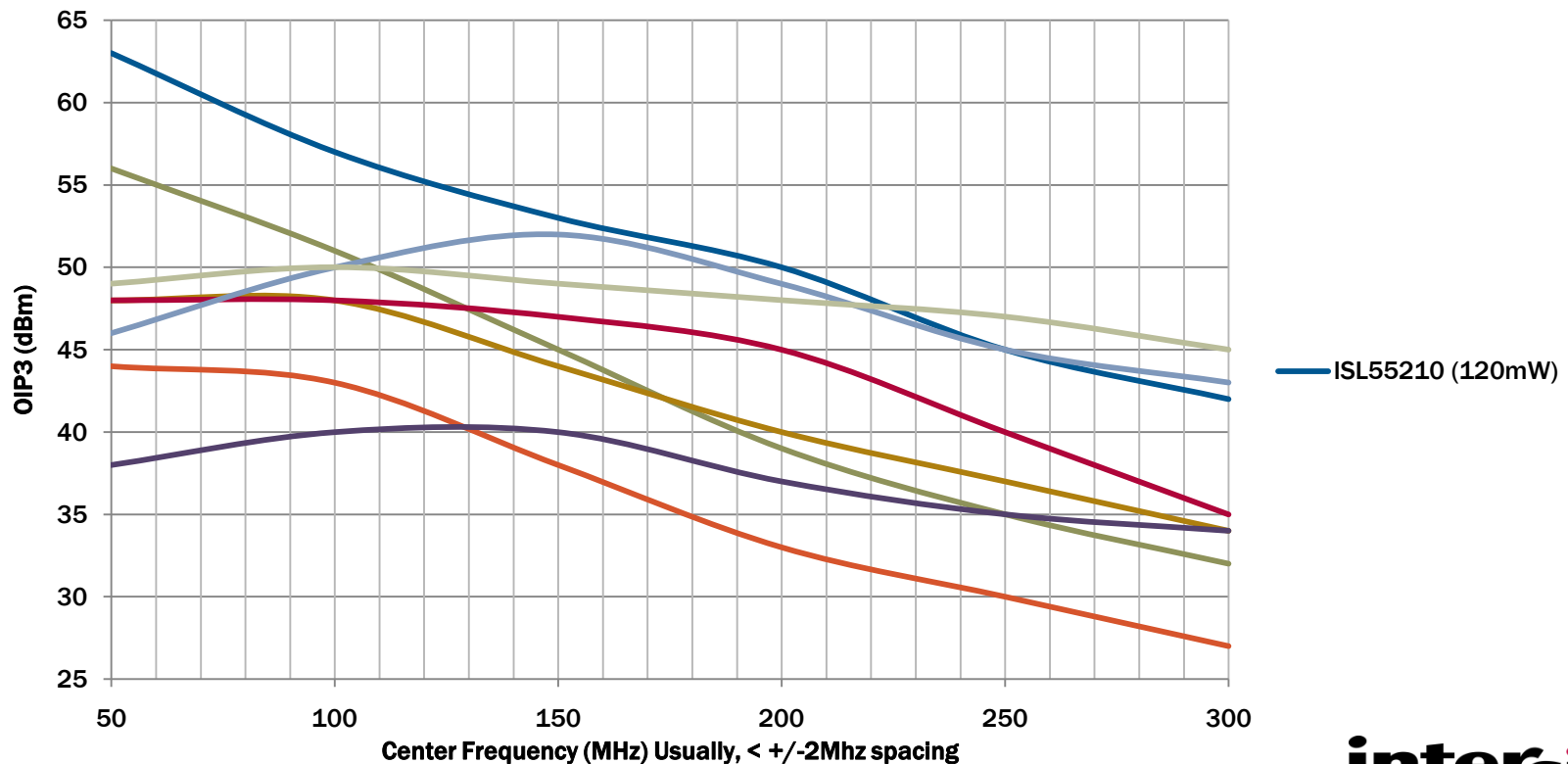


FIGURE 2. 2Vpp 200 ohm load, 3rd order intermodulation Distortion

ISL55210 – Performance Comparison IM3

This compares most of the best FDA devices for 3rd order intercept – high is good here. We far outperform the competitive devices through 150MHz and all competitive devices require higher quiescent power.

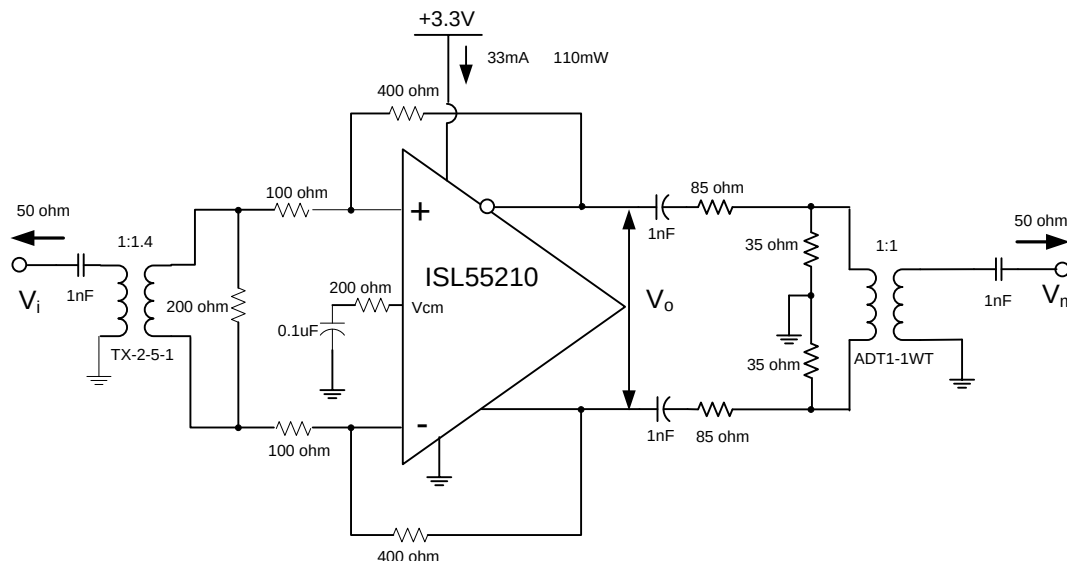
OIP3 for Differential Drivers (200 Ω) Load



ISL55210 – 300MHz ->600Mhz Apps Circuit

To test performance at higher frequencies in a similar configuration, the following circuit was used for these tests.

- AC coupled input to a higher frequency 1:1.4 turns ratio transformer (2Mhz -> 800Mhz)
- Gain and feedback resistors scaled up a bit to reduce output loading. This required an added input shunt R of 200Ω to get the input match which will increase noise figure.
- Total gain $V_o/V_i = 1.4 \times 4 = 5.2V/V$ (15dB)
- Output is AC coupled into a 200ohm differential load – 1:1 transformer is only for measurement purposes – would not normally be used in an ADC interface design.

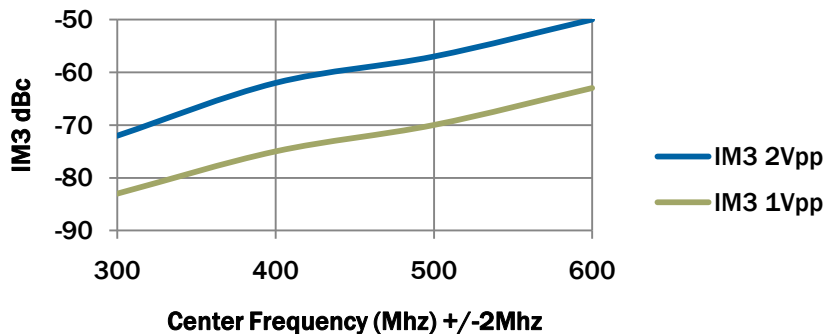


ISL55210 – 300Mhz ->600Mhz IM3 and IM2

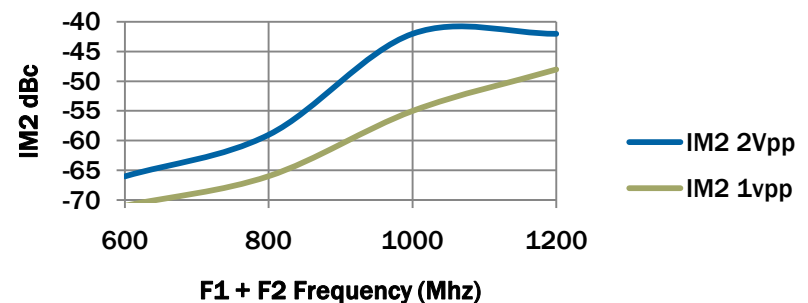
2-tone testing was done at 2Vpp output envelope and 1Vpp output envelope. (does show intercept characteristic vs. output swing)

- Each test frequency was then a 1Vpp and then 0.5Vpp across the differential outputs.
- Used a +/-2Mhz spacing around each test center frequency (Fo). This puts the IM2 terms at 4Mhz and 2*Fo and the IM3 terms at Fo +/- 6Mhz.
- 4Mhz IM2 term falls where there is considerable loop gain and is consistently un-measurable. Simulations estimate it should be < -120dBc below the carriers.
- 2*Fo term falls at a much higher, lower loop gain, frequency giving rapidly decreasing suppression. This term, however, can often be filtered out prior to the converter input.

**ISL55210, gain 15dB, 200ohm
load IM3**



**ISL55210, gain 15dB, 200ohm
load IM2**

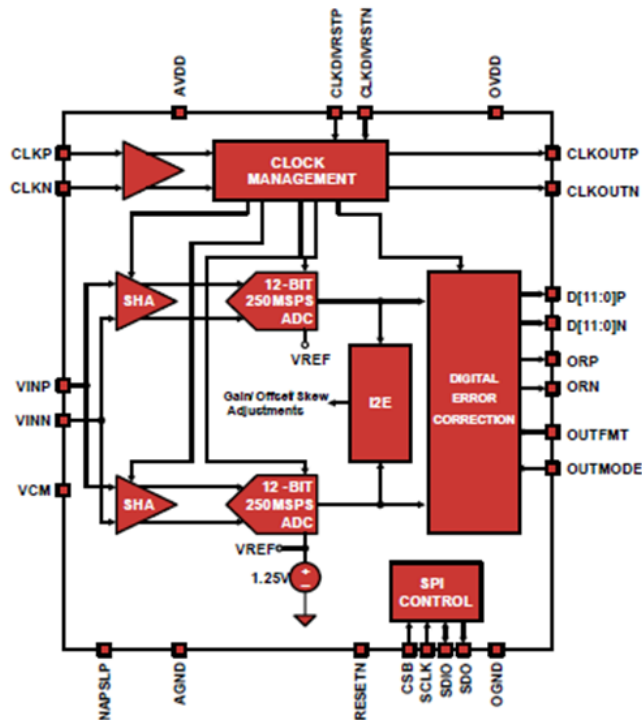


Intersil High Speed ADC Options

All of these ADC's use the Femto-Charge technique pioneered by Kenet – now part of Intersil.

The latest 12Bit, 500MSPS ADC is the ISLA112P50 using <500mW power. This is an interleaved ADC using two 250MSPS cores.

Block Diagram



Pin-Compatible Family

MODEL	RESOLUTION	SPEED (MSPS)
ISLA112P50	12	500
ISLA110P50	10	500
ISLA118P50	8	500

Key Specifications

- SNR = 65.8dBFS for $f_{IN} = 190\text{MHz}$ (-1dBFS)
- SFDR = 80dBc for $f_{IN} = 190\text{MHz}$ (-1dBFS)
- Total Power Consumption = 455mW

Intersil High Speed ADC Options

For 1st Nyquist zone designs, the ISLA112P50 is in -80dBc to -90dBc on the HD2 and HD3 terms. This data is taken with the two transformer input interface typical of ADC characterization.

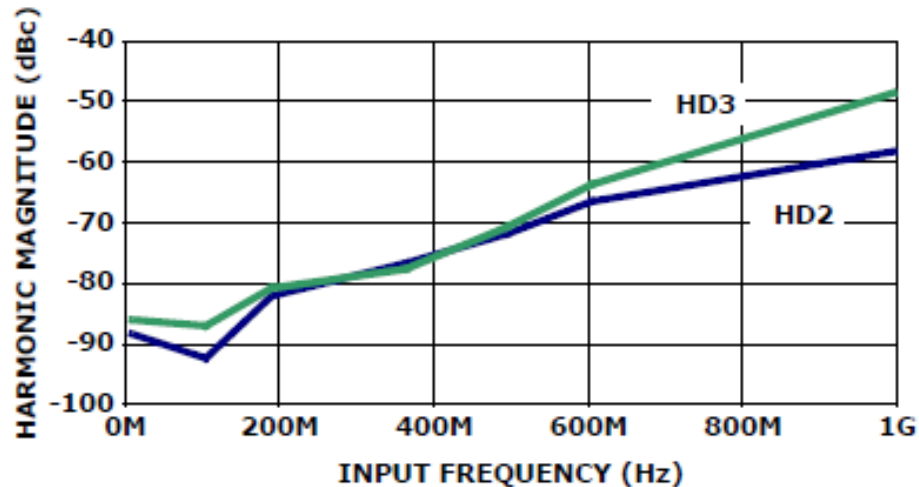


FIGURE 5. HD2 AND HD3 vs f_{IN}

Beyond this, there is an emerging family of 12,14, and 16bit ADCs based on a 14bit core.

Combining Amplifiers with ADCs

The input spectrum to the ADC inputs can be considered to have its own SNR and SFDR characteristics. Referenced from a single tone signal swing amplitude at -1dBFS (in RMS), an SNR can be developed from the spot noise at the amplifier outputs and the integration BW to the ADC inputs. The SFDR is simply the HD2 or HD3 dBc delivered to the ADC inputs for that level of signal swing.

- For SNR, combining the ADC with the input signal is an RMS calculation,

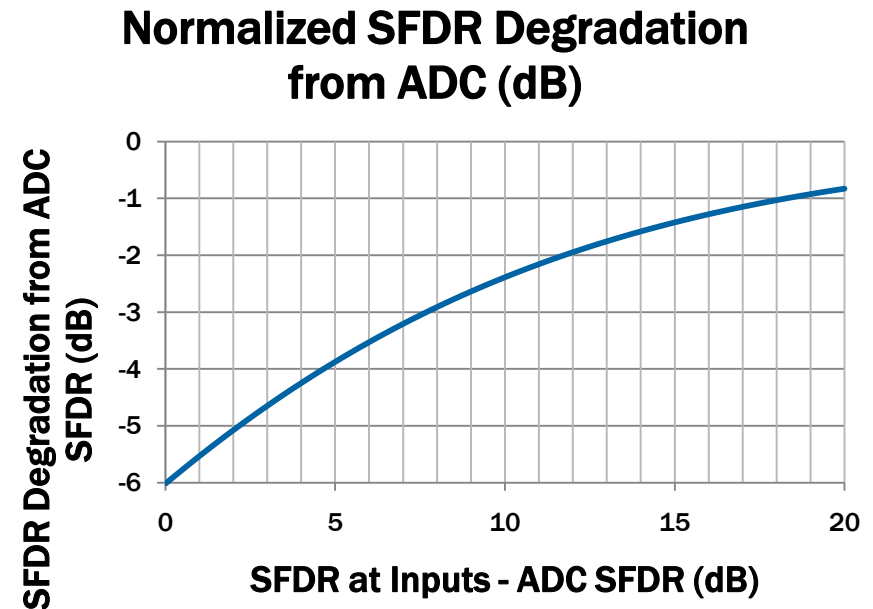
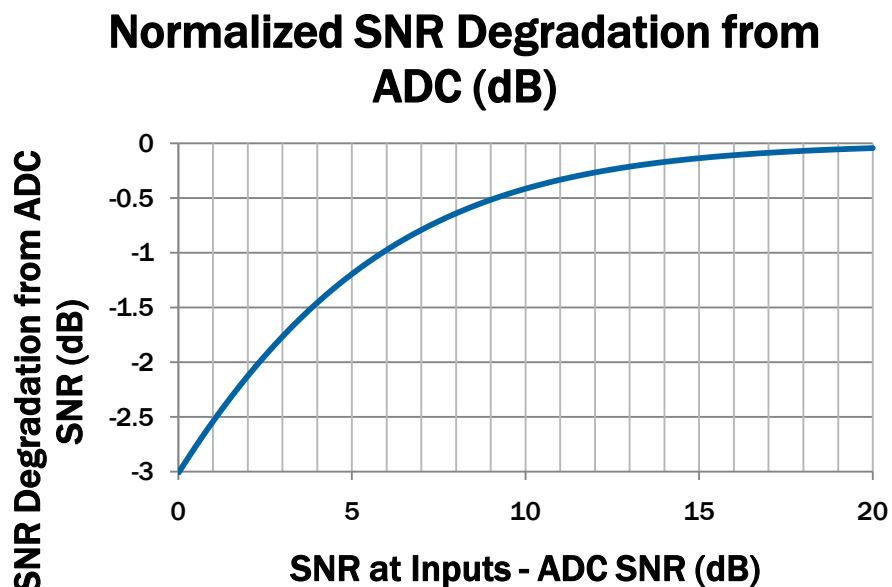
$$SNR_{System} = -20 \cdot \log \sqrt{\left(10^{\frac{-SNR_{ADC}}{20}}\right)^2 + \left(10^{\frac{-SNR_{Op-Amp}}{20}}\right)^2}$$

- For SFDR, the spurious combine linearly so it is straight addition of spurious amplitude- stating that in an SFDR specification form gives this.

$$SFDR_{System} = -20 \cdot \log \left(10^{\frac{-SFDR_{ADC}}{20}} + 10^{\frac{-SFDR_{Amp}}{20}} \right)$$

Drop from ADC Specification Adding the Amplifier

We can normalize these two equations to show just the degradation from any ADC SNR or SFDR given an input signal that has its own SNR and SFDR that is $\geq$ ADC. These curves start at 0dB on the x-axis, which is where the SNR and SFDR coming into the ADC equals the ADC numbers, then go up from there showing the effect of design margin in the input signal. SFDR needs a lot of margin.



ISL55210 – Combined with 12Bit 500MSPS ADC

Value Proposition:

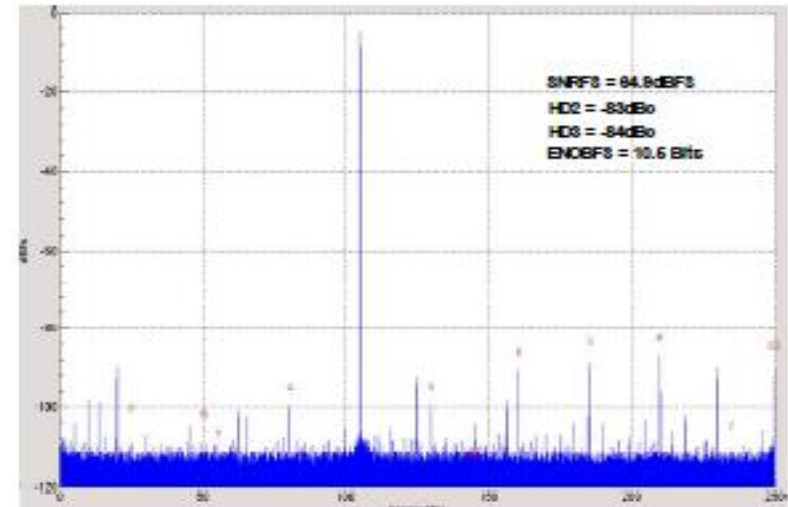
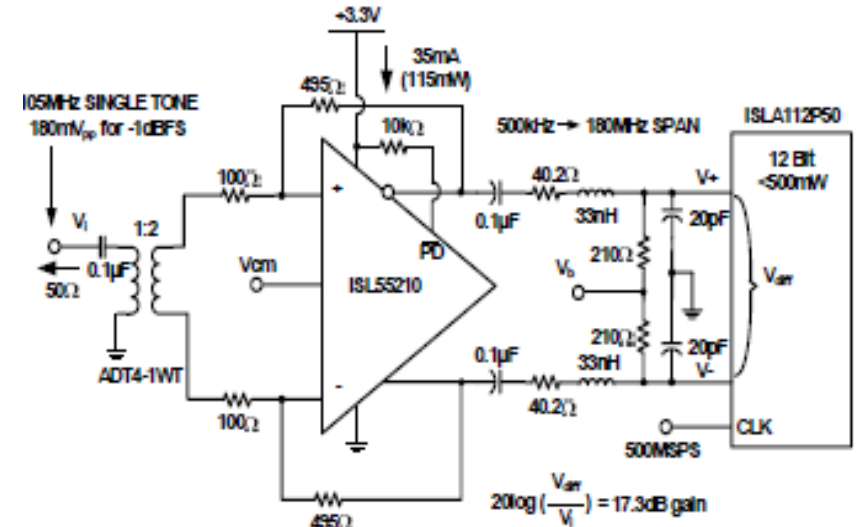
- **Industry's Lowest Power, Lowest HD, FDA (Fully Differential Amplifier)**

Key Strengths

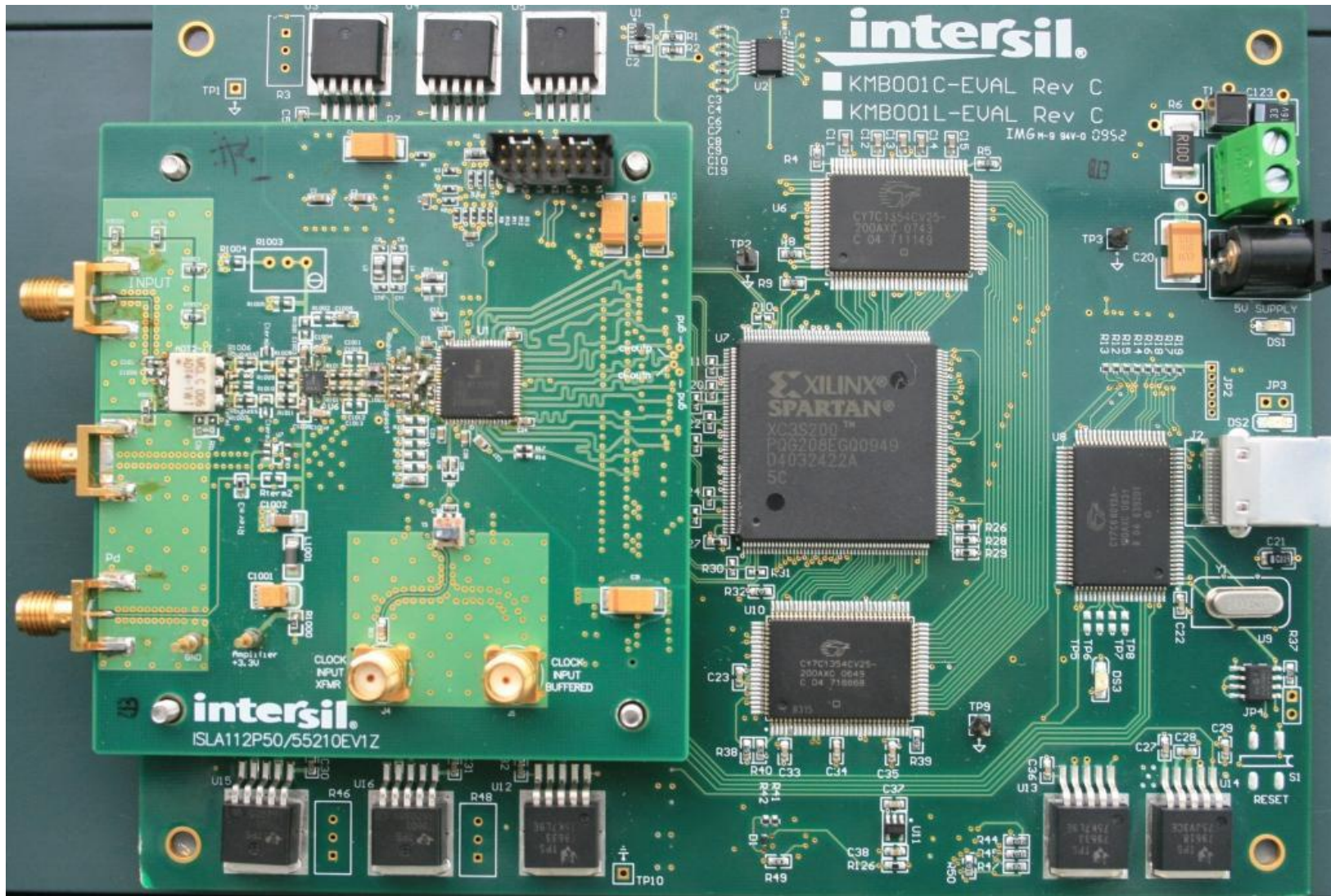
- **4GHz Gain Bandwidth Product. VFA design.**
- **Lowest input noise at $0.85\text{nV}/\sqrt{\text{Hz}}$**
- **Lowest power – 35mA on 3.3V supply (115mW)**
- **Lowest distortion (HD3 <-100dBc through 100MHz)**

Amplifier + ADC FFT

- Here a 17.3dB gain circuit is combined with an output 2nd order low pass filter to give a controlled noise power bandwidth interface with very good FFT results

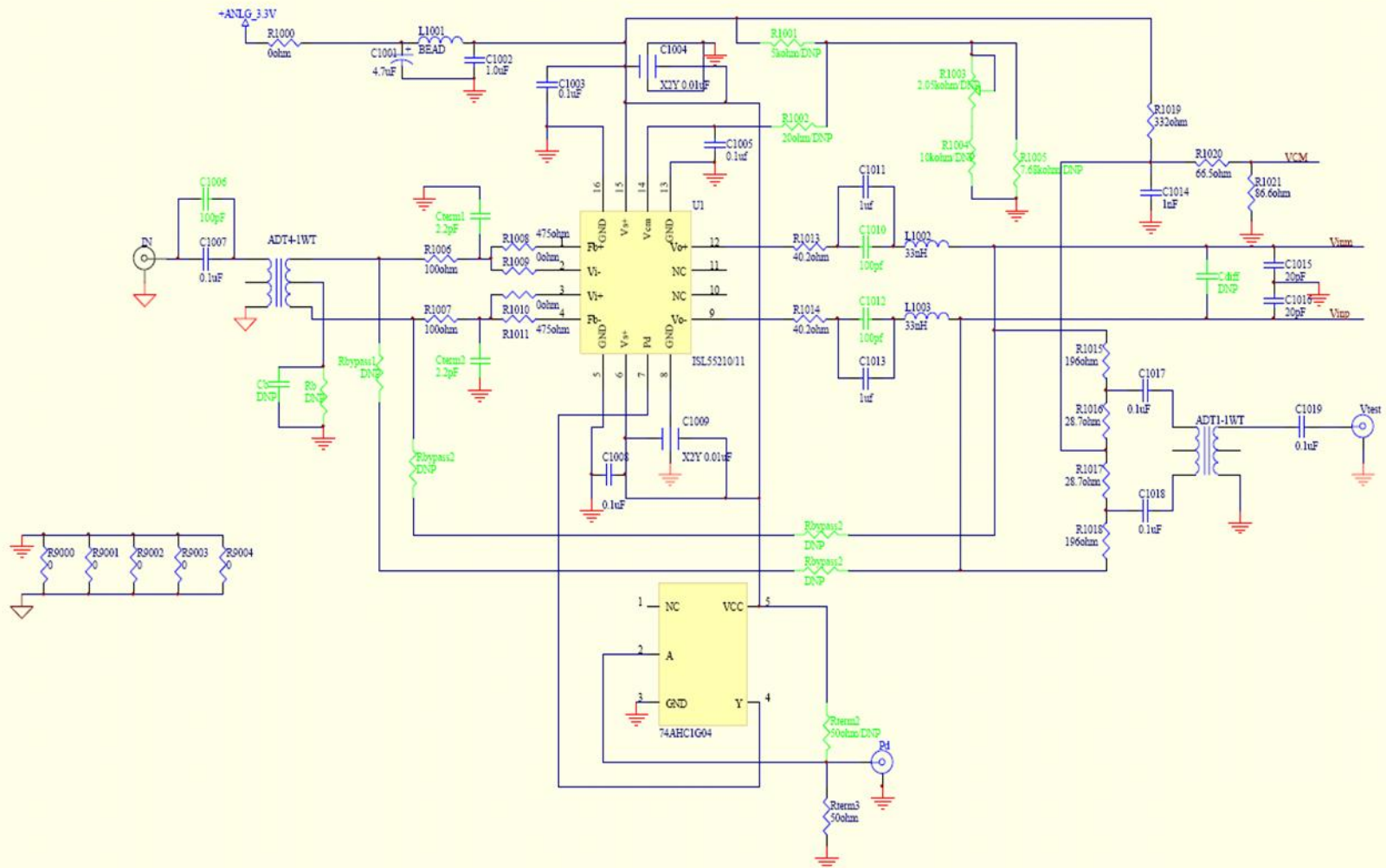


ISL55210 + ISLA112P50 ADC Daughterboard



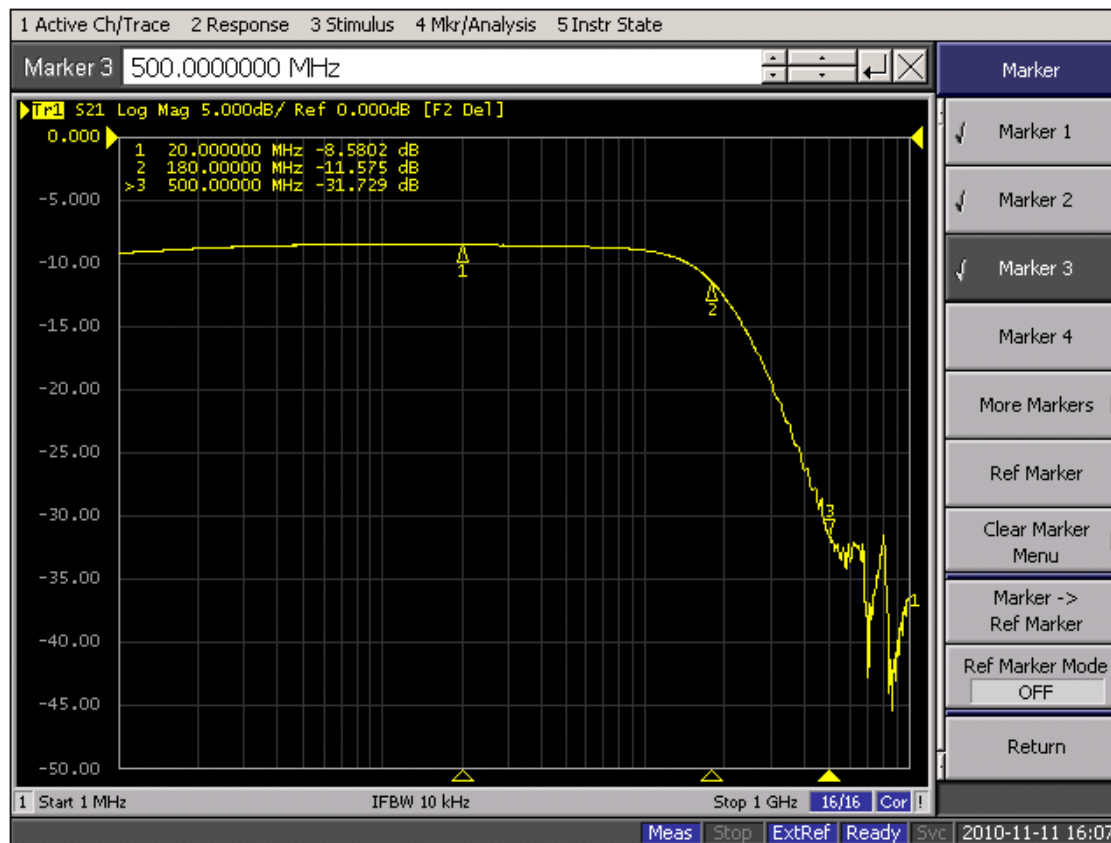
Design Example with the ISL55210 + ISLA112P50

Details for the circuit example design using a 1:2 turns ratio step up on the input and an RLC filter flat through 120MHz using a resistor bias for the lcm as the interstage connection (green are optional elements)



Design Example with the ISL55210 + ISLA112P50

This circuit includes a passive differential to single ended measurement port as part of the shunt R element in the filter. This allows us to measure the frequency response right up to the ADC input with the ADC clocking. This solution is giving 18dB gain to the ADC but the test port has 27db insertion loss – but it gives us the shape we want. 180MHz -3dB here



Comparative SNR and SFDR Data

Measuring single tone from 65Mhz to 115Mhz for this 18dB gain interface with postfilter vs. the simple 2 transformer interface that requires about 10dBm input power for -1dBFS. The amplifier interface has dropped the required input swing to 180mVpp from 2Vopp with minimal SNR or SFDR degradation.

- ISL55210 gain of 18dB interface test data.

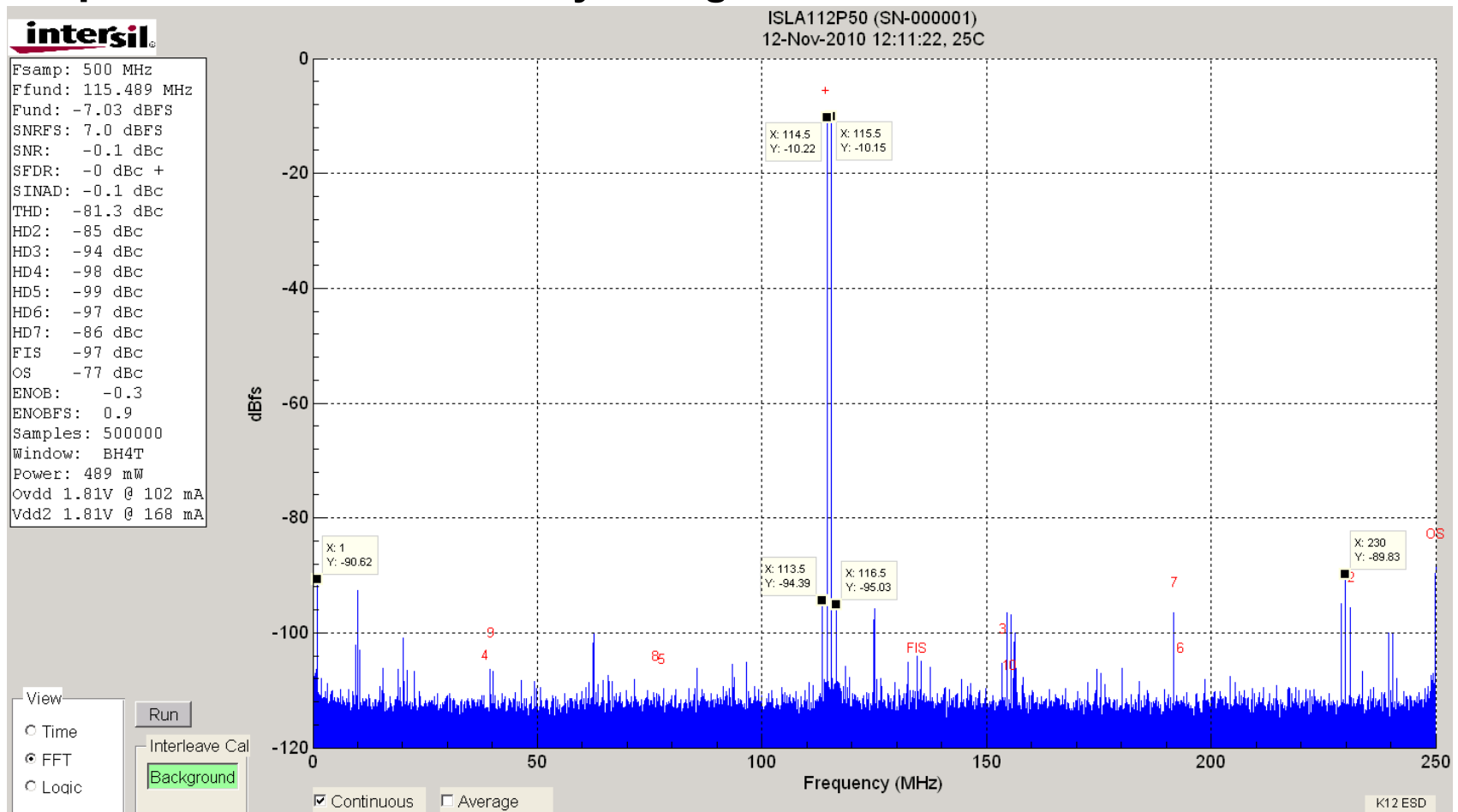
Frequency (MHz)	SNRFS (dBFS)	SNR (dBc)	SFDR (dBc)	HD2 (dBc)	HD3 (dBc)
65	64.8	63.8	78	-78	-85
75	64.9	63.8	80	-80	-85
85	64.8	63.8	80	-82	-84
95	64.7	63.8	80	-87	-82
105	64.8	63.8	80	-90	-82
115	64.7	63.8	79	-82	-84

- Simple 2 transformer interface test data – typical ADC characterization data

Frequency (MHz)	SNRFS (dBFS)	SNR (dBc)	SFDR (dBc)	HD2 (dBc)	HD3 (dBc)
65	65.8	64.8	86	-98	-94
75	65.8	64.8	84	-105	-84
85	65.7	64.7	83	-90	-86
95	65.7	64.7	83	-88	-89
105	65.6	64.6	82	-90	-85
115	65.5	64.6	81	-82	-82

2-tone FFT Data at 115MHz with an 18dB Gain Stage

This is showing about -85dBc in the IM3 terms – very close to the ADC itself suggesting the input signal is much better. This is using an input interface that is only using 115mW on 3.3V.



ISL55210 Additional Features

Packaging and Pinout

- 16Lead QFN with backside ground holds very low internal T_j rise from ambient.
- Measured thermal impedance is only 63°C/W . For a 115mW internal dissipation this is only a 7°C rise above ambient – excellent long term reliability and extended high temperature range performance.
- Pinout duplicates the output pins on the input side of the package – this gives a very good layout for the R_g and R_f resistors.

Shutdown Characteristics

- The shutdown feature takes the typical supply current to 400uA. This is not zero as the internal circuitry is still active to hold the output pins close to the V_{cm} setting. This is intended to have a start up characteristic that does not require large voltage/current spikes to reach the nominal V_{cm} voltage at the outputs.

Overdrive Considerations

- The differential input pins include back to back low capacitance diodes that will limit the differential input voltage under large overdrive conditions and sink the input signal current through the two gain resistors. These act to limit large output signals under disable as well – protecting the ADC inputs.

Highest ESD ratings in the industry for this type of device.

ISL55210 Performance and Design in Summary

- Easy to use, very wideband, FDA with independent output V_{cm} .
- Lowest IM3 vs. quiescent power (115mW) for this type of FDA
- Even order distortion is now the limiting factor. Output side filter design can help this (and reduce integrated noise) with minimal insertion loss and no added quiescent power.
- Single ended to differential can be implemented using the ISL55210. Both DC coupled and AC coupled give excellent performance – app notes underway to describe these approaches and resulting performance.
- Fixed gain version, ISL55211, offers 3 possible gain settings – 2, 4 or 5V/V depending on input side pin connections. Fixed Bandwidth of approximately 1.4GHz at all gain settings.
- Combined amplifier + ADC daughterboards in development for customer application. Available by 3Q2011.

Detailed Converter Interface Design Articles

- 4 part series on Planet Analog, from April 2011
 - Part 1. Advantages to transformer input in a single to differential AC coupled application.
<http://www.eetimes.com/design/analog-design/4215415/Deliver-the-lowest-distortion-and-noise-in-a-low-power-wideband-ADC-interface-Part-1-of-4->
 - Part 2. Calculating integrated noise at the ADC for different filters and input pin SNR with the ADC for a net result
<http://www.eetimes.com/design/analog-design/4215416/Deliver-the-lowest-distortion-and-noise-in-a-low-power-wideband-ADC-interface-Part-2-of-4->
 - Part3. Distortion issues and combining SFDR at input pins with ADC for a net result
<http://www.eetimes.com/design/analog-design/4215417/Deliver-the-lowest-distortion-and-noise-in-a-low-power-wideband-ADC-interface-Part-3-of-4->
 - Part 4. Summary amplifier + ADC data on the Rev. A daughterboard and transformer modeling.
<http://www.eetimes.com/design/analog-design/4215418/Deliver-the-lowest-distortion-and-noise-in-a-low-power-wideband-ADC-interface-Part-4-of-4-Ecosystem=analog-design>