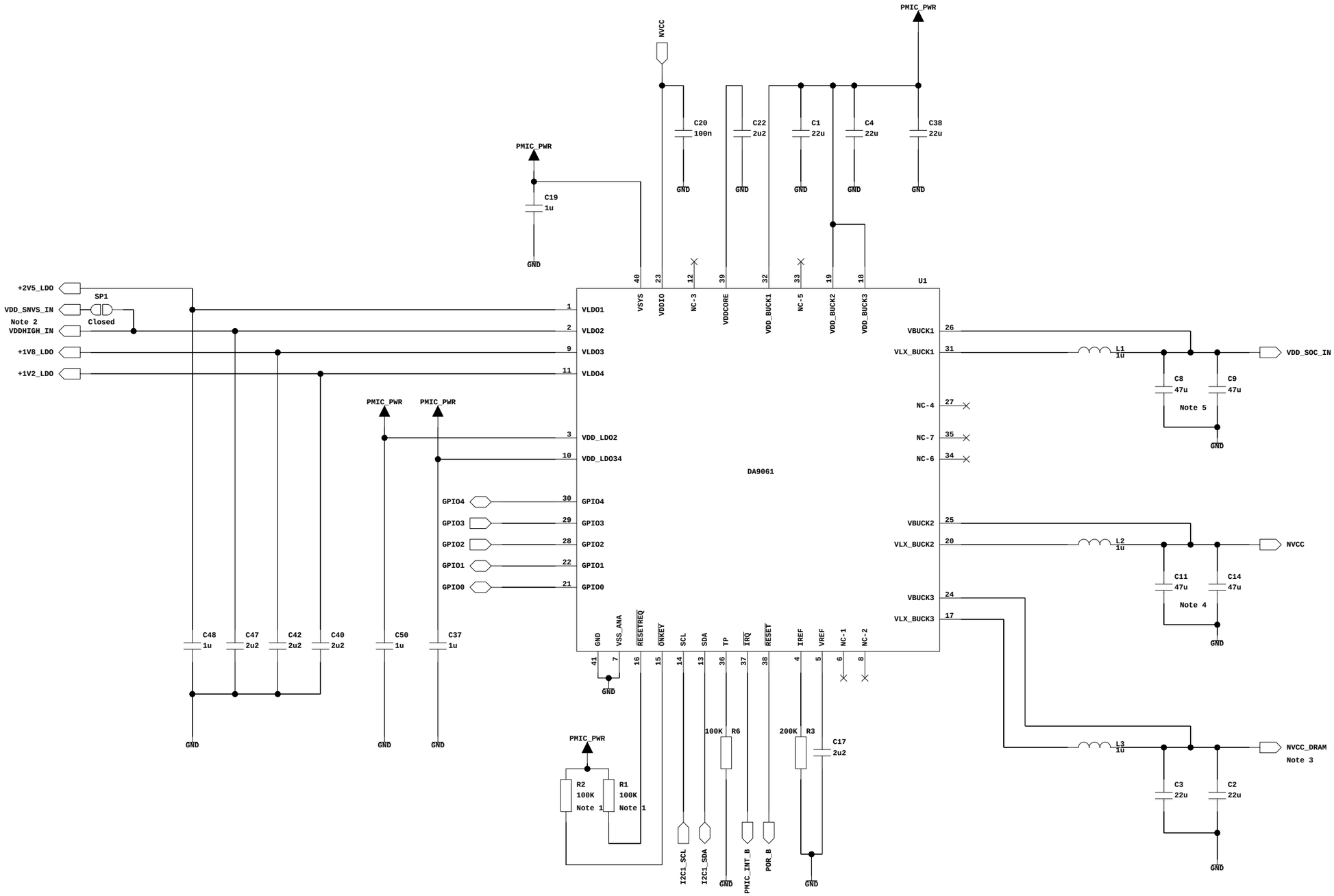

Notes:
[1] Can omit resistor and tie signal directly to PMIC_PWR to reduce BOM, but this will prevent access to these pins for flexibility / debug
[2] Switchable to 3V3 via GPIO3
[3] Switchable to 1V35 via GPIO2 to supply LV_DDR3
[4] Can replace with 2 x 22 uF when I_OUT < 1.5 A
[5] Can reaplce with 2 x 22 uF if I_OUT < 1.25 A and register control BUCK1_FCM = 0

SCHEMATIC TEMPLATE REV.xDxD_V7 (01-06-2017)

DESIGNED BY: TG <Designed by 2>

REVIEWED BY: N/A <Reviewed by 2>

SIZE: A3L

TITLE: DA9061 i.MX 6UL \ 6ULL

VARIANT: N/A

SAVED DATE: 18/10/2017:17:02

REVIEWED DATE: 18/10/2017

DA9061_6UL 1000
BOARD No. Sch Rev Variant No. Var Rev

DRAWING No:

SHEET NAME: DA9062

PAGE: 1 of 2

dialog SEMICONDUCTOR

REVISION TABLE

REV.	DATE	ENGINEER	NOTES
1.0	18/10/2017	TG	

MECHANICAL PARTS

SCHEMATIC TEMPLATE REV.xDxD_V7 (01-06-2017)

DESIGNED BY: TG <Designed by 2>

REVIEWED BY: N/A <Reviewed by 2>

SIZE: A3L

TITLE: DA9061 i.MX 6UL \ 6ULL

VARIANT: N/A

SAVED DATE: 18/10/2017:16:56

REVIEWED DATE: 18/10/2017

DRAWING No: DA9061_6UL1000 (BOARD No. / Sch Rev / Variant No. / Var Rev)

SHEET NAME: REVISION/MECHANICAL

PAGE: 2 of 2

dialog SEMICONDUCTOR