

3P3VDD32KA
Vdd from uProc
for 32KHz input.

Required to limit power
BT1 BATTERY CR2032
C21 10uF
TCS_VBAT

USE RESISTOR TO REDUCE XTAL
DRIVE POWER TO 50 uW IF
NECESSARY.
OTHER WISE USE 0 OHM RESISTOR.

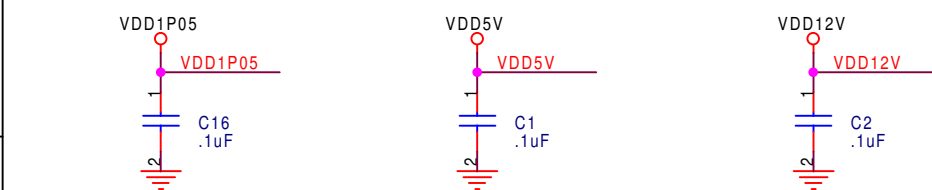
- VDD1P05 4
- 3P3VDD24M 7
- 3P3VDD27M 10
- 3P3VDD25MB 13
- 3P3VDD3P3 21
- 3P3VDD32KA 22
- 3P3VDDTS 26
- 3P3VDD32KB 29
- TCS_VBAT 30

- SMBUS_DAT 18
- SMBUS_CLK 17
- TCS_TCH 15
- TCS_TSDP2 1
- TCS_TSDN2 2
- TCS_TSDP1 31
- TCS_TSDN1 32
- TCS_PWRGD 14

- TCS_PWRGD
- SMBUS_DAT
- SMBUS_CLK
- SMBUS_ALERT#
- TCS_FLT#

Do not use multiple
pull-up resistors on
SMBus signals.
Use 27K pull-up on ALERT#

VDD3P3
SIG_BEAD
TOTAL IDD
= 200 MA

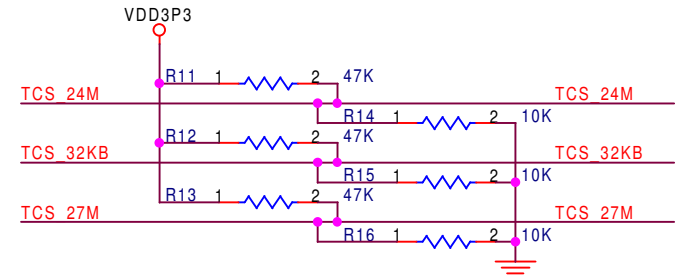


- Layout notes.
1. Separate Xout and Xin in traces by 3 x the trace width.
 2. Do not share crystal load capacitor ground via with other components.
 3. Ground C10 and C11 to U1 pin 29.
 4. Route power from bead through bulk capacitor pad then through 0.1 uF capacitor pad then to clock chip Vdd pad.
 5. Do not share ground vias. One ground one ground via.

NOTE:FERRITE BEADS =

Manufacture	Part Number	Z@100MHz	PkgSz	DC res.	Current (Ma)
muRata	BLM21A601R	600	0805	0.30	600
TDK	MMZ2012S601A	600	0805	0.30	600
STEWART	HZ0805E601R	600	0805	0.30	600
AssocCmpTch	CBG0805-600-50	600	0805	0.30	600

Manufacture	Part Number	Z@100MHz	PkgSz	DC res.	Current (Ma)
muRata	BLM18AG601SN1	600	0603	0.50	200
muRata	BLM18BD601SN1_PB	600	0603	0.65	200
Ceratech	HB-1T1608-601	600	0603	0.50	200
TDK	MMZ1608R301A	300	0603	0.20	500



Molex pn for server and desktop fan
47053-1000 47054-1000

Integrated Device Technology
San Jose, CA

Title: REFERENCE SCHEMATIC

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Date: Tuesday, October 04, 2011 | Sheet: 1 of 1