To our customers,

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April 1st, 2010
Renesas Electronics Corporation

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RENESAS

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# Diode

## Variable Capacitance Diodes

## 1. Characteristics of Variable Capacitance Diodes

### 1.1 About Variable Capacitance Diodes

Variable capacitance diodes, take advantage of the fact that the capacitance of the diode PN junction varies with the applied reverse bias voltage. This differs from other diodes, such as rectifying diodes and switching diodes, which use the rectifying effect of the PN junction, or current regulation diodes, which take advantage of zener breakdown or avalanche breakdown.

In the past, variable capacitance diodes have been used for AFT and AFC in TV, FM, and other tuners, and in FM modulators. At present, however, variable-capacitance diodes are most commonly used as tuning elements.

Recently, due to their adoption in new media applications such as car navigation systems, personal computers, and digital broadcasting, demand is increasing for more compact tuners offering improved performance. In particular, the market for portable communications equipment centered on mobile phones is growing rapidly, and large numbers of variable capacitance diodes are used in the VCO (voltage controlled oscillator) circuits in these products.

#### 1.1.1 Basic Operating Principle

When a reverse bias is applied to a PN junction, a depletion layer, a layer in which there are no free electrons, is formed. The width of this layer is proportional to the applied reverse bias. The junction capacitance is lower when the depletion layer is wider, and higher when it is narrower. In other words, in variable capacitance diodes, the width of the depletion layer changes with changes in the reverse bias voltage (VR). These diodes make use of the resulting changes in the junction capacitance.

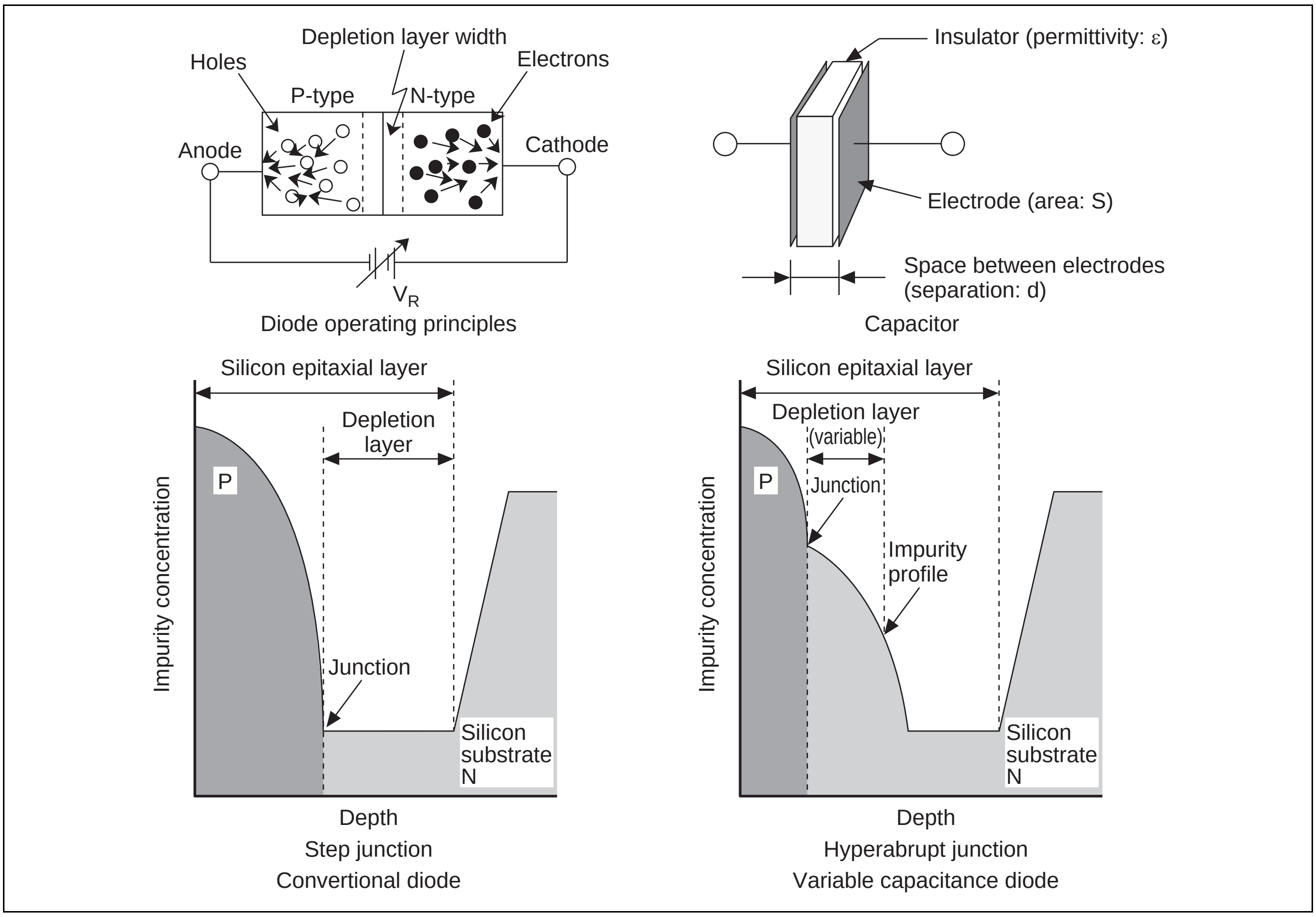



**Figure 1.1 Operating Principles**

As shown in figure 1.1, the capacitance, C, of a capacitor is given by the following formula.

$$C = \frac{\varepsilon \cdot S}{d}$$

S: Junction area, ε: Depletion layer permittivity, d: Depletion layer width

The junction capacitance of a variable capacitance diode can be expressed by the same formula as that used for the capacitance of a capacitor. In addition, changes in the capacitance depend on the impurity concentration, as illustrated in figure 1.1. Special techniques are used in the fabrication process to introduce the desired impurity concentration.

### 1.1.2 Variable Capacitance Diode Characteristics

The diode reverse direction region (saturation region) is a region in which current does not flow. This region has a capacitance component, allowing the diode to be used as a capacitor.

Variable capacitance diodes are used in tuning circuits formed from the diode capacitance (C) and the inductance (L) of a coil. The tuning frequency (f) is given by the following formula.

$$f = \frac{1}{2\pi\sqrt{C \cdot L}}$$

The tuning frequency (f) can be changed by changing the capacitance (C) with the applied voltage, a feature of this type of diode. This means that the desired tuning frequency can be achieved by controlling the voltage applied to the diode.

In addition, variable capacitance diodes are available with a variety of specific characteristics, such as capacitance value and variation ratio, to match different frequency and frequency range requirements.

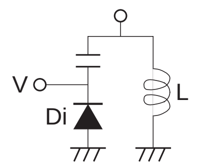



**Figure 1.2 Tuning Circuit**

## 1.2 Process C

Renesas has superseded the earlier process for fabricating variable capacitance diodes (process B) with process C, which yields more optimal results. In particular, process C provides uniform voltage-capacitance (CV) characteristics and a large capacitance variation ratio, allowing for an expanded range of reception frequencies. Additional advantages include low series resistance and a superior performance index (figure 1.3).

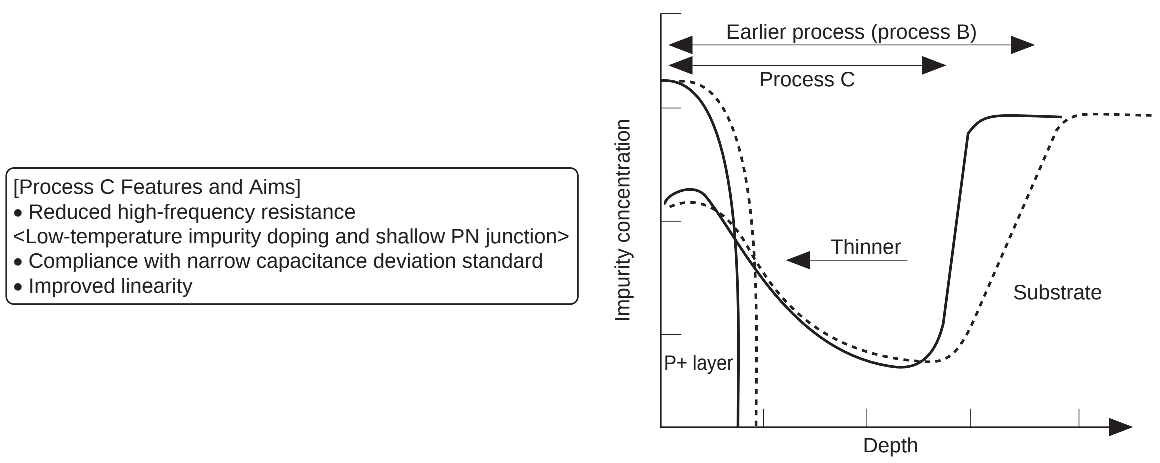



**Figure 1.3 Process C Features and Impurity Profile Comparison**

Note: Process C is adopted as a standard process technology also to the products of RKV-type no.

## 2. Variable Capacitance Diode Application Examples

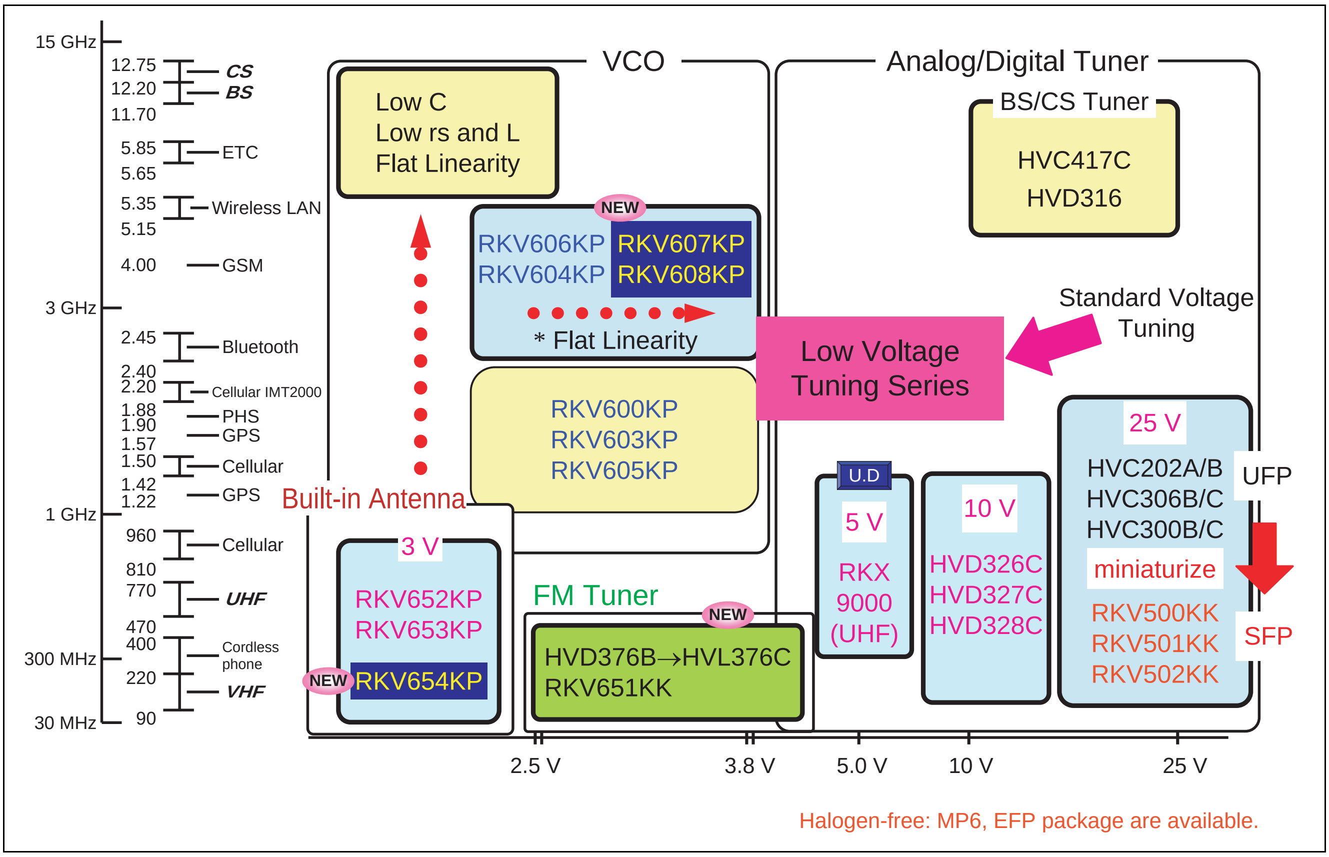



**Figure 2.1 High Frequency Vari-Cap Diode Products Road Map**

## 3. Variable Capacitance Diode Structure

### 3.1 Chip Cross-Sectional Structure

As shown in figure 3.1 high-quality single-crystal silicon is used for variable capacitance diodes, and silicon epitaxial planar pellets are employed to ensure a high level of reliability.

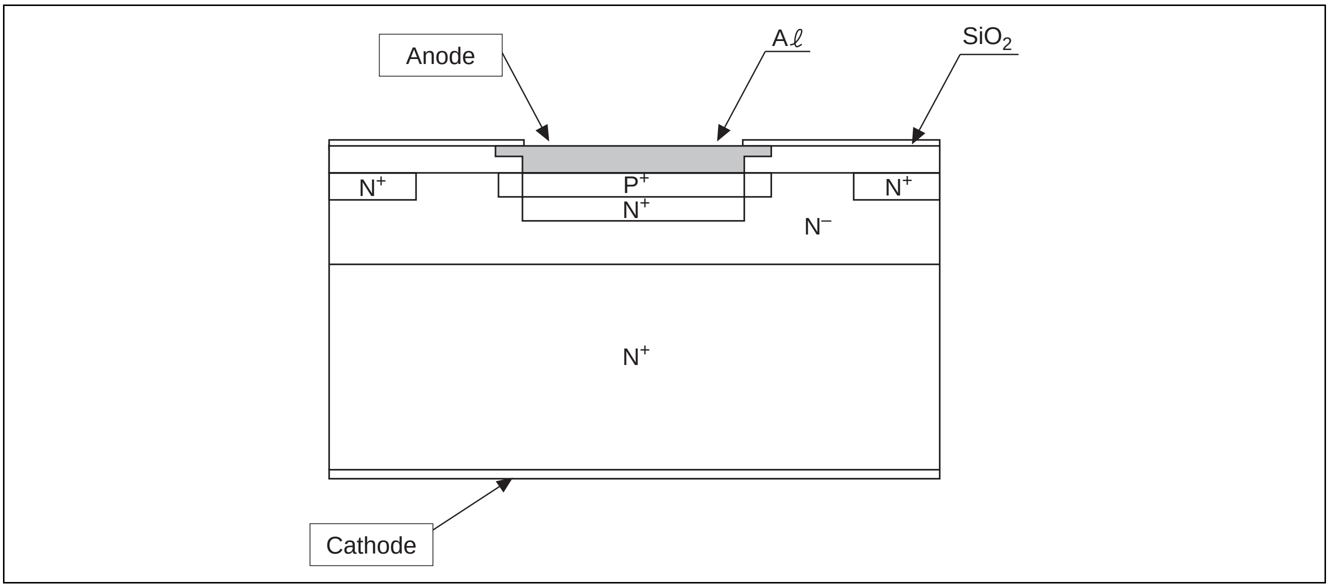



**Figure 3.1 Chip Cross Section**

### 3.2 Assembly Structure

Variable capacitance diodes are available in URP, UFP, SFP, EFP, MPAK, and CMPAK-4 packages.
(See figure 3.2 to figure 3.5.)

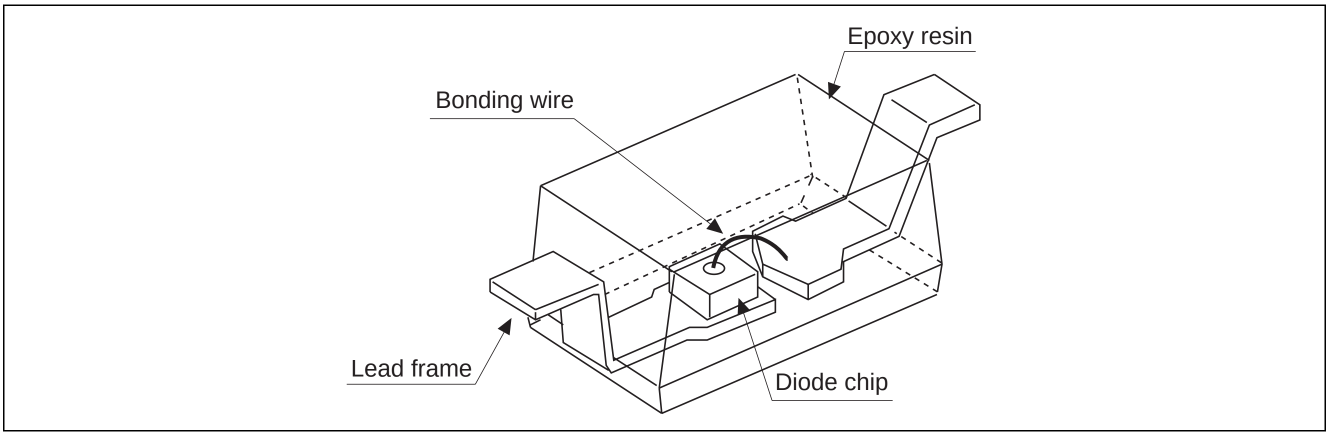



**Figure 3.2 URP Package Structure**

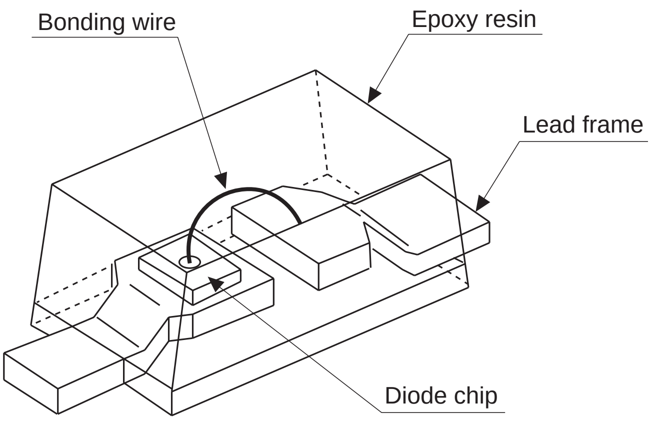



**Figure 3.3 UFP, SFP, and EFP Package Structure**

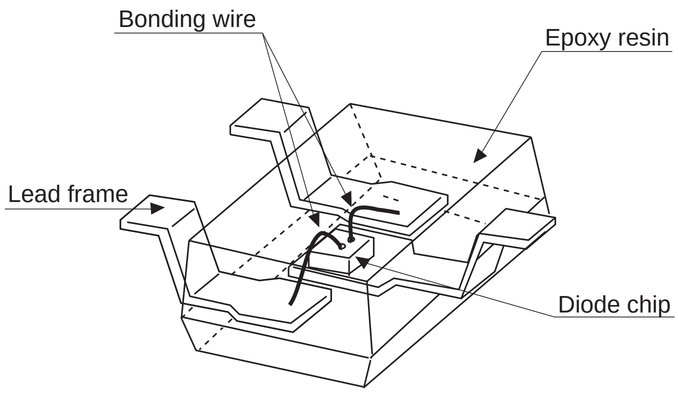



**Figure 3.4 MPAK Package Structure**

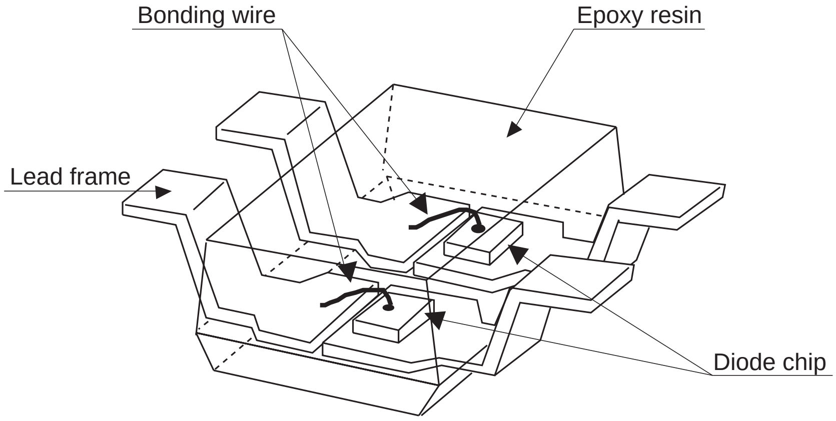



**Figure 3.5 CMPAK-4 Package Structure**

## 3.3 Trend in Packages

Portable equipment, such as mobile phones, is becoming thinner and offering a greater range of functions. As a result, there is a need for thinner electronic devices for use in modules such as VCO and antenna switches.

Renesas mass-produces variable capacitance diodes in the EFP (Extremely small Flat Package, Renesas package code, maximum external dimensions 0.8 × 0.6 × 0.5 mm) package, using the smallest lead pin type (1006). Furthermore, the MP6 (Micro Package 6) is provided as the package with the smallest external form (body size in mm: 0.6 × 0.3 × 0.3) as a response to the increasing trend towards ultra-slim electronic devices. The electrodes are arranged on the bottom of the package, so the MP6 is capable of reducing mounting areas by 70% as a measure for smaller and thinner embedded equipment.

Renesas is committed to offering electronic devices providing excellent performance in extremely compact packages.

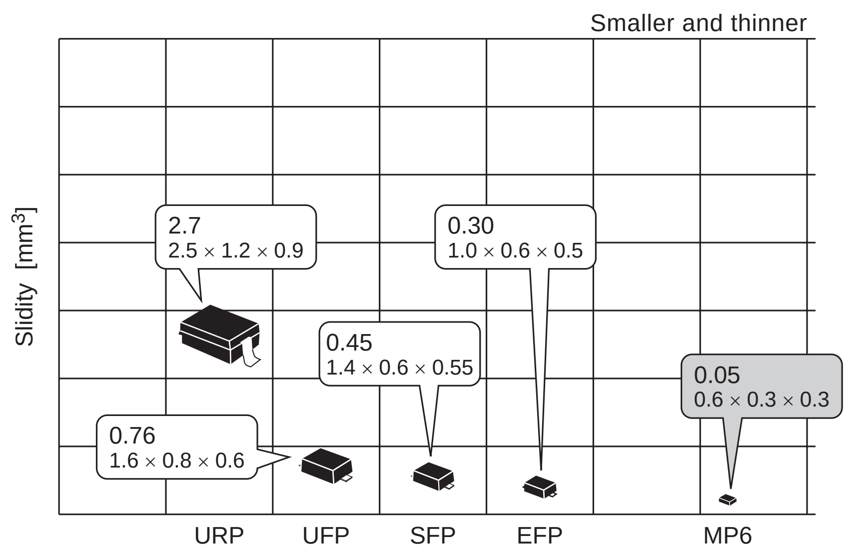
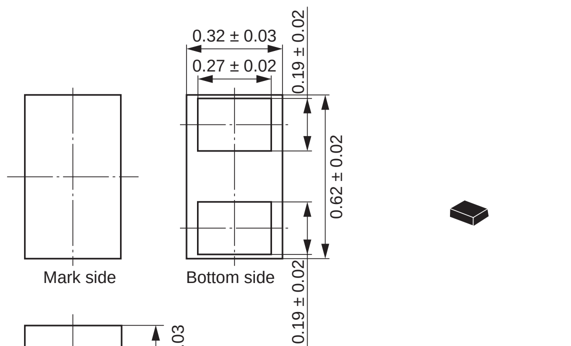



**Figure 3.6 Trend in Packages**

## 3.4 Package Dimensions

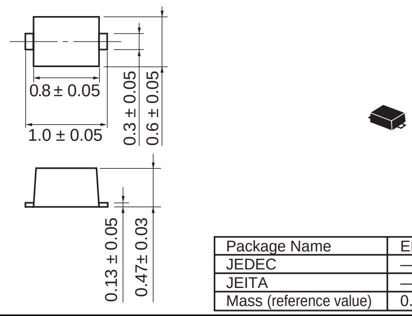
Unit: mm

MP6




| Package Name | MP6 |
|---|---|
| JEDEC | — |
| JEITA | — |
| Mass (reference value) | 0.00015 g |

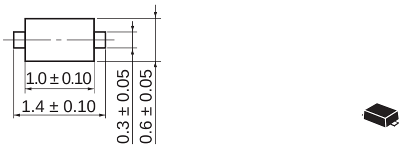
EFP

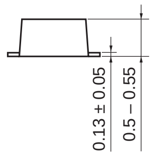



| Package Name | EFP |
|---|---|
| JEDEC | — |
| JEITA | — |
| Mass (reference value) | 0.0007 g |

Unit: mm

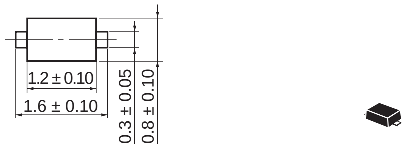
## SFP

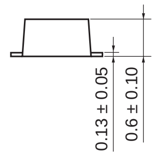



| Package Name | SFP |
|---|---|
| JEDEC | — |
| JEITA | — |
| Mass (reference value) | 0.0010 g |

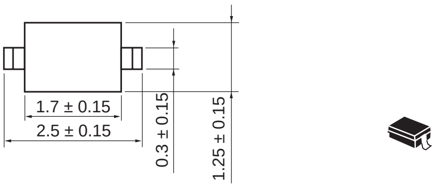
## UFP

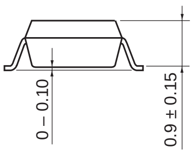



| Package Name | UFP |
|---|---|
| JEDEC | — |
| JEITA | Conforms |
| Mass (reference value) | 0.0016 g |

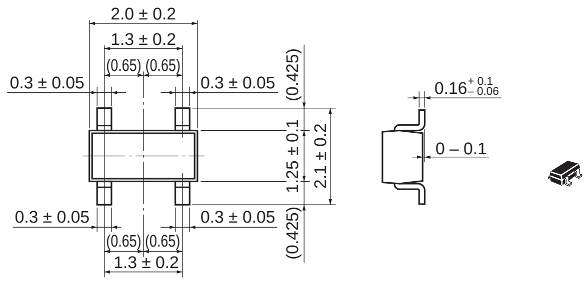
## URP

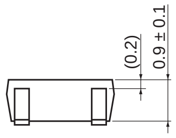



| Package Name | URP |
|---|---|
| JEDEC | Conforms |
| JEITA | — |
| Mass (reference value) | 0.004 g |

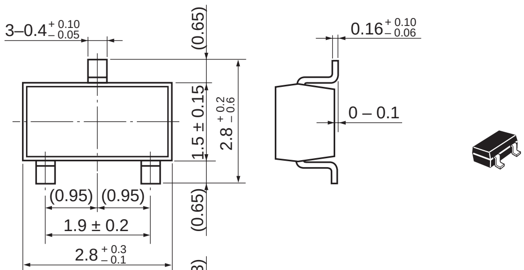
## CMPAK-4

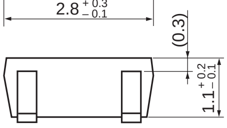



| Package Name | CMPAK-4 |
|---|---|
| JEDEC | — |
| JEITA | Conforms |
| Mass (reference value) | 0.006 g |

## MPAK



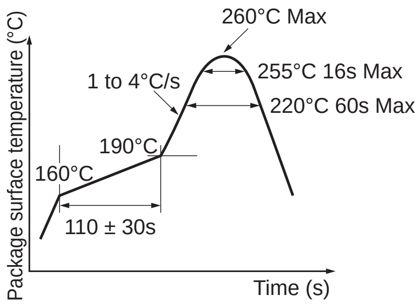
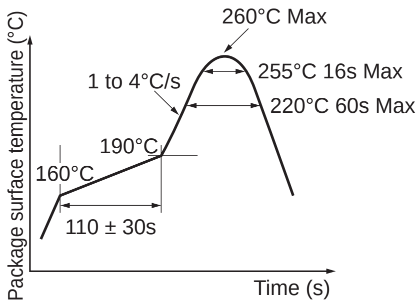

| Package Name | MPAK |
|---|---|
| JEDEC | — |
| JEITA | Conforms |
| Mass (reference value) | 0.011 g |

# 4. Soldering

## 4.1 Temperature Profile Example

### 4.1.1 Conditions for Using the Reflow Soldering Method

**Table 4.1 Soldering Conditions for the Diode Packages**

<table>
<tr><td>Lead plating</td><td colspan="2">Sn-Pb</td><td colspan="2">Sn-Bi, Sn-Cu</td></tr>
<tr><td>Solder paste</td><td>Eutectic alloy<br>of Sn-Pb</td><td>Sn-Ag</td><td>Eutectic alloy<br>of Sn-Pb</td><td>Sn-Ag</td></tr>
<tr><td>Package surface temperature (upper limit)</td><td>Peak: 260°C<br>220°C or higher for no more than 60 s</td><td colspan="3">Peak: 260°C<br>220°C or higher for no more than 60 s</td></tr>
<tr><td>Temperature profile</td><td></td><td colspan="3"></td></tr>
</table>

### 4.1.2 Flow-Soldering Conditions (URP, CMPAK-4, and MPAK)

Soldering Conditions for flow soldering are shown below.

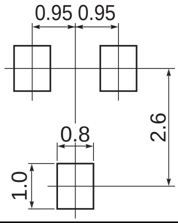
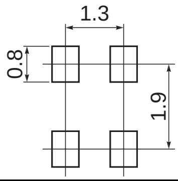
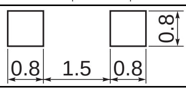
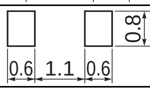
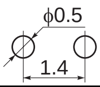
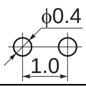
**Table 4.2 Soldering Conditions for Flow Soldering**

| Item | | Condition | Upper Limit | Applicability |
|---|---|---|---|---|
| Preheating | Temperature | 80 to 150°C | — | Substrate surface |
| | Time | 1 to 3 minutes | | |
| Solder dip | Temperature | 230 to 250°C | 260°C | Temperature of the solder layer |
| | Time | 2 to 4 s | 10 s | Time taken to pass through the solder layer |

## 4.2 Footprint of Surface-Mounted Diodes

Table 4.3 lists example soldering conditions for surface-mounted diodes.

**Table 4.3 Example Soldering Conditions for Surface-Mounted Diodes**

| Item / Package | Footprint (land) Dimensions | Cream Solder Thickness |
|---|---|---|
| MPAK |  | 0.15 to 0.30mm |
| CMPAK-4 |  | 0.15 to 0.30mm |
| URP |  | 0.15 to 0.30mm |
| UFP |  | 0.15 to 0.30mm |
| SFP |  | 0.15 to 0.30mm |
| EFP |  | 0.15 to 0.30mm |

Notes: 1. Footprint (land) dimensions are given in millimeters (mm).
2. Cream solder thickness values are examples using reflow mounting.

# 5. Variable Capacitance Diode Continuous Taping Method (C.C. Method)

## 5.1 Renesas C.C. Method

In order to avoid tracking error within the operating frequency band in electronic tuner front-end circuitry, and the like, variable capacitance diodes used are sorted into groups based on their voltage-capacitance characteristics (C-V curve). It is necessary to limit the capacitance deviation (ΔC/C) to no more than a few percentage points, within the specified bias range required by the tuner characteristics.

Renesas has introduced the C.C. (continuous connected taping system) method for grouping variable capacitance diodes. It is described below.

## 5.2 Grouping with the Renesas C.C. Method

Variations in the characteristics of semiconductor devices can be caused by inconsistencies in the materials or production processes used. However, chips that were located next to one another on the silicon wafer during the fabrication process exhibit nearly identical characteristics. Thus, if chips from adjacent positions on the silicon wafer are assembled sequentially and then affixed to a tape, it is possible to perform grouping in a continuous manner. This is how the C.C. method works.

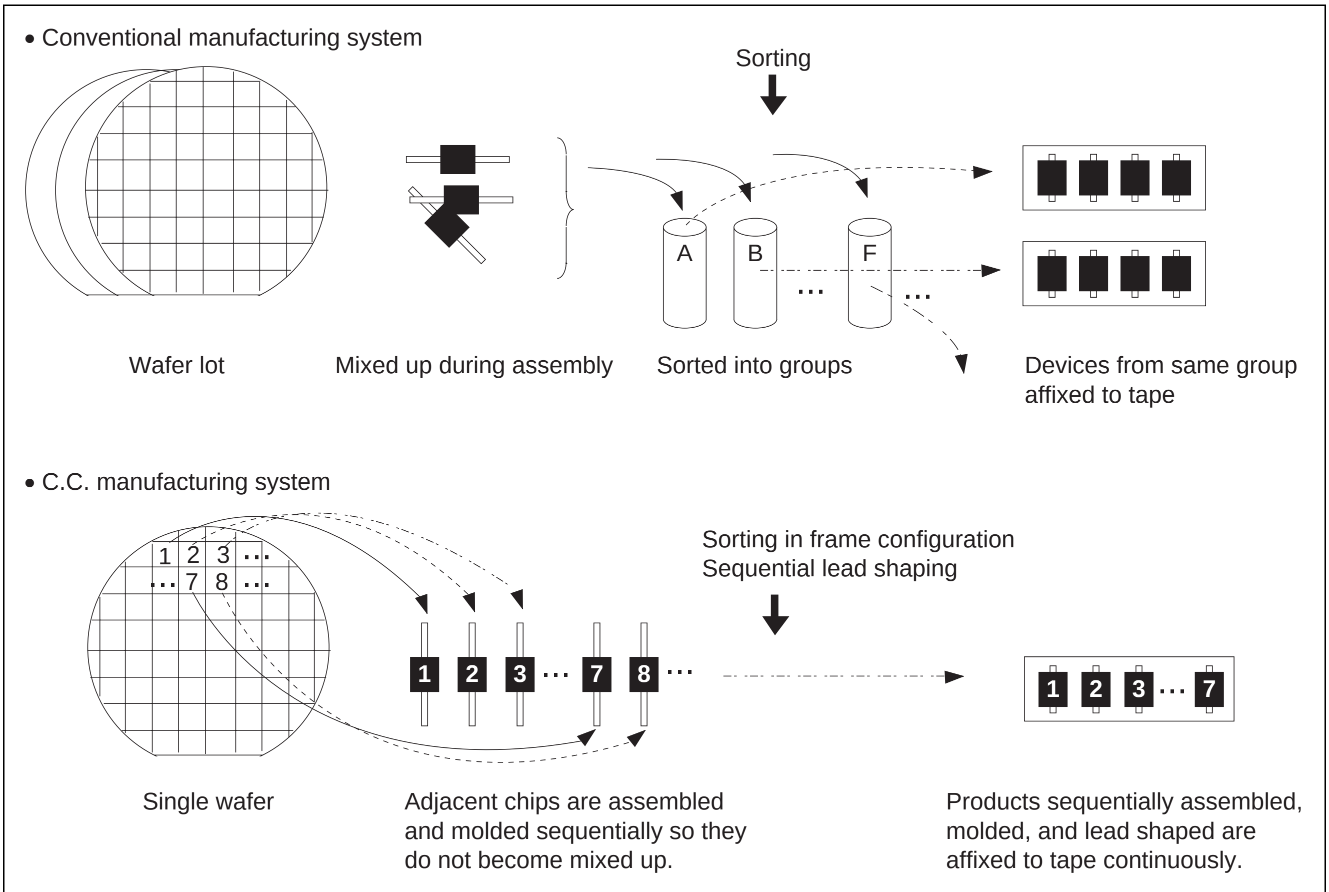
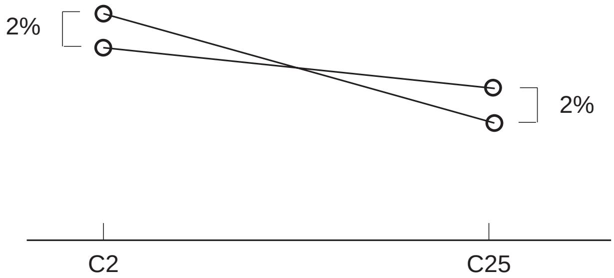
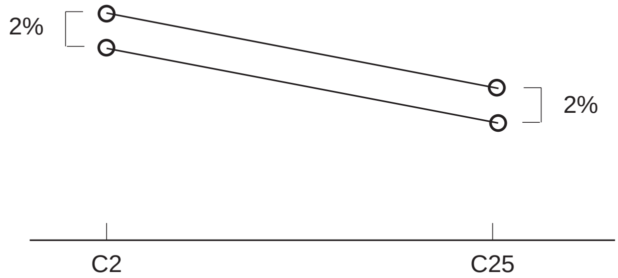



**Figure 5.1 Differences Between Systems Using Conventional Method and Renesas C.C. Method**

**Table 5.1 Differences Between Characteristics of Conventional Method and Renesas C.C. Method**

| Conventional Method | Renesas C.C. Method |
|---|---|
| Poor parallelism of C-V curves<br><br><br>For example, if ΔC/C is 2%, products with a cross-curve like that shown above may be present. | Good parallelism of C-V curves<br><br><br>For example, even if ΔC/C is 2%, the C-V curves will be in parallel as shown above. Thus, good tuner tracking characteristics are assured. |
| <u>High ΔC/C value</u><br>Due to the way the chips are sorted, there will be a distribution within the selection setting range. | <u>Low ΔC/C value</u><br>Chips that were next to each other on the silicon wafer are adjacent to each other on the tape, thereby minimizing variations. |
| <u>Many groups (breaks in continuity) per reel</u><br>Since the chips are sorted afterward, the quantity per group is small. This means that more groups will be included in each reel. | <u>Few groups (breaks in continuity) per reel</u><br>The continuous system minimizes breaks in continuity within individual reels, resulting in improved mounting efficiency during use (because the mounting machine does not need to be stopped as frequently). |

## 5.3 Renesas C.C. Method Tape Specifications

The main specifications are indicated below.

(1) Ten devices with continuous random ΔC/C are guaranteed. (However, the number of continuous devices differs depending on the product.)

(2) The two tape arrangements shown below are available.

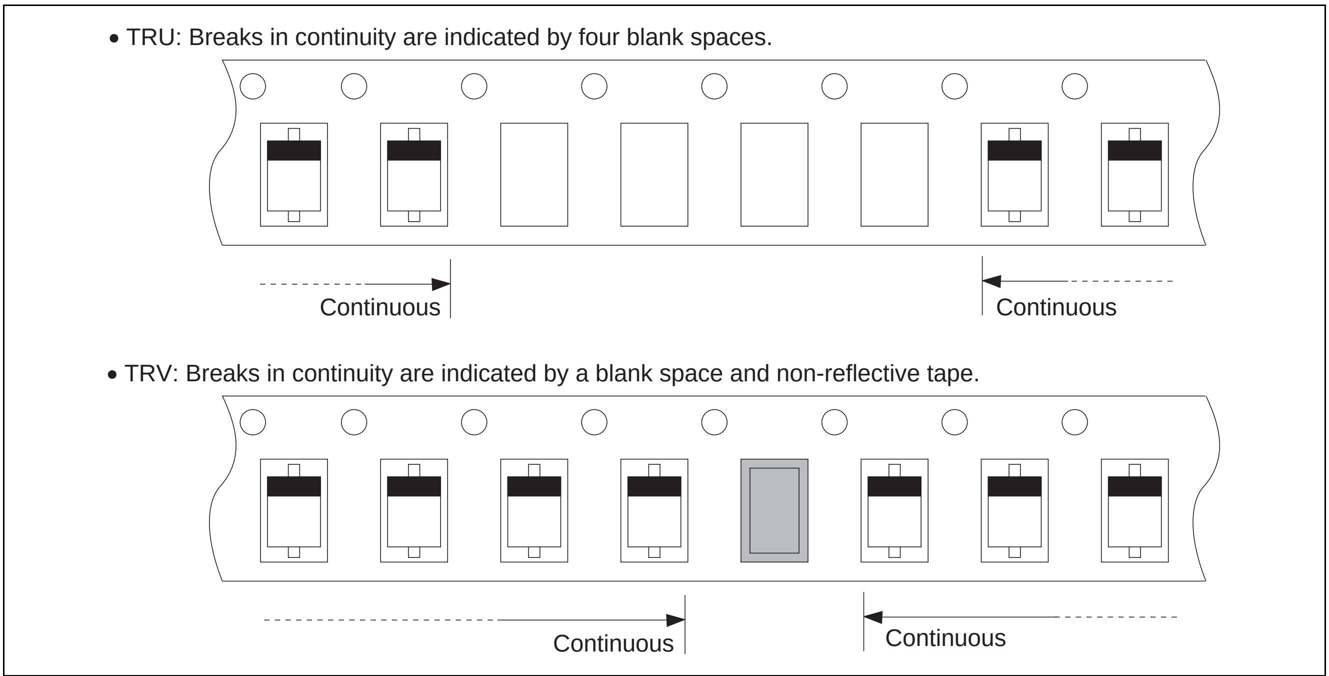



**Figure 5.2 Renesas C.C. Method Taping Specifications**

## 6. Specifications and Characteristics

### 6.1 Variable Capacitance Diodes for VCO (1)

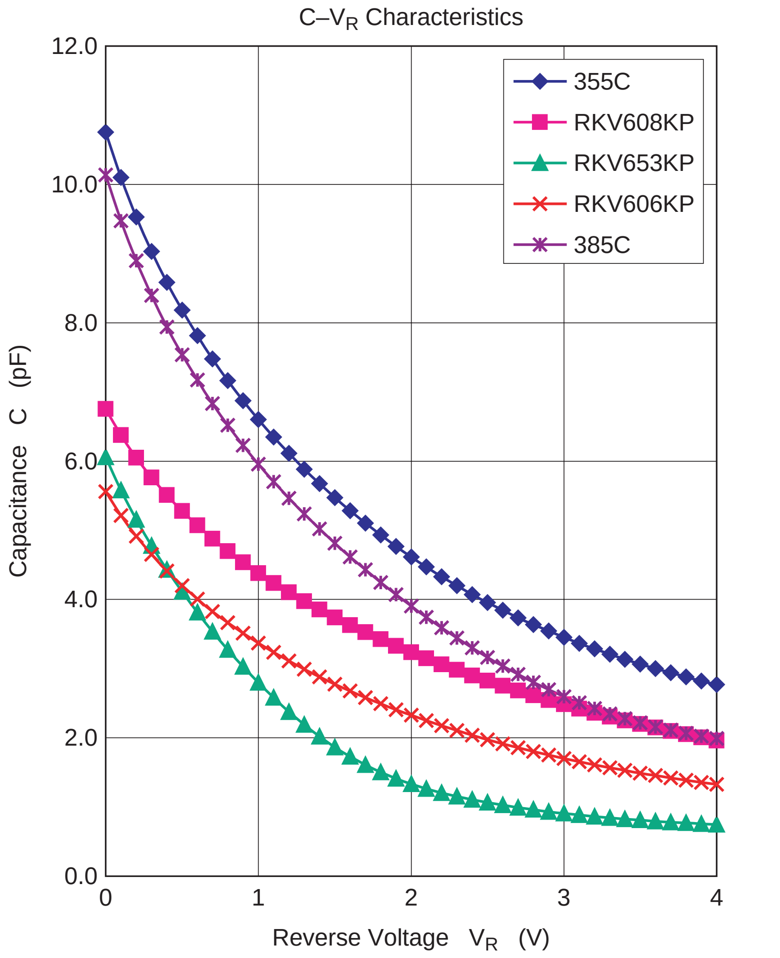



**Figure 6.1 Variable Capacitance Diodes for VCO (1)**

## 6.2 Variable Capacitance Diodes for VCO (2)

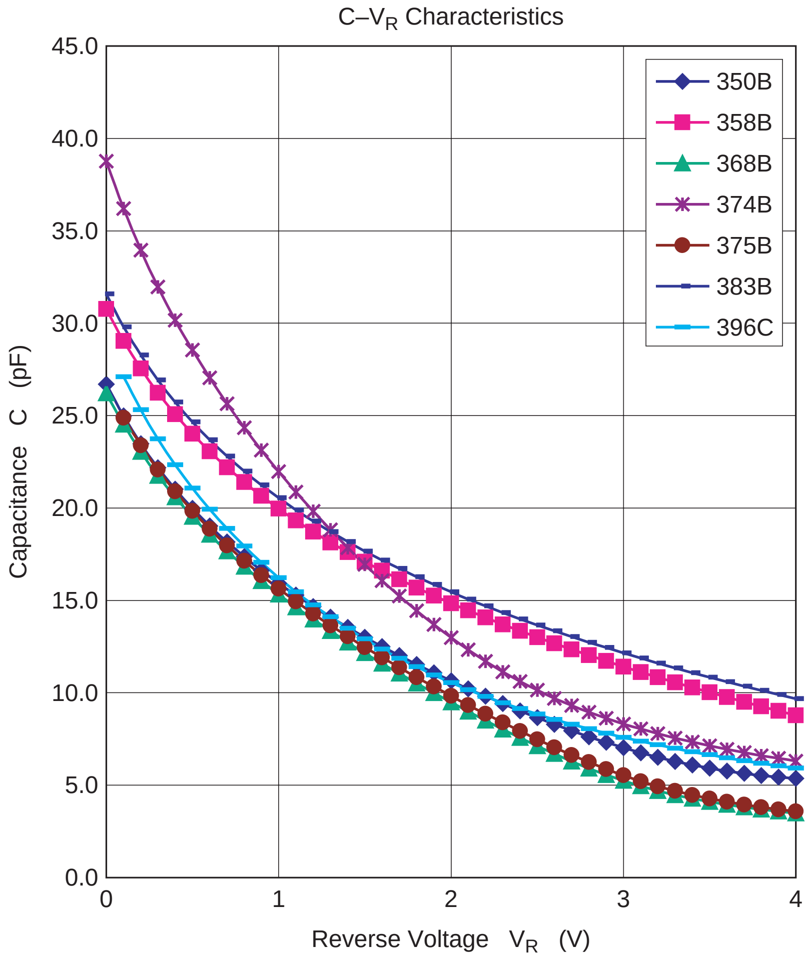



**Figure 6.2 Variable Capacitance Diodes for VCO (2)**

## 6.3 Variable Capacitance Diodes for VCO (3)

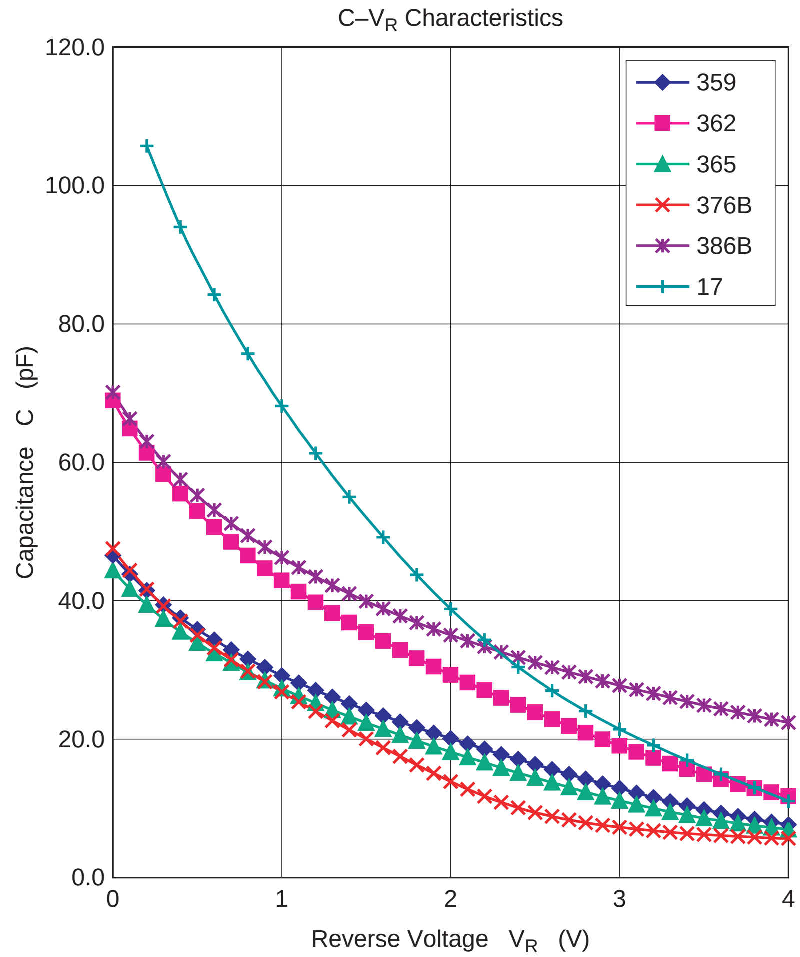



**Figure 6.3 Variable Capacitance Diodes for VCO (3)**

## 6.4 Variable Capacitance Diodes for Tuner (1)

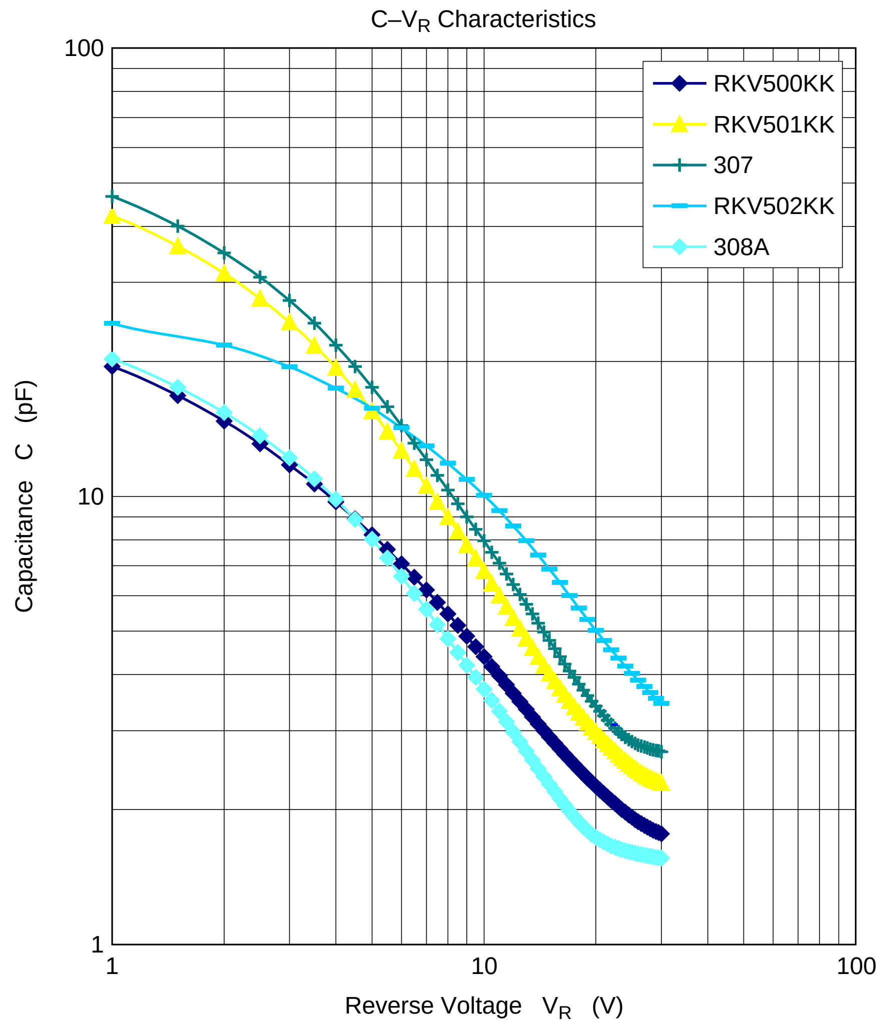



**Figure 6.4 Variable Capacitance Diodes for Tuner (1)**

## 6.5 Variable Capacitance Diodes for Tuner (2)

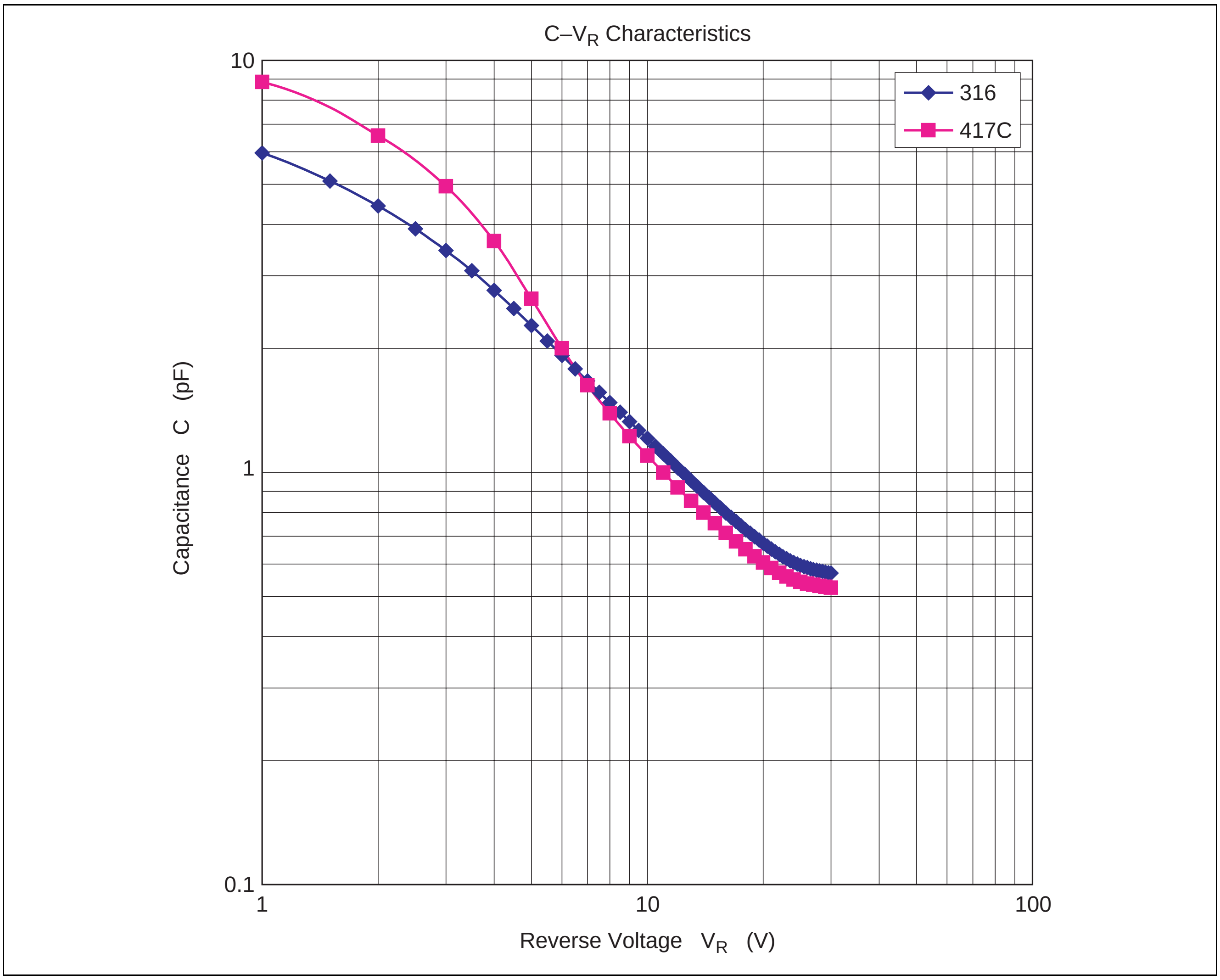



**Figure 6.5 Variable Capacitance Diodes for Tuner (2)**

## 6.6 Variable Capacitance Diodes for Tuner (3)

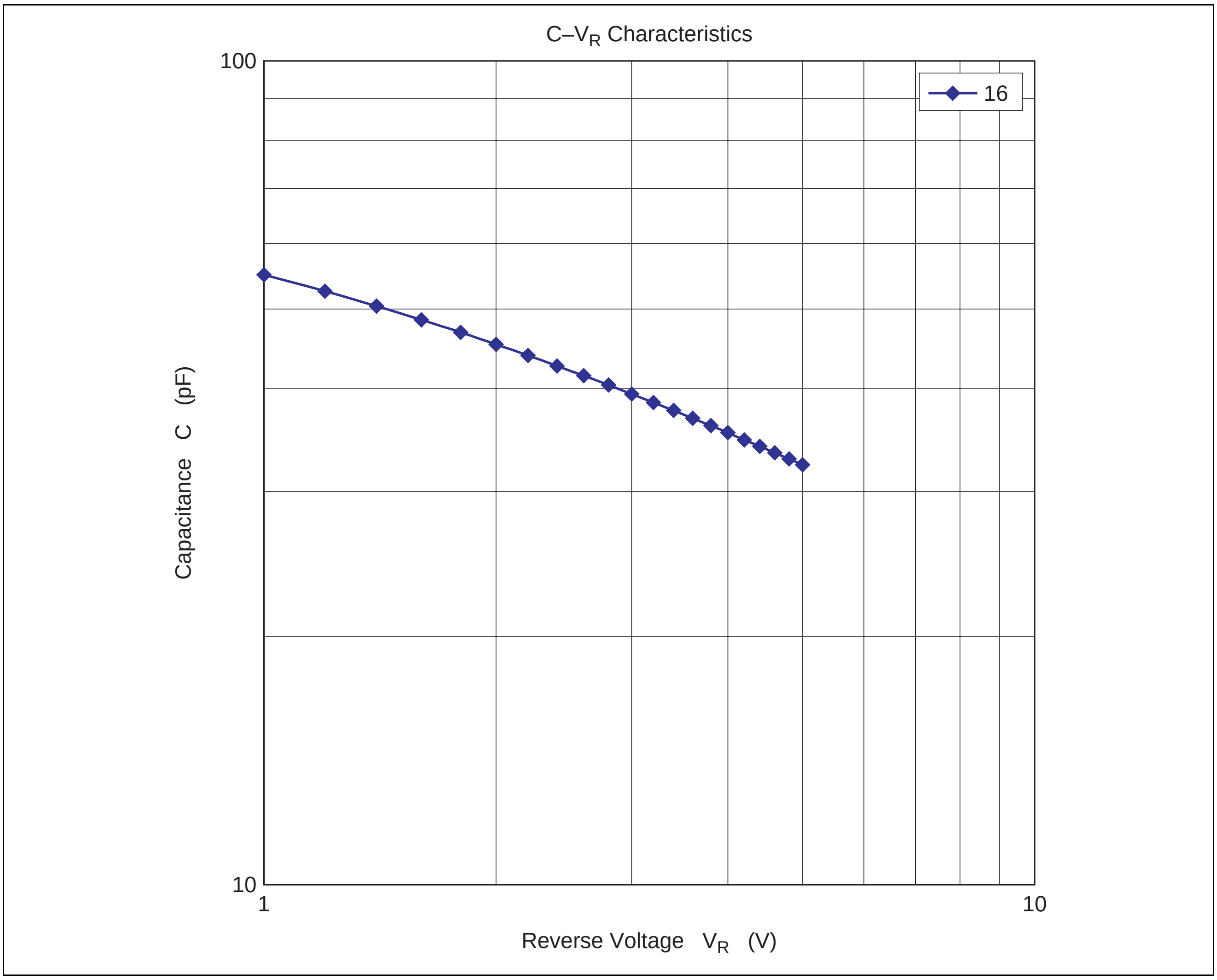



**Figure 6.6 Variable Capacitance Diodes for Tuner (3)**

## Website and Support

Renesas Technology Website
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