IDT®
Converting Designs from PLX PEX 8114 to IDT Tsi384

Application Note

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1. Converting Designs from PLX PEX 8114 to IDT Tsi384

This document explains the hardware differences between the PLX PEX 8114 and the IDT Tsi384. It is intended for anyone interested in converting designs based on the PEX 8114 to the Tsi384. The following topics are discussed:

Revision History

80E1000_AN001_04, Formal, August 2009

This version of the document does not include any technical changes.

80E1000_AN001_03, Formal, September 2007

This version includes a new section that discusses power supply differences between the two devices (see "VDD33 Power on Pin P12").

80E1000_AN001_02, Formal, December 2006

This version was revised to indicate guidelines for converting from only the PLX PEX 8114 to the IDT Tsi384. Multiple PEX devices was indicated in the previous version.

80E1000_AN001_01, Formal, November 2006

This is the first release of the document.

1.1 Overview

The Tsi384 is pinout and package compatible with the PLX PEX 8114 (PEX 8114) PCI Express®-to-PCI/X bridge for forward-bridging applications. The Tsi384 can be used as a drop-in replacement for the PEX 8114, taking into account the design considerations outlined in the following section.

The Tsi384 and PEX 8114 are available in a 256-pin BGA package with similar mechanical parameters that allow both devices to be soldered onto a common footprint on the system board.

1.2 Pin Compatibility

Table 1 shows the pin differences between the two devices, as well as any design implications caused by these differences. The Tsi384 is intended to drop into existing PLX sockets without the need to modify the existing layout or to add additional components. Any design changes due to the implications in the table are expected only to affect components used to change the power supply from 1.0V to 1.2V.

Table 1: Signal Differences

Pin Number	Signal Name		Tsi384 Design Implications
	PEX 8114	Tsi384	
E4	PCI_IDSEL	NC	None. The Tsi384 operates only as a forward bridge.
L13	EE_PR#	NC	None. The PEX 8114 supports this active-low input to indicate that a serial EEPROM is present. The Tsi384 does not require this input.
M13	HP_PWRLED#	NC	None. The Tsi384 supports the forward bridging function. These signals are not required when operating as a forward bridge. The PEX 8114 uses these signals for an internal hot plug controller when operating in reverse transparent mode only.
N13	HP_PWRFLT#	NC	
N14	HP_PWREN#	NC	
P13	HP_PRSNT#	NC	
P14	HP_PERST#	NC	
R13	HP_MRL#	NC	
R14	HP_CLKEN#	NC	
T13	HP_BUTTON#	NC	
T14	HP_ATNLED#	NC	
P15	STRAP_TRAN	NC	None. The PEX 8114 uses this pin to select Transparent or Non-transparent mode at power-up. The PEX 8114 powers up as a transparent bridge by default. The Tsi384 does not use a power-up option to select this mode; it is done through software. The Tsi384 defaults to transparent operation at power-up.
P16	STRAP_FWD	TEST_BIDR_CTL	None. The Tsi384 operates only as a forward bridge.
P12	VDD33	VDDA_PCIE	Tsi384 requires a low noise 3.3V supply on this pin.
E6, E8, E9, E11, F5, F12, G5, G12, J5, J12, K5, K12, M6, M10, M12	VDD10	VDD	The Tsi384 requires a 1.2V core supply voltage on its VDD inputs, while the PEX 8114 uses a 1.0V core supply voltage on its VDD10 inputs.

Table 1: Signal Differences *(Continued)*

Pin Number	Signal Name		Tsi384 Design Implications
	PEX 8114	Tsi384	
M8	VDD10A	VDDA_PLL	The Tsi384 requires a 1.2V analog supply voltage on its VDDA_PLL input, while the PEX 8114 uses the VDD10A (1.0V) as its SerDes analog supply input. PLX-based designs should have the VDD10A input filtered as indicated in the PEX 8114 reference design. The same filter used in the PLX design for the VDD10A input can be used for the Tsi384 VDDA_PLL input with no modifications.
P8, R4, R6, R8, R10, R12	VDD10S	VDD_PCIE	The Tsi384 requires a 1.2V supply voltage on its VDD_PCIE inputs, while the PEX 8114 uses a 1.0V supply voltage on its VDD10S inputs.
T6	VTT_PEX[0]	NC	None. The PEX 8114 requires a separate external 1.5V termination voltage for proper SerDes termination. The Tsi384 does not require this termination as it is done internally. The corresponding Tsi384 pins are no connects.
T10	VTT_PEX[1]	NC	

1.2.1 VDD33 Power on Pin P12

On the PEX 8114, P4 and P12 are supplied with separate power rails. On the Tsi384, however, P4 and P12 must be supplied with a common filtered 3.3V rail.

Table 2: 3.3V Pin Differences

Pin Number	Signal Name	
	PEX 8114	Tsi384
P4	VDD33A	VDDA_PCIE (3.3V)
P12	VDD33	VDDA_PCIE (3.3V)

In an existing PEX 8114 design, P4 should be supplied with a filtered 3.3V source, but P12 does not require filtering. VDD33 is used for PCI I/O buffers and is expected to be noisy when the PCI bus I/Os are used. When the Tsi384 is installed in an existing PEX 8114 design, P4 and P12 internally bridge the filtered 3.3V rail with the unfiltered 3.3V plane. This renders the on-board filter useless. The excessive noise on VDDA_PCIE may cause excessive jitter on the PCIe links.

The best method to avoid this problem is to ensure there is sufficient decoupling on the 3.3V plane. Ideally, the decoupling capacitors are located under the BGA as close as possible to P4 or P12. If jitter on the PCIe links is excessive, and if it is not possible to directly decouple P4 or P12, P12 can be left unconnected. This can be completed by cutting the breakout trace from the P12 pad to the breakout via.

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