# IDT®
# Converting Designs from PLX PEX8111 or PEX8112 to IDT Tsi381

# Application Note

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# 1. Converting Designs from PLX PEX8111 or PEX8112 to IDT Tsi381

This document explains the hardware differences between the PLX PEX 8111BB or PEX8112AA and the IDT Tsi381. It is intended for anyone interested in converting designs based on the 8111 or 8112 to the Tsi381. Topics discussed include the following:

- "Overview"
- "Design Changes to Existing 8111 or 8112 Designs"
- "Recommendations for New Tsi381 or PEX8111/8112 Designs"

This document does not discuss register or functional differences between the PEX 8111/8112 and the Tsi381.

## Revision History

### 80E2000_AN002_05, Formal, September 2009

This document was rebranded as IDT. It does not include any technical changes.

### 80E2000_AN002_04, Formal, November 2008

Added PEX8112 information.

### 80E2000_AN002_03, Formal, November 2007

This version includes a minor update to "Power Sequencing".

### 80E2000_AN002_02, Formal, August 2007

There are no technical changes to this document version.

### 80E2000_AN002_01, Preliminary, April 2007

This is the first release of this document.

## 1.1 Overview

The Tsi381 is pin and package compatible with the PLX PEX8111 and PEX8112. The Tsi381 can be used as a drop-in replacement for these devices when the design differences outlined in the following section are considered.

The Tsi381 and 8111/8112 are available in a 144-pin BGA package with similar mechanical parameters. Each device can be soldered onto a common footprint on a system board.

## 1.2 Design Changes to Existing 8111 or 8112 Designs

Table 1 outlines the signal differences between the Tsi381 and 8111/8112.

**Table 1: Signal Differences**

| Pin Number | Signal Type | | Pin Name | | Target Board Implications |
|---|---|---|---|---|---|
| | 8111/8112 | Tsi381 | 8111/8112 | Tsi381 | |
| A9 | Output, open drain | N/A | WAKEOUT# | NC | None. This pin is never driven by Tsi381. |
| B9 | Output | N/A | PWR_OK | NC | This pin not driven by the Tsi381. If the board requires a power_ok status, a pull-up should be installed on this signal. |
| B1 | Input | Input | TMC1 | TEST_ BIDRCTL | None. This pin is tied low for both devices for normal operation. |
| C12 | Input | N/A | WAKEIN# | NC | None. The Tsi381 can accept a bias on this pin. |
| C8 | Input | Input | TMC | TEST_BCE | None. This pin is tied low for both devices for normal operation. |
| C2 | Input (8112 only) | Output | NC1 (8111) PCLKO62SEL# (8112) | PCI_CLKO[1] | On a 8111 target board, there should not be any connection to this pin. On a 8112 target board, this pin may be grounded or tied to VDD(3.3V). It is important not to connect Tsi381's PCI_CLKO[1] directly to ground or VDD. Verify if the target board makes such connection and correct it if required. A weak pull-up or pull-down resistor on this pin is acceptable. |
| K1 | Input | Input | SMC | TEST_ SPARE2 | None. The Tsi381 can accept a bias on this pin. |
| M11 | Input | Input | BTON | TEST_ SPARE0 | None. The Tsi381 can accept a bias on this pin. |
| D8 | Input | Input | BUNR1 | TEST_ SPARE1 | None. The Tsi381 can accept a bias on this pin. |
| E8 | Input | N/A | BAR0ENB# | NC | None. The Tsi381 can accept a bias on this pin. |
| K9 | Input | N/A | IDSEL | NC | None. The Tsi381 can accept a bias on this pin. |

**Table 1: Signal Differences *(Continued)***

| Pin Number | Signal Type | | Pin Name | | Target Board Implications |
|---|---|---|---|---|---|
| | 8111/8112 | Tsi381 | 8111/8112 | Tsi381 | |
| L11 | Input | N/A | FORWARD | NC | None. The Tsi381 can accept a bias on this pin. |
| L12 | Output, open drain | N/A | PMEOUT# | NC | The Tsi381 does not drive this pin. |
| M1 | Input | Input | TMC2 | PWRUP_PLL_ BYPASS | None. This pin is tied low for both devices for normal operation. |
| C10, D4, F6, F8, G6, G7, J9, K3, A5, A7, D5, E7 | Power | Power | AVDD, VDD_P, VDD_R, VDD_T, VDD1.5 | VDD, VDD_PCIE, VDDA_PLL | These pins must be 1.2V. |

## 1.2.1 Power Supply Differences

### *Supply Voltage*

The following 1.5V 8111/8112 signals, AVDD, VDD_P, VDD_R, VDD_T, and VDD1.5, must be lowered to 1.2V to support the Tsi381. When the 1.5V rail is supplied with an adjustable regulator and the 8111/8112 is the only device on the board using the 1.5V rail, this adjustment is usually made by changing a resistor on the regulator voltage sense circuit.

Alternatively, if a 1.2V rail already exists on the board, the 1.5V regulator can be removed. The 1.2V rail can be connected to the 1.5V power plane.

## 1.2.2 Power Sequencing

The 8111/8112 requires a high-to-low power sequence (5V → 3.3V → 1.5V). The Tsi381 does not have any power sequencing constraints, and therefore, is compatible with the 8111/8112 power sequencing.

## 1.2.3 Serial EEPROM

The contents of a Serial EEPROM that is programmed for an 8111/8112 will not be read by the Tsi381. For the Tsi381, the first two bytes in the Serial EEPROM (0x28AB) are used to store an identification code. For the 8111/8112, the first byte in the EEPROM (0x5A) is used to store an identification code. If the 8111/8112 board has specific setups in the Serial EEPROM, a conversion is required for Tsi381.

The default EECLK frequency on the 8111/8112 is 2 MHz, while on the Tsi381 it is 7.8 MHz. Some older Serial EEPROMs do not support 7.8 MHz. If the target board uses such a device (AT25010, AT25020, AT25040), it should be replaced with a Serial EEPROM suitable for the Tsi381. In general, the Tsi381 can use the same Serial EEPROM device as PEX8111/8112.

### 1.2.4 AC and DC Specifications

The AC and DC specification differences are outlined in Table 2.

**Table 2: AC and DC Specification Differences**

| Specification | Tsi381 | 8111 | 8112 |
|---|---|---|---|
| Minimum PCI clock frequency | 25 MHz | None | None |
| 3.3V Input high minimum voltage | 2.0V | 1.6V | 1.7V |
| 3.3V Input low maximum voltage | 0.8V | 0.7V | 0.7V |
| 5V PCI maximum output low voltage | 0.55V @6mA | 0.4V @ 12mA | 0.4V @12mA |

### 1.2.5 Thermal Specifications

The thermal differences are outlined in Table 3.

**Table 3: Thermal Specification Differences**

| Specification | Tsi381 | 8111 | 8112 |
|---|---|---|---|
| JA | 21.8°C/W | 32.4°C/W | 33.07°C/W |
| JB | 16.3°C/W | Not available | Not available |
| JC | 9.7°C/W | 6.8°C/W | 11.06°C/W |
| $T_{junc}$ | -40/+125°C | Not available | +125°C |
| $T_{ambiant}$ | -40/+85°C | 0/+70°C | -40/+85°C |

# 1.3 Recommendations for New Tsi381 or PEX8111/8112 Designs

This section describes possible design implementations that can accommodate both the Tsi381 and 8111/8112.

## 1.3.1 PLL Filters

The Tsi381 analog supply pins are different from those used by the 8111/8112: the Tsi381 supply pins require a noise suppression filter. To accommodate this difference, place a filter on each pin in Table 4. For more information on implementing a PLL filter in a Tsi381 design, see the *Tsi381 Evaluation Board Schematics*.

**Table 4: Analog Power Pin Differences**

| Tsi381 | 8111/8112 |
|---|---|
| **1.2V analog pin** | **1.5V analog pin** |
| E7 (VDDA_PLL) | D5 (VDD_P) |
| | |
| **3.3V analog pin** | **3.3V analog pin** |
| E5 (VDDA_PCIE) | None |

## 1.3.2 Power Supply Selection

Use an adjustable voltage regulator to supply the 1.2V rail of the Tsi381 or the 1.5V rail of the 8111/8112. Most “buck” switching regulators can use the 12V rail as the source for the 1.2V or 1.5V rail. There are also a few adjustable LDOs (low drop-out linear regulators) that can use the 12V rail to regulate down to 1.2V. Table 5 lists a number of suitable LDOs.

**Table 5: Adjustable LDO for 1.2V or 1.5V Supply**

| Manufacturer | Part Number |
|---|---|
| Micrel | MIC49150 |
| National Semiconductor | LP38842 |
| National Semiconductor | LP38841 |
| Linear Technology | LTC3025 |
| Linear Technology | LT3021 |

### 1.3.3 Power Sequencing

The Tsi381 does not have any power sequencing constraints, and therefore, is compatible with the 8111/8112's power sequencing.

### 1.3.4 PCLKO62SEL# (8112)

The 8112 uses pin C2 as an input for PCLKO62SEL#, whereas C2 is a PCI clock output on Tsi381. Pin C2 should be weakly pulled-up or pulled-down when the 8112 is used, and left unconnected when using the Tsi381.