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CMOS Logic IC HD74AC Series (FACT)

Descriptions and Family Characteristics

1. Advanced CMOS FACT Logic

FACT logic offers a unique combination of high speed, low power dissipation, high noise immunity, wide fanout capability, extended power supply range and high reliability.

This document describes the product line with device specifications as well as material discussing design considerations and comparing the FACT family to predecessor technologies.

For direct replacement of LS, ALS and other TTL devices, HD74ACT circuits with TTL-type input thresholds are included in the FACT family. These include the more popular bus drivers/transceivers as well as many other HD74ACTXXX devices.

1.1 Characteristics

- Full logic product line
- Industry standard functions and pinouts for SSI and MSI
- Meets or exceeds JEDEC standards for HD74ACXX family
- TTL inputs on selected circuits
- High performance outputs
  - Common output structure for standard and buffer drivers
  - Output Sink/Source Current of 24 mA
  - Transmission line driving 50 Ω guaranteed
- Operation from 2 to 6 volts guaranteed
- Temperature range –40°C to +85°C
- Improved ESD protection network
- High current latch-up immunity

1.2 Interfacing

FACT devices have a wide operating voltage range (V_{CC} = 2 to 6 VDC) and sufficient current drive to interface with most other logic families available today.

Device designators are as follows:

- HD74AC is a high-speed CMOS device with CMOS input switching levels and buffered CMOS outputs that can drive ±24 mA of I_{OH} and I_{OL} current. Industry standard HD74AC nomenclature and pinouts are used.
- HD74ACT is a high-speed CMOS device with a TTL-to-CMOS input buffer stage. These device inputs are designed to interface with TTL outputs operating with a V_{CC} = 5 V ±0.5 V with V_{OH} = 2.4 V and V_{OL} = 0.4 V, but are functional over the entire FACT operating voltage range of 2.0 to 5.5 VDC. These devices have buffered outputs that will drive CMOS or TTL devices with no additional interface circuitry. HD74ACT devices have the same output structures as HD74AC devices.

1.3 Low Power CMOS Operation

If there is one single characteristic that justifies the existence of CMOS, it is low power dissipation. In the quiescent state, FACT draws three orders of magnitude less power than the equivalent LS or ALS TTL device. This enhances system reliability; because costly regulated high current power supplies, heat sinks and fans are eliminated. FACT logic devices are ideal for portable systems such as laptop computers and backpack communications systems. Operating power is also very low for FACT logic. Power consumption of various technologies with a clock frequency of 1 MHz is shown below.

- FACT = 0.1 mW/gate
- ALS = 1.2 mW/gate
- LS = 2.0 mW/gate
- HC = 0.1 mW/gate

Figure 1 illustrates the effects of I_{CC} versus power supply voltage (V_{CC}) for two load capacitance values: 50 pF and stray capacitance. The clock frequency was 1 MHz for the measurements.

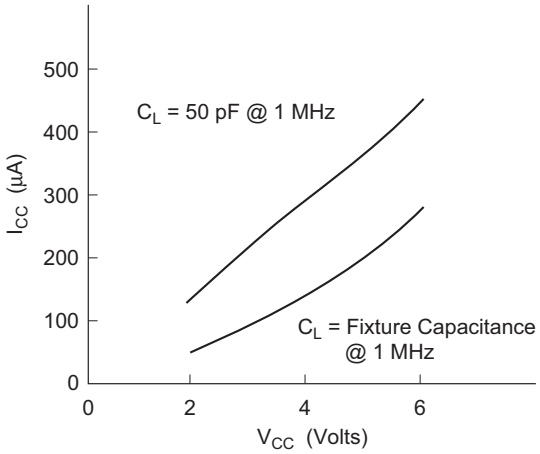

Figure 1 I_{CC} vs V_{CC}

1.4 AC Performance

In comparison to LS, ALS and HC families, FACT devices have faster internal gate delays as well as the basic gate delays. Additionally, as the level of integration increases, FACT logic leads the way to very high-speed systems.

The example below describes typical values for a HD74XX138, 3 to 8 line decoder.

- FACT = 6.0 ns @ CL = 50 pF
- ALS = 12.0 ns @ CL = 50 pF
- LS = 27.0 ns @ CL = 15 pF
- HC = 17.0 ns @ CL = 50 pF

AC performance specifications are guaranteed at 5.0 V ± 0.5 V and 3.3 V ± 0.3 V. For worst case design at 2.0 V V_{CC} on all device types, the formula below can be used to determine AC performance.

AC performance at 2.0 V V_{CC} = 1.9 × AC specification at 3.3 V

1.5 Multiple Output Switching

Propagation delay is affected by the number of outputs switching simultaneously. Typically, devices with more than one output will follow the rule: for each output switching, derate the document specification by 250 ps. This effect typically is not significant on an octal device unless more than four outputs are switching simultaneously. This derating is valid for the entire temperature range and 5.0 V ± 10% V_{CC}.

1.6 Noise Immunity

The noise immunity of a logic family is also an important equipment cost factor in terms of decoupling components, power supply dynamic resistance and regulation as well as layout rules for PC boards and signal cables.

The comparisons shown describe the difference between the input threshold of a device and the output voltage, $|V_{IL}–V_{OL}| / |V_{IH}–V_{OH}|$ at 4.5 V V_{CC}.

- FACT = 1.25/1.25 V
- ALS = 0.4/0.7 V
- LS = 0.3/0.7 V@ 4.75 V V_{CC}
- HC = 1.25/1.25 V

1.7 Output Characteristics

All FACT outputs are buffered to ensure consistent output voltage and current specifications across the family. Both HD74AC and HD74ACT device types have the same output structures. Two clamp diodes are internally connected to

the output pin to suppress voltage overshoot and undershoot in noisy system applications witch can result from impedance mismatching. The balanced output design allows for controlled edge rates and equal rise and fall times.

All devices (HD74AC or HD74ACT) are guaranteed to source and sink 24 mA. HD74AC/ACTXXX, are capable of driving 50 Ω transmission lines.

1.7.1 I_{OL}/I_{OH} Characteristics

- FACT = 24/–24 mA
- ALS = 24/–15 mA
- LS = 8/–0.4 mA @ 4.75 V V_{CC}
- HC = 4/–4 mA

1.7.2 Dynamic Output Drive

Traditionally, in order to predict what incident wave voltages would occur in a system, the designer was required to do an output analysis using a Bergeron diagram. Not only is this a long and time-consuming operation, but the designer needed to depend upon the accuracy and reliability of the manufacturer-supplied 'typical' output I/V curve. Additionally, there was no way to guarantee that any supplied device would meet these 'typical' performance values across the operating voltage and temperature limits. Renesas has taken the necessary steps to guarantee incident wave switching on transmission lines with impedances as low as 50 Ω.

Figure 2 shows a Bergerton diagram for switching both high-to-low and low-to-high. On the right side of the graph (I out > 0), are the VOH and IIH curves for FACT logic while on the left side (Iout < 0), are the curves for VOL and IIL. Although we will only discuss here the low-to-high transition, the information presented may be applied to a high-to-low transition.

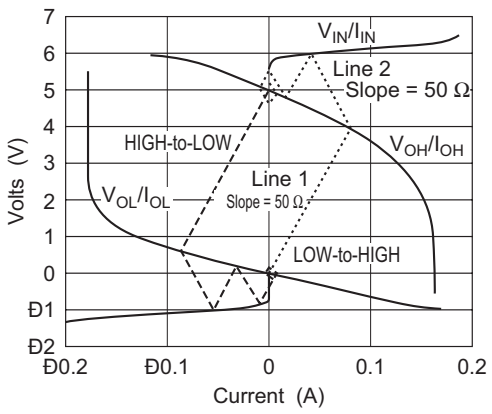

Figure 2 Gate Driving 50 Ω Line Reflection Diagram

Begin analysis at the V_{OL} (quiescent) point. This is the intersection of the V_{OL}/I_{OL} curve for the output and the VIN/IIN curve for the input. For CMOS inputs and outputs, this point will be approximately 100 mV. Then draw a 50 Ω load line from this intersection to the V_{OH}/I_{OH} curve as shown by Line 1. This intersection is the voltage that the incident wave will have. Here it occurs at approximately 3.95 V. Then draw a line with a slope of –50 Ω from this first intersection point to the V_{IN}/I_{IN} curve as shown by Line 2. This second intersection will be the first reflection back from the input gate. Continue this process of drawing the load line from each intersection to the next. Lines terminating on the V_{OH}/I_{OH} curve should have positive slopes while lines terminating on the V_{IN}/I_{IN} curve should have negative slopes.

Each intersection point predicts the voltage of each reflected wave on the transmission line. Intersection points on the V_{OH}/I_{OH} curve will be waves traveling from the driver to the receiver while intersection points on the VIN/IIN curve will be waves traveling from the receiver to the driver.

Figure 3 and 4 show the resultant waveforms. Each division on the time scale represents the propagation delay of the transmission line.

While this exercise can be done for FACT, it is no longer necessary. FACT is guaranteed to drive an incident wave of enough voltage to switch another FACT input.

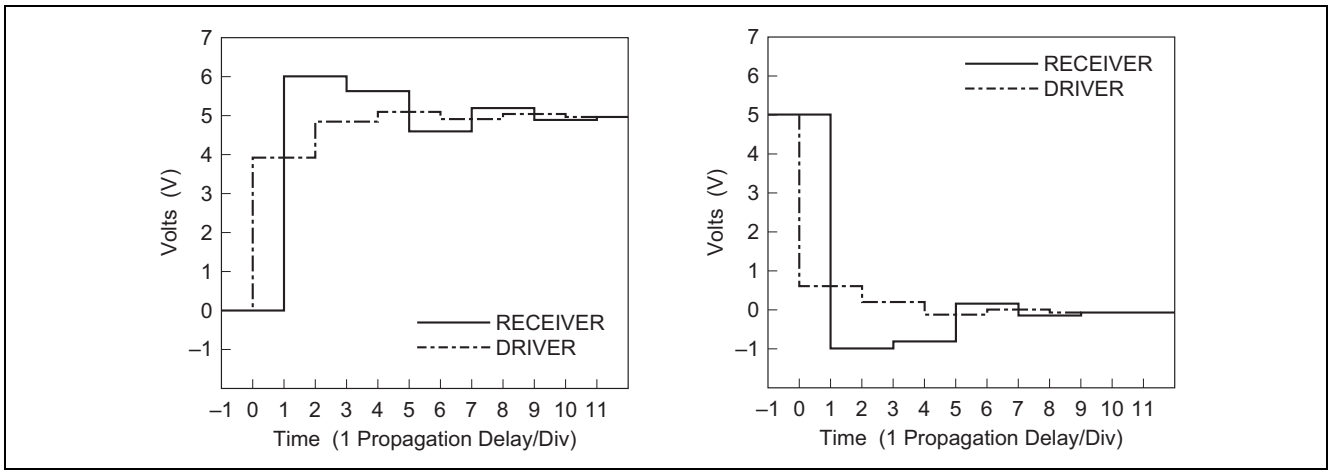

Figure 3 Resultant Waveforms Driving 50 Ω Line–Theoretical

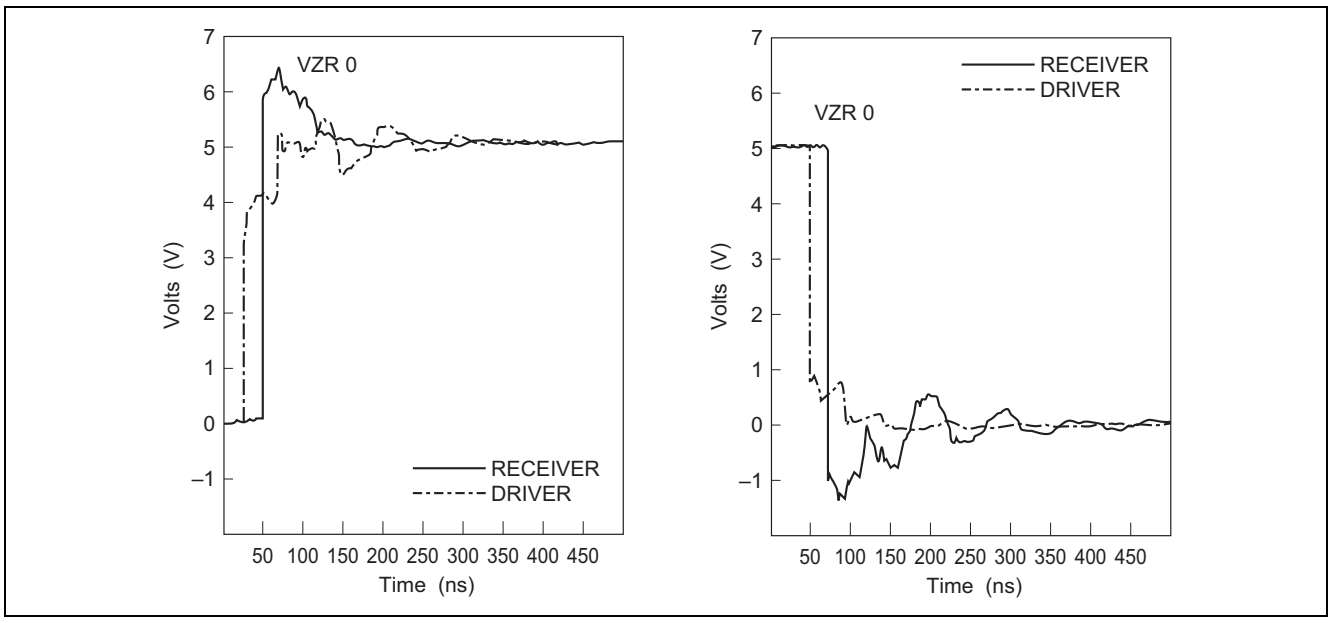

Figure 4 Resultant Waveforms Driving 50 Ω Line–Actual

We can calculate what current is required by looking at the Bergeron diagram. The quiescent voltage on the line will be within 100 mV of either rail. We know what voltage is required to guarantee a valid voltage at the receiver. This is either 70% or 30% of V_{CC}. The formula for calculating the current and voltage required is $| (V_{OQ}–V_I)/Z_O |$ at V_I. For V_{OQ} = 100 mV, V_{IH} = 3.85 V, V_{CC} = 5.5 V and Z_O = 50 Ω, the required I_{OH} at 3.85 V is 75 mA. For the high-to-low transition, V_{QQ} = 5.4 V, V_{IL} = 1.65 V, and Z_O = 50 Ω, I_{OL} is 75 mA at 1.65 V. FACT's I/O specifications include these limits. For transmission lines with impedances greater than 50 Ω, the current requirements are less and switching is still guaranteed.

It is important to note that the typical 24 mA drive specification is not adequate to guarantee incident wave switching. The only way to guarantee this is to guarantee the current required to switch a transmission line from the output quiescent point to the valid V_{IN} level.

The performance charts in figures 5 to 7 are provided in order to aid the designer in determining dynamic output current drive of FACT devices with various power supply voltage.

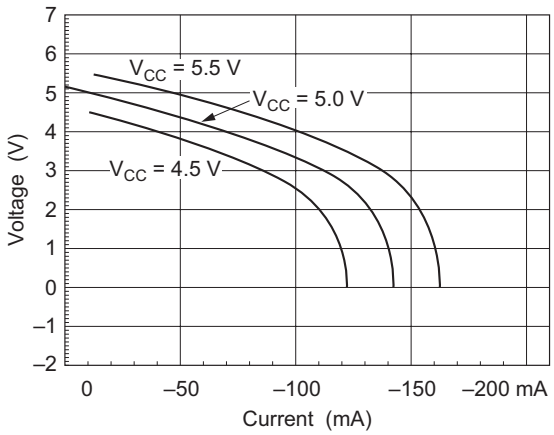

Figure 5 Output Characteristics V_{OH}/I_{OH}, HD74AC00

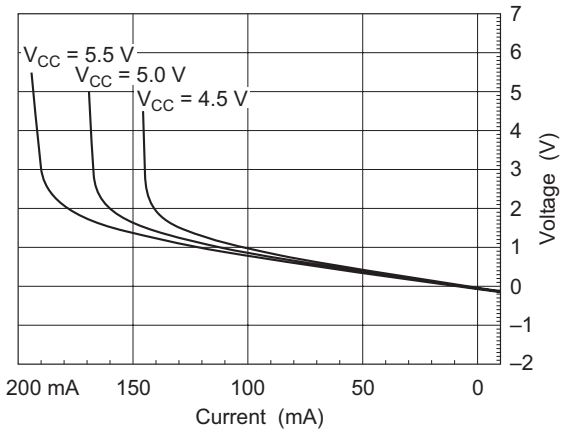

Figure 6 Output Characteristics V_{OL}/I_{OL}, HD74AC00

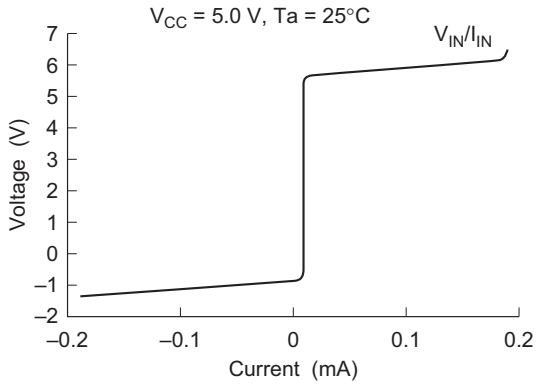

Figure 7 Input Characteristics VIN/IIN

1.8 Choice of Voltage Specifications

To obtain better performance and higher density, semiconductor technologies are reducing the vertical and horizontal dimensions of integrated device structures. Due to a number of electrical limitations in the manufacture of VLSI devices and the need for low-voltage operation in memory cards, the JEDEC committee decided to establish interface standards for devices operating at 3.3 V ±0.3 V. To this end, Renesas guarantees all of its devices operational at 3.3 V ±0.3 V. Note also that AC and DC specifications are guaranteed between 3.0 and 5.5 V. Operation of FACT logic is also guaranteed from 2.0 to 6.0 V on V_{CC}.

Operating Voltage Ranges

- FACT = 2.0 to 6.0 V
- ALS = 5.0 V ±10%
- LS = 5.0 V ±5%
- HC = 2.0 to 6.0 V

1.9 FACT Replaces LS, ALS, HCMOS

The Advanced CMOS family is specifically designed to outperform the LS, ALS, and HCMOS families. Figure 8 shows the relative position of various logic families in speed/power performance.

Table 1 summarizes the key performance specifications for various competitive technology logic families. Table 2 compares propagation delays.

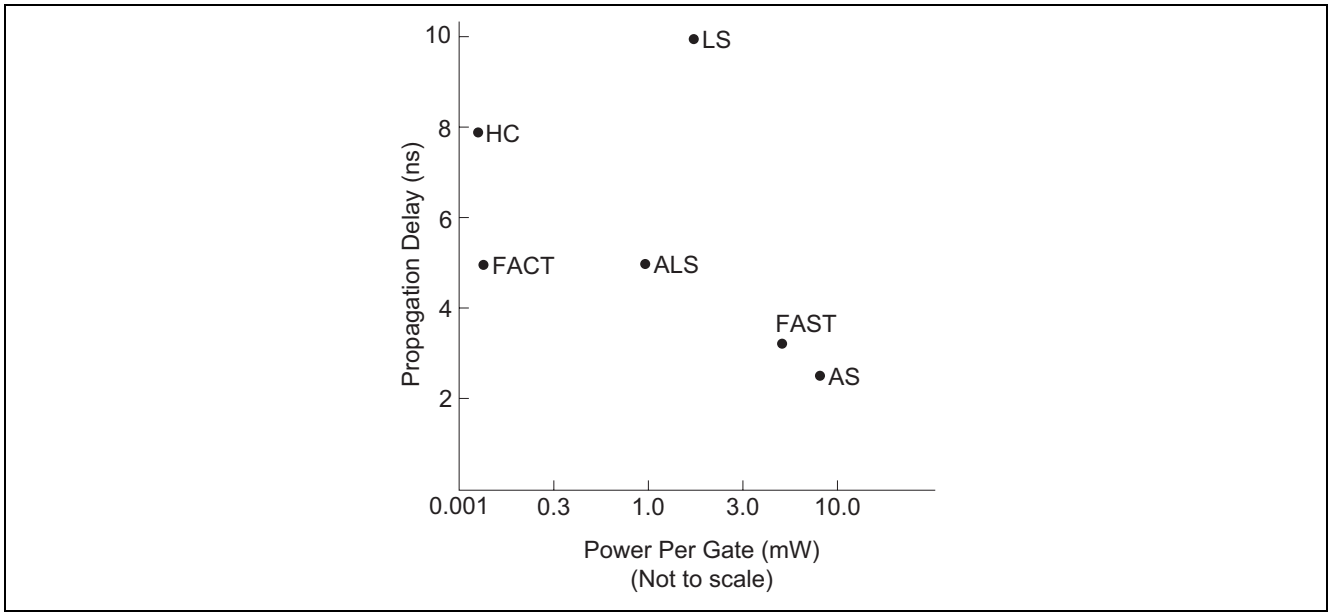

Figure8 Propagation Delays

Table 1a Logic Family Comparisons General Characteristics (All Max Ratings)

Characteristics	Symbol	LS	ALS	HCMOS	FACT		Unit
					HD74AC	HD74ACT	
Operating voltage range	$V_{CC/EE/DD}$	5 ± 5%	5 ± 10%	2.0 to 6.0	2.0 to 6.0	4.5 to 5.5	V
Operating temperature range		–20 to +75	0 to +70	–40 to +85	–40 to +85	–40 to +85	°C
Input voltage (limits)	V_{IH} (min)	2.0	2.0	3.15	3.15	2.0	V
	V_{IL} (max)	0.8	0.8	1.35	1.35	0.8	V
Output voltage (limits)	V_{OH} (min)	2.7	2.7	V_{CC} – 0.1	V_{CC} – 0.1	V_{CC} – 0.1	V
	V_{OL} (max)	0.5	0.5	0.1	0.1	0.1	V
Input current	I_{IH}	20	20	+1.0	+1.0	+1.0	µA
	I_{IL}	–400	–200	–1.0	–1.0	–1.0	µA
Output current at V0 (limit)	I_{OH}	–0.4	–0.4	–4.0 @ V_{CC}–0.37	–24 @ V_{CC}–0.7	–24 @ V_{CC}–0.7	mA
	I_{OL}	8.0	8.0	4.0 @ 0.33 V	24 @ 0.37 V	24 @ 0.37 V	mA
DC noise margin low/high	DCM	0.3/0.7	0.4/0.7	1.25/1.25	1.25/1.25	0.7/2.4	V

Table 1b Logic Family Comparisons Speed/Power Characteristics (All Typical Ratings)

Characteristics	Symbol	LS	ALS	HCMOS	FACT		Unit
					HD74AC	HD74ACT	
Quiescent supply current/Gate	I_G	0.4	0.2	0.0005	0.0005		mA
Power/gate (Quiescent)	P_G	2.0	1.2	0.0025	0.0025		mW
Propagation delay	t_P	10	5.0	8.0	5.0		ns
Speed power product	—	20	6.0	0.02	0.01		pJ
Clock frequency D/FF	f_{max}	33	50	50	160		MHz

Table 2 Propagation Delay

Product			LS	ALS	HCMOS	FACT	unit
t_{PLH}/t_{PHL}	HD74XX00	Typ	10.0	5.0	8.0	5.0	ns
		Max	15.0	11.0	23.0	8.5	ns
t_{PLH}/t_{PHL} (Clock to Q)	HD74XX74	Typ	25.0	12.0	14.0	8.0	ns
		Max	40.0	18.0	40.0	10.5	ns
t_{PLH}/t_{PHL} (Clock to Q)	HD74XX163	Typ	18.0	10.0	18.0	5.0	ns
		Max	27.0	17.0	40.0	10.0	ns

Note: continuous: (LS) V_{CC} = 5.0 V, CL = 15pF, 25°C;
(ALS/HC/FACT) V_{CC} = 5.0 V ± 10%, C_L = 50 pF, typ values at 25°C, max values at 0 to 70°C for ALS. –40 to +85°C for HC/FACT.

2. Circuit Characteristics

2.1 Power Dissipation

One advantage to using CMOS logic is its extremely low power consumption. During quiescent conditions, FACT will consume several orders of magnitude less current than its bipolar counterparts. But DC power consumption is not the whole picture. Any circuit will have AC power consumption, whether it is built with CMOS or bipolar technologies.

Power consumption of a circuit can be calculated using the formula:

$$P_D = [(C_L + C_{PD}) \bullet V_{CC} \bullet V_S \bullet f] + [I_Q \bullet V_{CC}]$$

where:

P_D = power dissipation
C_L = load capacitance
C_{PD} = device power capacitance
V_{CC} = power supply
V_S = output voltage swing
f = frequency of operation
I_Q = quiescent current

Power consumption for FACT is dependent on the supply voltage, frequency of operation, internal capacitance and load. V_S will be V_{CC} and I_Q can be considered negligible for CMOS. Therefore, the simplified formula for CMOS is:

$$P_D = (C_L + C_{PD})V_{CC}^2 f$$

C_{PD} values for CMOS devices are calculated by measuring the power consumption of a device at two different frequencies. C_{PD} is calculated in the following manner.

1. The power supply voltage is set to V_{CC} = 5.0 VDC.
2. Signal inputs are set up so that as many outputs as possible are switching, giving a worst-case situation per JEDEC C_{PD} conditions.

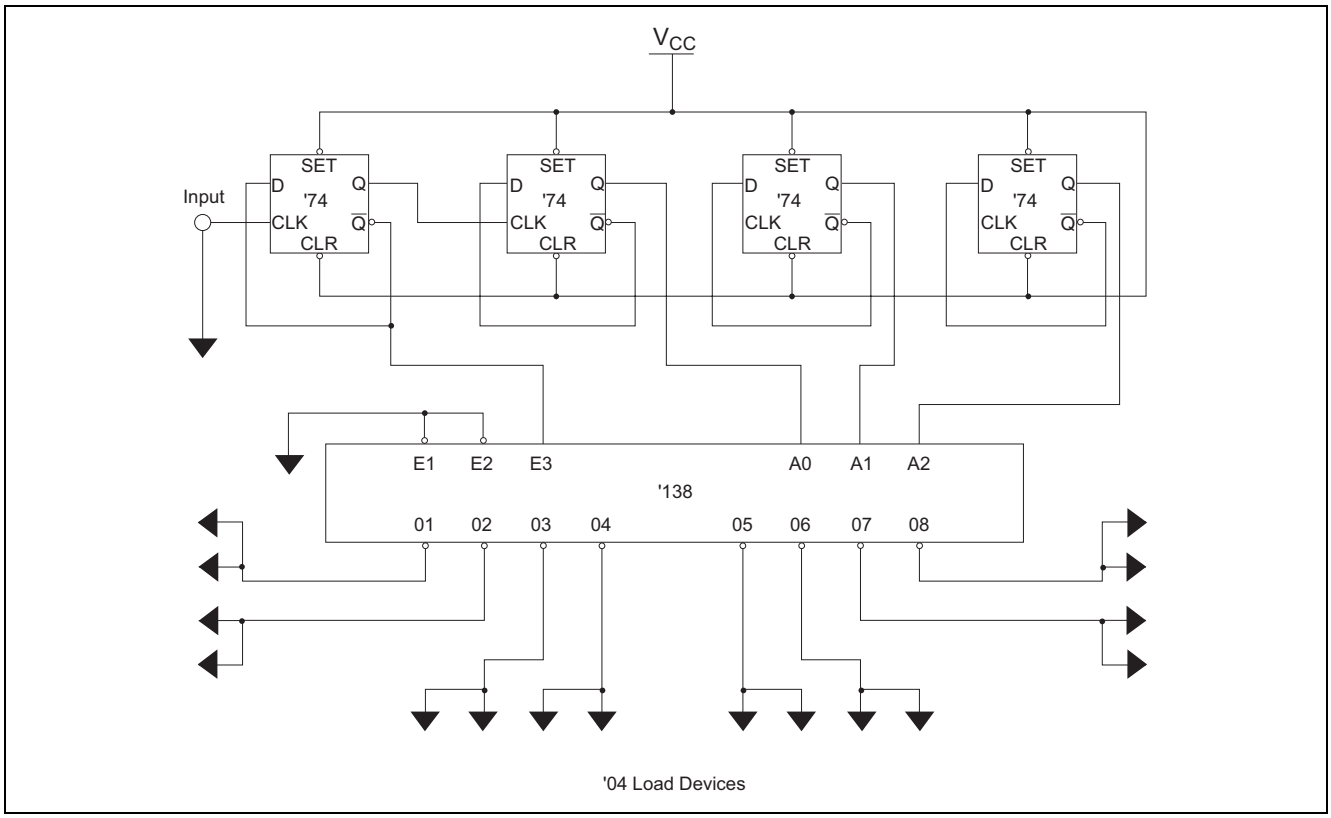

Figure 9 Power Demonstration Circuit Schematic

3. The power supply current is measure and recorded at input frequencies of 200 kHz and 1 MHz.
4. The power dissipation capacitance is calculated by solving the two simultaneous equations

$$P_1 = (C_{PD} \bullet V_{CC}^2 \bullet f_1) + (I_{CC} \bullet V_{CC})$$
$$P_2 = (C_{PD} \bullet V_{CC}^2 \bullet f_2) + (I_{CC} \bullet V_{CC})$$

giving

$$C_{PD} = (P_1 - P_2)/V_{CC}^2 (f_1 - f_2)$$

or

$$C_{PD} = (I_1 - I_2)/V_{CC}(f_1 - f_2)$$

where

I_1 = supply current at f_1 = 200 kHz.
I_2 = supply current at f_2 = 1 MHz

On FACT device data sheets, C_{PD} is a typical value and is given either for the package or for the individual device (i.e., gates, flip-flops, etc.) within the package.

The circuit shown in Figure 9 was used to compare the power consumption of FACT versus ALS devices.

Two identical circuits were built on the same board and driven from the same input. In the circuit, the input signal was driven into four D-type flip-flops which act as divide-by-2 frequency dividers. The outputs from the flip-flops were connected to the inputs of a HD74AC138/74ALS138 decoder. This generated eight non-overlapping clock pulses on the outputs of the HD74AC138/74ALS138, which were then connected to an HD74AC04/74ALS04 inverter. The input frequency was then varied and the power consumption was measured. Figure 10 illustrates the results of these measurements.

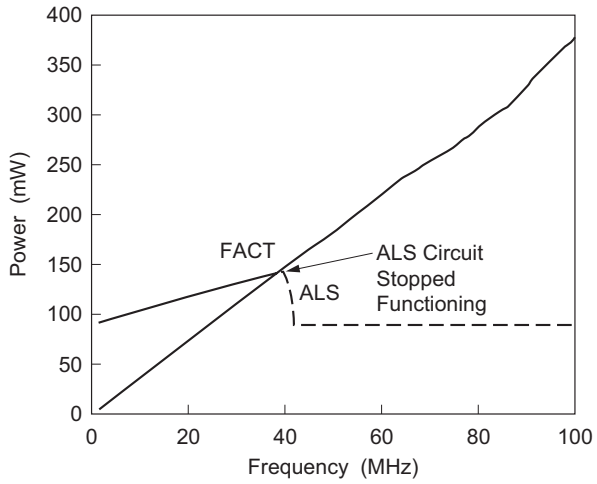

Figure 10 FACT vs ALS Circuit Power

Below 40 MHz, the FACT circuit dissipates much less power than the ALS version. It is interesting to note that when the frequency went to zero, the FACT circuit's power consumption also went to zero; the ALS circuit continued to dissipate almost 100 mW. Another advantage of FACT is its capabilities above 40 MHz. At this frequency, the first 74ALS74 D-type flip-flop ceased to operate. Once this occurred, the entire circuit stopped working and the power consumption fell to its quiescent value. The FACT device, however, continued functioning beyond the limit of the frequency generator, which was 100 MHz.

This graph shows two advantages of FACT circuits (power and speed). FACT logic delivers increased performance in addition to offering the power savings of CMOS.

2.2 Capacitive Loading Effects

In addition to temperature and power supply effects, capacitive loading effects for loads greater than 50 pF should be taken into account for propagation delays of FACT devices. Minimum delay numbers may be determined from table 3. Propagation delays are measured to the 50% point of the output waveform.

Table 3 Minimum Propagation Delay

Parameter	**Voltage(V)**			**Units**
	3.0	**4.5**	**5.5**	
T_{rise}	31	22	19	ps/pF
t_{fall}	18	13	12.5	ps/pF

Note: TA = 25°C

The two graphs following, figures 11 and 12, describe propagation delays on FACT devices as affected by variations in power supply voltage (V_{CC}) and lumped load capacitance (C_L). Figures 13 and 14 show the effects of lumped load capacitance on rise and fall times for FACT devices.

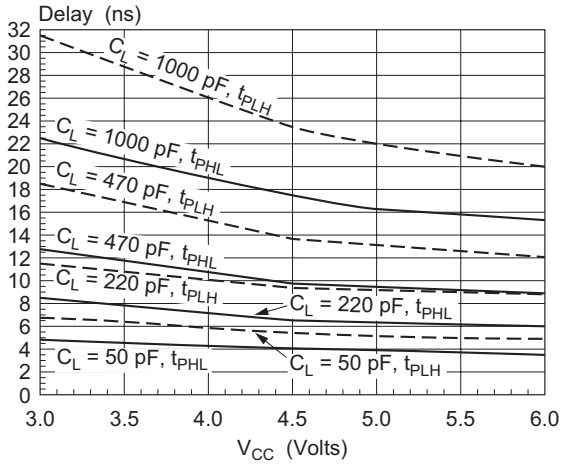

Figure 11 Propagation Delay vs. V_{CC} (HD74AC00)

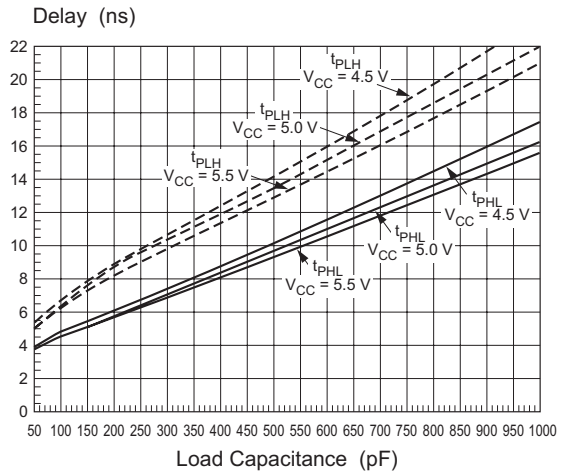

Figure 12 Propagation Delay vs. C_L (HD74AC00)

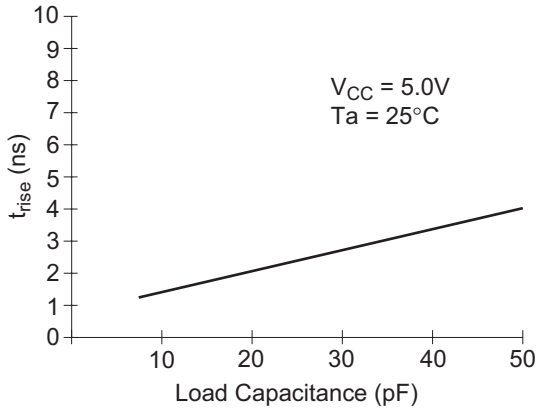

Figure 13 t_{rise} vs. Capacitance

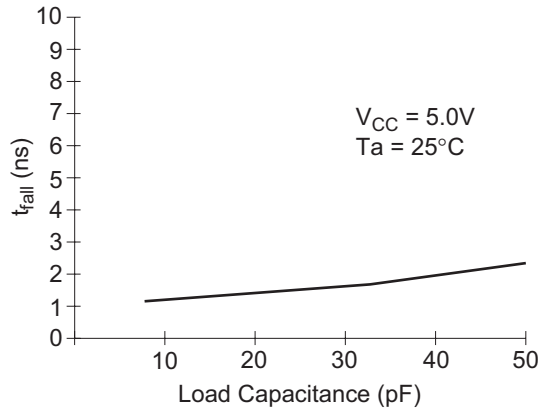

Figure 14 t_{fall} vs. Capacitance

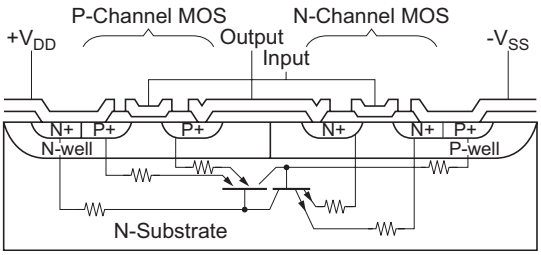

Figure 15 CMOS Inverter Cross Section with Latch-up Circuit Schematic

2.3 Latch-up

A major problem with CMOS has been its sensitivity to latch-up, usually attributed to high parasitic gains and high input impedance (figure 15). FACT logic is guaranteed not to latch-up with dynamic currents of 100 mA forced into or out of the inputs or the outputs under worst case conditions (Ta = 85˚C and V_{CC} = 5.5 VDC). At room temperature the parts can typically withstand dynamic currents of over 450 mA. For most designs, latch-up will not be a problem, but the designer should be aware of its causes and how to prevent it.

FACT devices have been specifically designed to reduce the possibility of latch -up occurring; Renesas accomplished this by lowering the gain of the parasitic transistors, reducing N-well and p-well resistivity to increase external drive current required to cause a parasitic to turn on, and careful design and layout to minimize the substrate-injected current coupling to other circuit areas.

2.4 Electrostatic Discharge (ESD) Sensitivity

FACT circuits show excellent resistance to ESD-type damage. These logic devices are classified as category ‘B’ of MIL-STD-883C, test method 3015, and withstand 4000 V typically. FACT logic is guaranteed to have 2000 V ESD immunity on all inputs and outputs. FACT parts do not require any special handling procedures. However, normal handling precautions should be observed as in the case of any semiconductor device.

Figure 16 shows the ESD test circuit used in the sensitivity analysis for this specification. Figure 17 is the pulse waveform required to perform the sensitivity test.

The test procedure is as follows: five pulses, each of 2000 V, are applied to every combination of pins with a five second cool-down period between each pulse. The polarity is then reversed and the same procedure, pulse and pin combination used for an additional five discharges. Continue until all pins have been tested. If none of the devices from the sample population fails the DC and AC test characteristics, the device shall be classified as category B of MIL-STD-883C, TM-3015. For further specifications of TM-3015, refer to the relevant standard. The voltage is increased and the testing procedure is again performed; this entire process is repeated until all pins fail. This is done to thoroughly evaluate all pins.

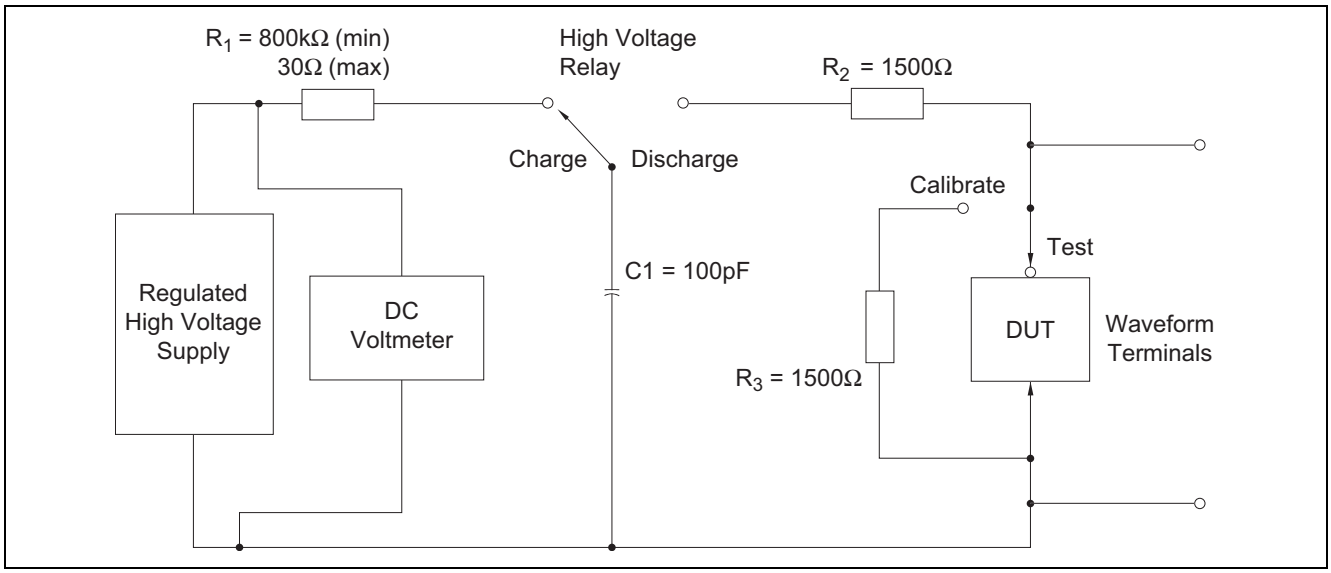

Figure 16 ESD Test Circuit

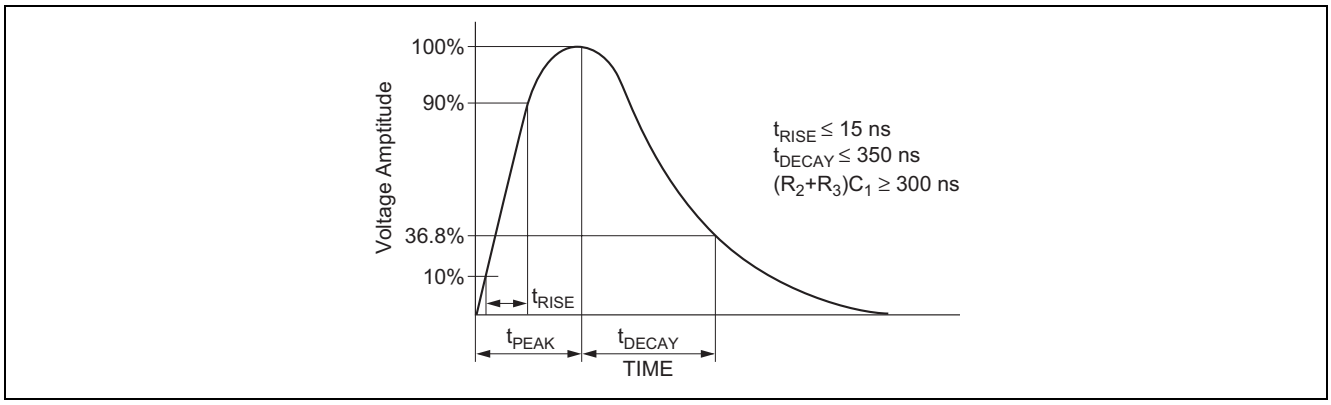

Figure 17 ESD Pulse Waveform

Revision Record

Rev.	Date	Description	
		Page	Summary
1.00	Jul.09.04	—	First edition issued

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