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April 1st, 2010
Renesas Electronics Corporation

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Bi-CMOS Logic IC HD74BC Series

Definition

1. Loading Circuit

Figure 2 shows the AC loading circuit used in characterizing and specifying propagation delays of all HD74BC series devices unless otherwise specified. The loading capacitance of 50 pF allows more leeway in stray capacitance and also serves as a load to the device during rising and falling output transitions. This more closely resembles the loading to be expected in average applications and thus gives the designer more useful delay estimations. The 500 Ω of resistor to ground can be a passive probe for an oscilloscope. In another word, the 500 Ω resistor to ground can be a series of a 450 Ω resistor and a sampling oscilloscope with 50 Ω internal termination through a 50 Ω coaxial cable. And, the device input pin is connected with the other input to the sampling oscilloscope through a cable of the same impedance. It equivalents to terminating output of pulse generator signal with 50 Ω. As shown in figure 2, another 500 Ω resistor is used across the output of a tested device and a switch. This switch is open for most measurements, and to measure enable and disable time of three-state outputs (low to off, off to low) it is closed.

Output pins voltage when this switch is closed will be quiescent high level, as 7 V voltage is divided by two 500 Ω resistors. See figures 3 to 7 for definitions of AC test waveforms.

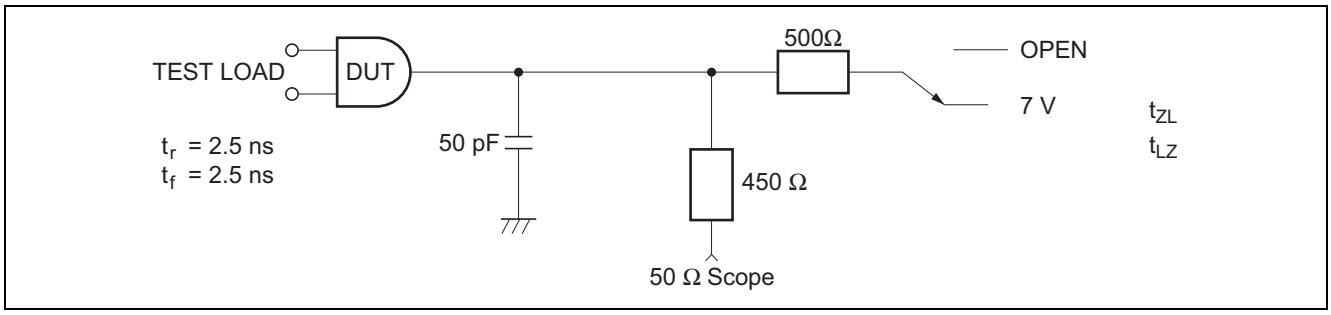

Figure 1 AC Loading Circuit

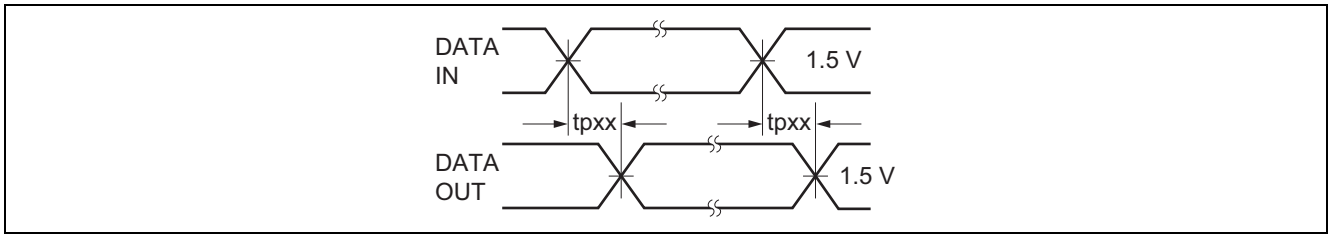

Figure 2 Propagation Delay Time

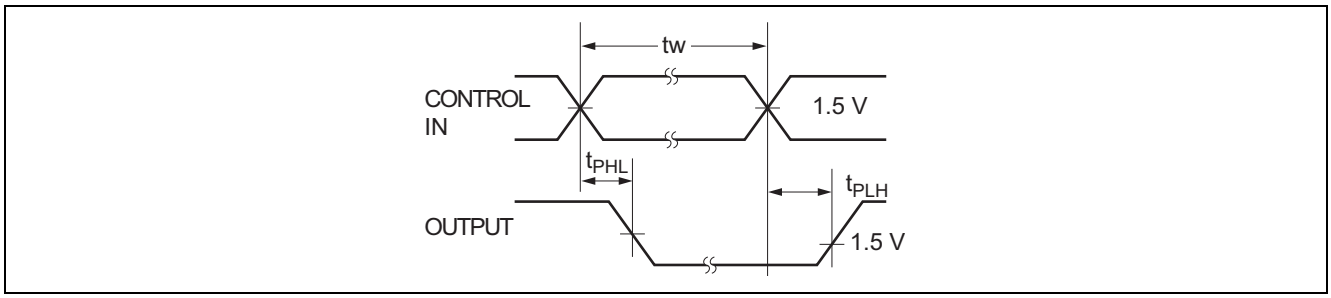

Figure 3 Propagation Delay Time and Pulse Width

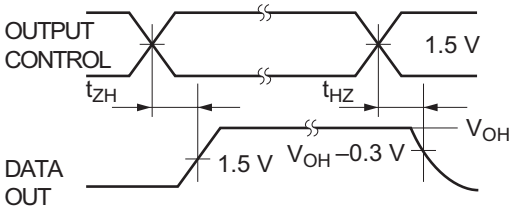

Figure 4 Three-State Output: t_{ZH}, t_{HZ}

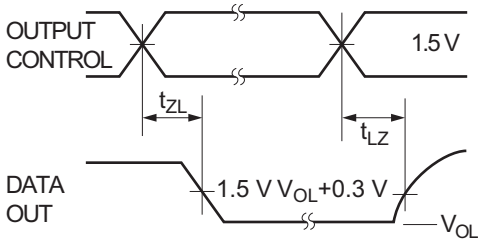

Figure 5 Three-State Output: t_{ZL}, t_{LZ}

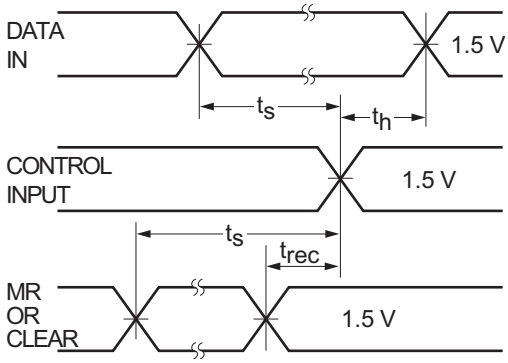

Figure 6 Set Up Time and Hold Time

2. Test Conditions

The AC test conditions take 0 V as low level and 3 V for high level as same as other families. And input rising and falling time is defined to be 2.5 ns, and 1 ns at maximum clock frequency and pulse-width measurements. DC characteristics tests use VIH and VIL defined in specifications for input voltages. On test, adequate decoupling of power supplies is required to eliminate the influence of noise. Special attention must be paid when an IC tester or a handler is used. To improve the noise margin for testers' inherent noise which does not occur in the actual system, DC input levels may need to be adjusted. Noise immunity testing is performed by raising V_{IN} to the supply voltage, V_{CC} then dropping it to a level corresponding to V_{IH}, and then raising it again to the V_{CC} level. Noise tests can also be performed on the V_{IL} characteristics by raising V_{IN} from 0 V to V_{IL}, then returning it to 0 V. Confirm that no changes appear at outputs when input levels reach V_{IH} or V_{IL}. On fabricating test jigs and tools, high frequency characteristics should be sufficiently considered for wirings. Leads on the load capacitor should be as short as possible to evaluate ripples and undershoot on output waveforms. Generous ground metal or preferably a plane ground should be used for the same reasons. A V_{CC} bypass capacitor should be provided at the test socket, also with minimum lead lengths.

3. Multiple Output Switching

Propagation delay is affected by the number of outputs switching simultaneously. Devices with two or more outputs will delay by 250 ps in typical than the specification in datasheet for each increase of simultaneously switching outputs.

This effect is not significant on an octal devices unless more than four outputs are switching simultaneously. This derating is applied for the entire temperature range from –40 to 85°C and V_{CC} range of 5 V ±10%.

4. I_{CCT} Characteristics

If a HD74BC series device is used to replace a TTL counterpart, I_{CCT} specification should be considered. The I_{CCT} specification denotes the increase in normal I_{CC}. For each input at applied V_{CC} –2.1 V, the I_{CCT} value should be added to the quiescent current to get the circuit's worst-case static I_{CC} value. In fact, there are several factors which tend to reduce the increase in I_{CC} per input.

Most TTL devices can drive input voltage beyond the TTL output voltage specification owing to low input current because input part is constructed by CMOS in typical systems. For example, the normal high speed bipolar logic outputs can drive HD74BC type inputs down to 200 mV and up to 3.5 V. Consequently, voltage can be applied to input pins under relaxed conditions than the I_{CCT} test conditions. Moreover, typical values of I_{CCT} on each input pin will be much less than the specification. Figure 8 shows the change of I_{CCT} for input voltages. On designing with HD74BC series as well as designing with other TTL level compatible CMOS, understand the meaning of I_{CCT} spec. and consider that the actual values will be fairly small compared with the specs. in the datasheet.

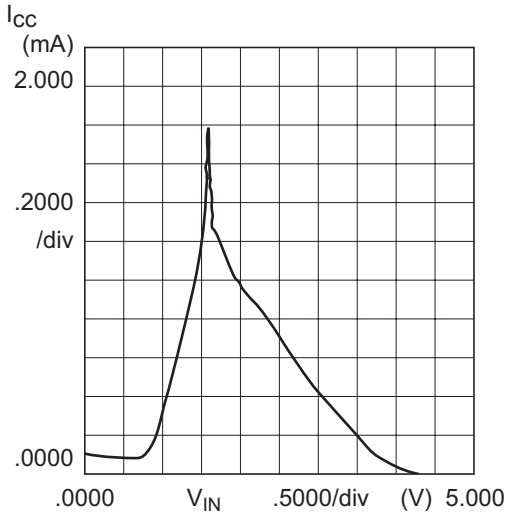

Figure 7 Input Voltage vs. I_{CC} Characteristics in HD74BC Series

Revision Record

Rev.	Date	Description	
		Page	Summary
1.00	Jul.09.04	—	First edition issued

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