Integrated Device Technology, Inc.

IDT79RV4700 PROCESSOR-BASED PCI CARD

PRELIMINARY
IDT7M9507

FEATURES:

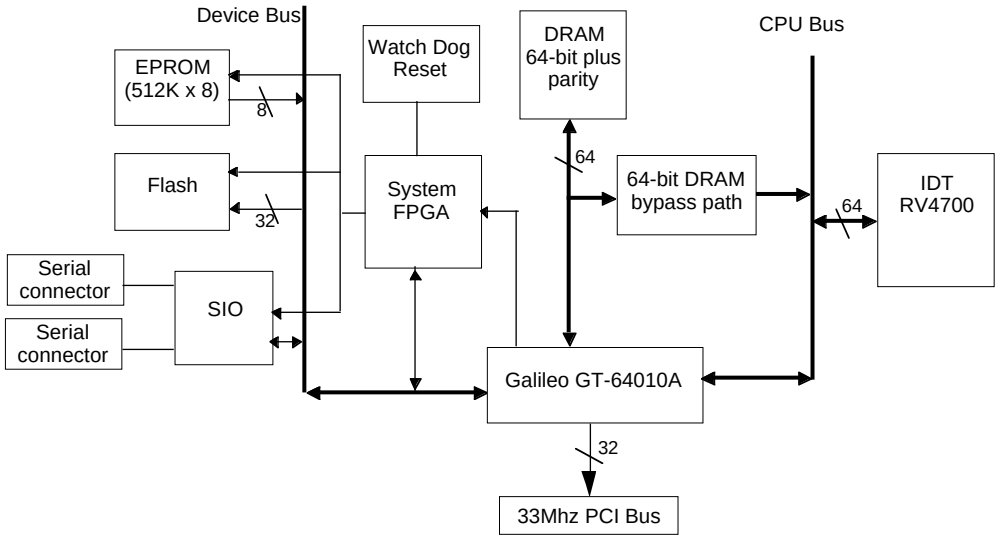
- Industry Standard PCI based expansion board
- High performance IDT79RV4700 CPU
  - 100MHz to 200MHz CPU frequencies supported
  - 50MHz maximum CPU bus frequency
- DRAM
  - two 72-position SIMM slots (gold contacts)
  - 4MB to 256MB of DRAM
  - 64-bit width to processor
  - parity generation and checking
- Flash
  - one 80-position JEDEC standard Flash SIMM slot (gold contacts)
  - 2MB to 8MB of Flash memory
  - 32-bit width
- EPROM
  - up to 512KB
  - 8-bit width
  - PLCC or DIP options (consult factory for availability)
- Debug Environment/Features
  - two serial interface ports
  - four software controlled LEDs
  - IDT/SIM Debug/Monitor (consult factory for other options)
- Uses Galileo GT-64010A single chip core logic function
- DMA
  - four independent channels
  - chaining via linked lists of records
  - byte alignment on source and destination
  - transfers through a 32 byte internal FIFO
  - moves data between PCI, memory and devices
- PCI
  - host to PCI bridge
  - PCI to main memory bridge
  - fully compatible to PCI rev 2.1
  - high performance PCI interfaces via 96 bytes of posted write and read prefetch buffers; 32-bit data bus
- Other Features
  - watch dog timer reset support (consult factory for other options)
  - software generated reset support both from local processor and from PCI bus
  - general purpose scratch pad register
  - hardware based masking of interrupts

DESCRIPTION:

The IDT7M9507 is a full size PCI card that consists of an IDT79RV4700 processor based subsystem that can either form the core CPU function for an embedded application, or it can be an optional add-in accelerator to a PCI based system.

It is designed to be plugged into any PCI based system or a passive PCI backplane such as the IDT7M9502. The card conforms to the full size PCI card form factor, and it contains all of the features required of a typical CPU subsystem for embedded processor applications. Some of these features include: dedicated DRAM/Flash, two serial ports, watchdog reset timer and software reset support.

FUNCTIONAL BLOCK DIAGRAM



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BOARD OVERVIEW

The IDT7M9507 consists of the following functional blocks: IDT79RV4700 processor, Galileo GT-64010A system controller, DRAM memory, system Glue Logic, Flash/EPROM and serial port controller. The IDT7M9507 CPU subsystem is designed to interface with its targeted system through a standard PCI bus interface.

IDT79RV4700 PROCESSOR

The IDT79RV4700 is a high performance cost-effective processor targeted at embedded applications which runs at internal frequencies from 100MHz to 200MHz.

GT-64010A PCI SYSTEM CONTROLLER

The GT-64010A is a system support core logic device from Galileo Technology, Inc. This chip provides the bulk of the system control and support functions required for a MIPS R4XXX/R5000 CPU based system. The GT-64010A has a three bus architecture. These three busses are: a CPU bus interface, a PCI bus interface and a memory/device bus interface. In addition the GT-64010A contains a DRAM controller and a DMA controller.

DRAM

The main memory is implemented using two standard 72-position DRAM SIMMs. Parity support is provided for in the main memory; however, it can be disabled by setting the appropriate register values in the GT-64010A. The main memory can be configured to operate in either 32-bit mode or in 64-bit mode; however, if the main memory is configured in 32-bit mode, only one SIMM is allowed to be populated. When the main memory is configured to operate in 64-bit mode, both SIMMs must be of the same type (e.g., 1M x 32/36).

The main memory is designed to support one or two banks of DRAM which is dependent on the type of SIMM being used. One bank is supported when single bank DRAM SIMMs are used (e.g., 1M x 32/36), and two banks are supported when double bank DRAM SIMMs are used (e.g., 2M x 32/36). The design can use any standard DRAM SIMM containing 4MB (1M x 32/36), 8MB (2M x 32/36), 16 MB (4M x 32/36), 32MB (8M x 32/36), 64MB (16M X 32/36), or 128MB (32M x 32/36) allowing the 7M9507 to have up to a maximum of 256MB of memory. The memory configuration is flexible and is field upgradeable.

SYSTEM FPGAS

The system FPGAs are responsible for processor initialization, reset control, General Purpose Register, device decoding, interrupt masking/mapping.

PROCESSOR INITIALIZATION

The 4700 requires a serial data stream for initialization. The initialization process is handled by the system Glue Logic. The Endian Mode and CPU clock ratio reset parameters can be configured by moving jumpers on the board.

RESET CONTROL

The 7M9507 supports several levels of reset:

- Power on reset
- Manual Cold Reset (a button on the board)
- SW Warm Reset
- PCI Reset – from the PCI bus (generates a Cold Reset to the CPU)
- Watchdog warm reset

The SW warm reset can be triggered either by the 7M9507 CPU or by the system host processor. This is accomplished by writing to a special register in the 7M9507 address space which is accessible to both to the 7M9507 local CPU and the system host processor.

INTERRUPT MASKING/MAPPING

The 7M9507 supports the following interrupts:

- GT-64010A interrupt
- Serial I/O interrupt
- PCI interrupts INTA#, INTB#, INTC# and INTD#

The PCI interrupts are run through the system FPGAs to allow for hardware based interrupt masking. If bit 0 of the General Purpose Register (Address: 0x1D000000) is set to 0, the PCI interrupts are masked, and the assertion of any of the PCI interrupts will not be recognized by the 7M9507. If bit 0 of the General Purpose Register is set to 1 the PCI interrupts are mapped as follows: PCI INTA# to CPU INT2*, PCI INTB# to CPU INT3*, PCI INTC# to CPU INT4*, PCI INTD# to CPU INT5*. Interrupts are not latched and must be cleared at the source.

BOOT EPROM

The Boot EPROM is a standard 512K x 8 EPROM which holds the boot code, the debug monitor and power-on diagnostics.

FLASH MEMORY

The flash Memory is a JEDEC standard flash Memory SIMM with a minimum configuration of 2 MB, expandable up to 8 MB. The flash Memory is used for storing the OS image code and optional configuration tables.

SERIAL PORT CONTROLLER

The serial port controller is an AM85C30, a standard serial controller from Advanced Micro Devices, Inc. (AMD) for connecting to an RS232 port. The serial port is used for monitoring the CPU, performing tests of the 7M9507 and general bring-up and debug of the 7M9507.

WATCHDOG RESET

The watchdog reset is generated from a MAX705. It is used to control the system reset logic and to provide a watchdog reset.

PCI BUS

The IDT7M9507 communicates with the system host processor through a standard PCI bus that is compliant with the PCI Rev 2.1 specification.

SOFTWARE MEMORY MAP

The following is the default memory map of the IDT7M9507. These values can be changed by writing to the appropriate address decode registers in the GT-64010A. The DRAM size listed below is the maximum DRAM size that can be used with the 7M9507 without updating the values of the DRAM address decode registers in the GT-64010A.

GT-64010A Physical Address	Size	Description	Device Select
0x00000000	8MB	DRAM Bank 0	—
0x00800000	8MB	DRAM Bank 1	—
0x10000000	—	PCI I/O	—
0x12000000	—	PCI Memory	—
0x14000000	—	GT-64010A Internal Registers	—
0x1FC00000	512KB	Boot EPROM	Boot CS*
0x1C800000	2MB	Flash Memory	CS1*
0x1C000000	1 byte	Serial Port (85C30)	CS0*
0x1C000000	1 byte	Channel B control/status	—
0x1C000004	1 byte	Channel B data	—
0x1C000008	1 byte	Channel A control/status	—
0x1C00000C	1 byte	Channel A data	—
0x1D000000	1 byte	Processor Scratchpad	CS2*
0x1DC00000	—	Watchdog Timer Strobe	CS2*
0x1F000000	—	SW Warm Reset	CS3*

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GENERAL PURPOSE REGISTER

The register bit definitions are shown in the table below. The reset values are set when RESET* (warm reset) is asserted.

Bit	Reset Value	Bit Definition
0	0	Interrupt Enable/LED0: set to 0 to disable PCI interrupts/turn off LED; set to 1 to enable interrupts/turn on LED
1	0	Watch Dog Enable/LED1: set to 1 to enable Watch Dog/turn on LED. (1)
2	0	General Purpose/LED2: set to 0 to turn off LED, set to 1 to turn on LED
3	0	General Purpose/LED3: set to 0 to turn off LED, set to 1 to turn on LED
4	0	General Purpose
5	0	General Purpose
6	0	General Purpose
7	0	General Purpose

NOTE:
1. This bit cannot be cleared (except by RESET*) once it has been set.

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POWER REQUIREMENTS

	7M9507S200M		7M9507S175M		7M9507S150M		7M9507S133M		7M9507S100M	
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
VCC	4.75V	5.25V	4.75V	5.25V	4.75V	5.25V	4.75V	5.25V	4.75V	5.25V
ICC	—	4.9	—	4.7A	—	4.5A	—	4.3A	—	4.1A

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ENVIRONMENTAL

	Temp. (°C)		Humidity (1)		Altitude	
Condition	Min	Max	Min	Max	Min	Max
Operating	0	50	20%	80%	0	10,000
Under Bias	-10	50	10%	90%	0	10,000
Storage	-25	60	10%	90%	0	

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NOTE:
1. Non-Condensing

PHYSICAL DIMENSIONS

The IDT7M9507 conforms to the dimensional requirements of a full size PCI card. The maximum component height on the primary component side of the card does not exceed 0.57 inches (14.48mm) and the maximum component height on the backside of the card does not exceed 0.105 inches (2.67mm).

ORDERING INFORMATION